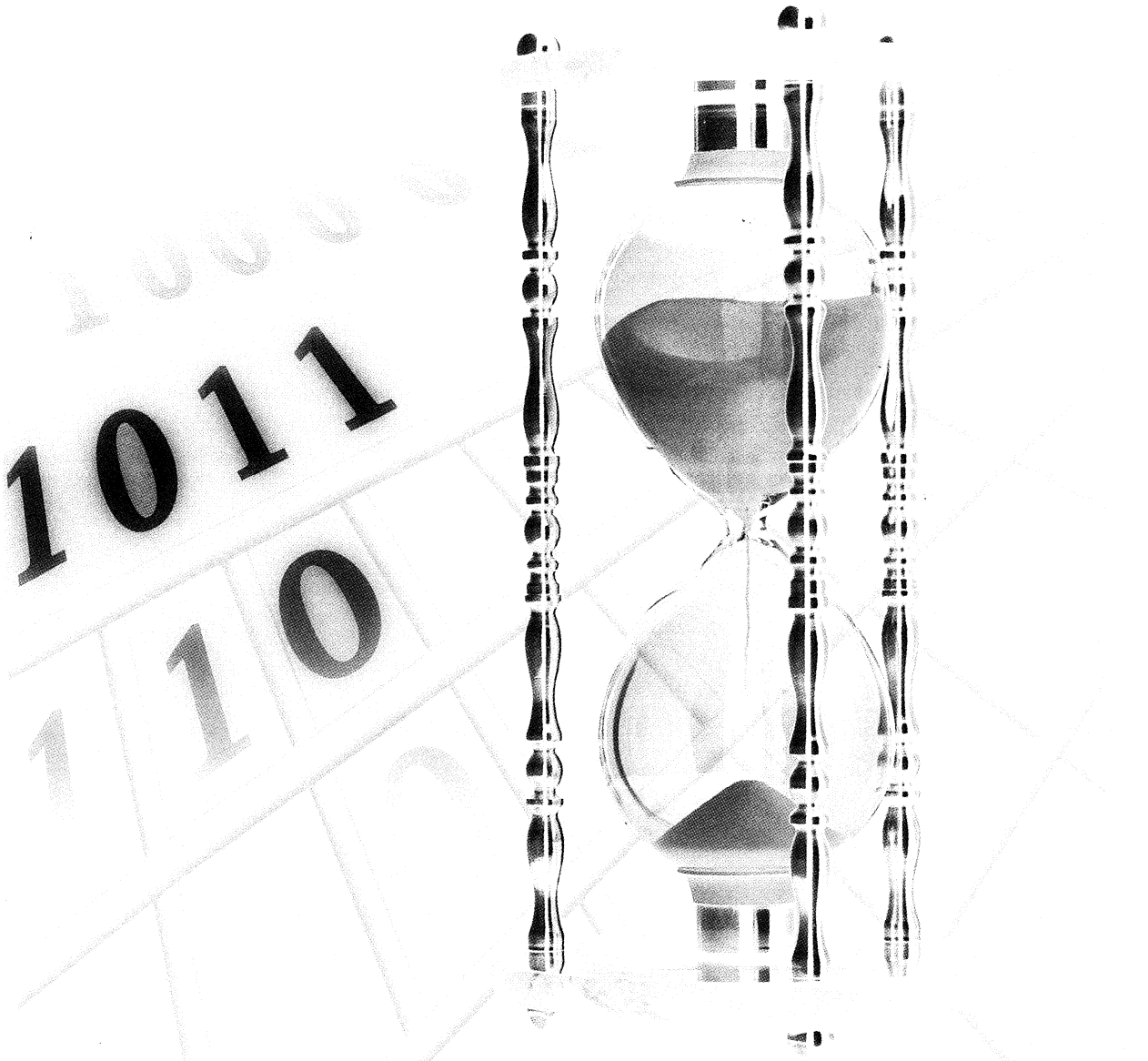

Timekeeping & NV SRAM Data Book

DALLAS SEMICONDUCTOR

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GENERAL INFORMATION

PART NUMBER	DESCRIPTION	DATA BOOK
DS0621	TMEX™ Professional Software Developer's Kit	Automatic Identification
DS0630x	TMEX™ Performance Modules	Automatic Identification
DS1000	5–Tap Silicon Delay Line	System Extension
DS1000–IND	Industrial Temperature Range 5–Tap Silicon Delay Line	System Extension
DS1003	4–Tap Silicon Delay Line for RISC Applications	System Extension
DS1004	5–Tap High–Speed Silicon Delay Line	System Extension
DS1005	5–Tap Silicon Delay Line	System Extension
DS1007	7–in–1 Silicon Delay Line	System Extension
DS1010	10–Tap Silicon Delay Line	System Extension
DS1012	2–in–1 Sub–Miniature Silicon Delay Line with Logic	System Extension
DS1013	3–in–1 Silicon Delay Line	System Extension
DS1020	Programmable 8–Bit Silicon Delay Line	System Extension
DS1021	Programmable 8-Bit Silicon Delay Line	System Extension
DS1033	3–in–1 Low–Voltage Silicon Delay Line	System Extension
DS1035	3–in–1 High–Speed Silicon Delay Line	System Extension
DS1040	Programmable One–Shot Pulse Generator	System Extension
DS1044	4–in–1 High–Speed Silicon Delay Line	System Extension
DS1045	4–Bit Dual Programmable Delay Line	System Extension
DS1200	Serial RAM Chip	Timekeeping and NV SRAM
DS1201	Electronic Tag	Timekeeping and NV SRAM
DS1202, DS1202S	Serial Timekeeping Chip	Timekeeping and NV SRAM
DS1204V	Electronic Key	Automatic Identification
DS1205S	MultiKey Chip	Automatic Identification
DS1205V	MultiKey	Automatic Identification
DS1206	Phantom Serial Interface Chip	System Extension
DS1207	TimeKey	Automatic Identification
DS1210	Nonvolatile Controller Chip	System Extension
DS1211	Nonvolatile Controller x 8 Chip	System Extension
DS1212	Nonvolatile Controller x 16 Chip	System Extension
DS1213B	SmartSocket 16K/64K	Timekeeping and NV SRAM
DS1213C	SmartSocket 256K	Timekeeping and NV SRAM
DS1213D	SmartSocket 256K/1M	Timekeeping and NV SRAM
DS1215	Phantom Time Chip	Timekeeping and NV SRAM
DS1216B	SmartWatch/RAM 16K/64K	Timekeeping and NV SRAM
DS1216C	SmartWatch/RAM 64K/256K	Timekeeping and NV SRAM
DS1216D	SmartWatch/RAM 256K/1M	Timekeeping and NV SRAM
DS1216E	SmartWatch/ROM 64K/256K	Timekeeping and NV SRAM
DS1216F	SmartWatch/ROM 64K/256K/1M	Timekeeping and NV SRAM
DS1217A	Nonvolatile Read/Write Cartridge	Timekeeping and NV SRAM
DS1217M	Nonvolatile Read/Write Cartridge	Timekeeping and NV SRAM
DS1218	Nonvolatile Controller	System Extension
DS1220AB/AD	16K Nonvolatile SRAM	Timekeeping and NV SRAM
DS1220Y	16K Nonvolatile SRAM	Timekeeping and NV SRAM
DS1221	Nonvolatile Controller x 4 Chip	System Extension
DS1222	BankSwitch Chip	System Extension
DS1225AB/AD	64K Nonvolatile SRAM	Timekeeping and NV SRAM
DS1225Y	64K Nonvolatile SRAM	Timekeeping and NV SRAM

PART NUMBER	DESCRIPTION	DATA BOOK
DS1228	+5V Powered Dual RS–232 Transmitter/Receiver	System Extension
DS1229	+5V Powered Triple RS–232 Transmitter/Receiver	System Extension
DS1230Y/AB	256K Nonvolatile SRAM	Timekeeping and NV SRAM
DS1231/S	Power Monitor Chip	System Extension
DS1232	MicroMonitor Chip	System Extension
DS1232LP/LPS	Low Power MicroMonitor Chip	System Extension
DS1233	5V EconoReset	System Extension
DS1233A	3.3V EconoReset	System Extension
DS1233D	5V EconoReset	System Extension
DS1233M	EconoReset	System Extension
DS1234	Conditional Nonvolatile Controller Chip	System Extension
DS1236	MicroManager Chip	System Extension
DS1236A	MicroManager Chip	System Extension
DS1237	DRAM Nonvolatizer Chip	System Extension
DS1238	MicroManager	System Extension
DS1238A	MicroManager	System Extension
DS1239	MicroManager Chip	System Extension
DS1243Y	64K NV SRAM with Phantom Clock	Timekeeping and NV SRAM
DS1244Y	256K NV SRAM with Phantom Clock	Timekeeping and NV SRAM
DS1245Y/AB	1024K Nonvolatile SRAM	Timekeeping and NV SRAM
DS1248Y	1024K NV SRAM with Phantom Clock	Timekeeping and NV SRAM
DS1249Y	2048K Nonvolatile SRAM	Timekeeping and NV SRAM
DS1250Y/AB	4096K Nonvolatile SRAM	Timekeeping and NV SRAM
DS1258YAB	128K x 16 Nonvolatile SRAM	Timekeeping and NV SRAM
DS1259	Battery Manager Chip	Timekeeping and NV SRAM
DS1260	Smart Battery	Timekeeping and NV SRAM
DS1267	Dual Digital Potentiometer Chip	System Extension
DS1275	Line–Powered RS–232 Transceiver Chip	System Extension
DS1280	3–Wire to Bytewide Converter Chip	Timekeeping and NV SRAM
DS1283	Watchdog Timekeeper Chip	Timekeeping and NV SRAM
DS1284	Watchdog Timekeeper Chip	Timekeeping and NV SRAM
DS1286	Watchdog Timekeeper	Timekeeping and NV SRAM
DS12885, DS12885Q, and DS12885T	Real Time Clock	Timekeeping and NV SRAM
DS12887	Real Time Clock	Timekeeping and NV SRAM
DS12887A	Real Time Clock	Timekeeping and NV SRAM
DS129x	Eliminator	System Extension
DS1302	Trickle Charge Timekeeping Chip	Timekeeping and NV SRAM
DS1305	Serial Alarm Real Time Clock	Timekeeping and NV SRAM
DS1307	64 X 8 Serial Real Time Clock	Timekeeping and NV SRAM
DS1315	Phantom Time Chip	Timekeeping and NV SRAM
DS1330Y/AB	256K Nonvolatile SRAM with Battery Monitor	Timekeeping and NV SRAM
DS1336	Afterburner Chip	System Extension
DS1345Y/AB	1024K Nonvolatile SRAM with Battery Monitor	Timekeeping and NV SRAM
DS1350Y/AB	4096K Nonvolatile SRAM with Battery Monitor	Timekeeping and NV SRAM
DS1380	RAMport	Timekeeping and NV SRAM
DS1381	NV SRAMport	Timekeeping and NV SRAM
DS1384	Watchdog Timekeeping Controller	Timekeeping and NV SRAM

PART NUMBER	DESCRIPTION	DATA BOOK
DS1385/DS1387	RAMified Real Time Clock 4K x 8	Timekeeping and NV SRAM
DS1386	RAMified Watchdog Timekeeper	Timekeeping and NV SRAM
DS1401	Front Panel Button Holder	Automatic Identification
DS1402	Button Cable	Automatic Identification
DS1410D	Parallel Port Button Holder	Automatic Identification
DS1410K	Parallel Holder Developer's Kit	Automatic Identification
DS1412	Serial Port Button Holder	Automatic Identification
DS1412K	Serial Holder Developer's Kit	Automatic Identification
DS1414	Network Button Holder	Automatic Identification
DS1414K	Authorization Button Developer's Kit	Automatic Identification
DS1420	Serial ID Button	Automatic Identification
DS1422	1Kbit Add–Only UniqueWare™ Button	Automatic Identification
DS1425	Multi Button™	Automatic Identification
DS1427	Time Button™	Automatic Identification
DS14285/DS14287	Real Time Clock with NVRAM Control	Timekeeping and NV SRAM
DS1485/DS1488	RAMified Real Time Clock 8K x 8	Timekeeping and NV SRAM
DS1486	RAMified Watchdog Timekeeper	Timekeeping and NV SRAM
DS1585/DS1587	Serialized Real Time Clocks	Timekeeping and NV SRAM
DS1602	Elapsed Time Counter	Timekeeping and NV SRAM
DS1603	Elapsed Time Counter Module	Timekeeping and NV SRAM
DS1608	EconoRAM Time Chip	Timekeeping and NV SRAM
DS1609	Dual Port RAM	Timekeeping and NV SRAM
DS1610	Partitioned NV Controller	System Extension
DS1613C	Partitioned SmartSocket 256K	Timekeeping and NV SRAM
DS1613D	Partitioned SmartSocket 1M	Timekeeping and NV SRAM
DS1620	Digital Thermometer and Thermostat	System Extension
DS1621	Digital Thermometer and Thermostat	System Extension
DS1623	Digital Thermometer and Thermostat	System Extension
DS1624	Digital Thermometer and Memory	System Extension
DS1625	Digital Thermometer and Thermostat	System Extension
DS1630Y/AB	Partitionable 256K NV SRAM	Timekeeping and NV SRAM
DS1632	PC Power Fail and Reset Controller	System Extension
DS1633	High–Speed Battery Recharger	System Extension
DS1633x	High–Speed Battery Charger	System Extension
DS1640/DS1640C	Personal Computer Power FET	System Extension
DS1642	Nonvolatile Timekeeping RAM	Timekeeping and NV SRAM
DS1643/DS1643LPM	Nonvolatile Timekeeping RAM	Timekeeping and NV SRAM
DS1644/DS1644LPM	Nonvolatile Timekeeping RAM	Timekeeping and NV SRAM
DS1645Y/AB	Partitionable 1024K NV SRAM	Timekeeping and NV SRAM
DS1646/DS1646LPM	Nonvolatile Timekeeping RAM	Timekeeping and NV SRAM
DS1647/DS1647LPM	Nonvolatile Timekeeping RAM	Timekeeping and NV SRAM
DS1650Y/AB	Partitionable 4096K NV SRAM	Timekeeping and NV SRAM
DS1651/DS1652	3–Code Lock/Key Match Memory System	System Extension
DS1652B	Code Memory Key	System Extension
DS1653/DS1652	4–Code Lock/Key Match Memory System	System Extension
DS1658Y/AB	Partitionable 128K x 16 NV SRAM	Timekeeping and NV SRAM
DS1666, DS1666S	Audio Digital Resistor	System Extension
DS1667	Digital Resistor with OP AMP	System Extension
DS1668, DS1669, DS1669S	Dallastat™ Electronic Digital Rheostat	System Extension
DS1670	Portable System Controller	Timekeeping and NV SRAM

PART NUMBER	DESCRIPTION	DATA BOOK
DS1685/DS1687	3 Volt/5 Volt Real Time Clock	Timekeeping and NV SRAM
DS1688/DS1691	3 Volt/5 Volt Serialized Real Time Clock with NVRAM Control	Timekeeping and NV SRAM
DS1689/DS1693	5 Volt/3 Volt Serialized Real Time Clock with NV SRAM Control	Timekeeping and NV SRAM
DS1705/DS1706	3.3 and 5.0 Volt MicroMonitor	System Extension
DS1707/DS1708	3.3 and 5.0 Volt MicroMonitor	System Extension
DS1710	Partitioned NV Controller	System Extension
DS17285/DS17287	3 Volt/5 Volt Real Time Clock	Timekeeping and NV SRAM
DS17485/DS17487	3 Volt/5 Volt Real Time Clock	Timekeeping and NV SRAM
DS17885/DS17887	3 Volt/5 Volt Real Time Clock	Timekeeping and NV SRAM
DS1800	Dual Inverting Log/Gain Attenuator	System Extension
DS1801	Dual Audio Taper Potentiometer	System Extension
DS1802	Dual Audio Taper Potentiometer with Pushbutton Control	System Extension
DS1803	Addressable Dual Digital Potentiometer	System Extension
DS1804	NV Trimmer Potentiometer	System Extension
DS1806	Digital Sextet Potentiometer	System Extension
DS1807	Addressable Dual Audio Taper Potentiometer	System Extension
DS1810	5V EconoReset	System Extension
DS1811	5V EconoReset	System Extension
DS1813	5V EconoReset with Pushbutton	System Extension
DS1815	5V EconoReset	System Extension
DS1816	3.3V EconoReset	System Extension
DS1818	3V EconoReset with Pushbutton	System Extension
DS1820	1–Wire™ Digital Thermometer	System Extension
DS1821	Programmable Digital Thermostat	System Extension
DS1832	3.3 Volt MicroMonitor Chip	System Extension
DS1833	5V EconoReset	System Extension
DS1834/A/D	Dual EconoReset with Pushbutton	System Extension
DS1836A/B/C/D	3.3V/5.5V MicroManager	System Extension
DS1866	Log Trimmer Potentiometer	System Extension
DS1867	Dual Digital Potentiometer with EEPROM	System Extension
DS1868	Dual Digital Potentiometer Chip	System Extension
DS1869	3V Dallastat™ Electronic Digital Rheostat	System Extension
DS1920	Touch Thermometer™	Automatic Identification
DS1971	256–Bit EEPROM Touch Memory™	Automatic Identification
DS1981U/DS1982U	UniqueWare™ Touch Memory	Automatic Identification
DS1982	1Kbit Add–Only Touch Memory™	Automatic Identification
DS1985	16Kbit Add–Only Touch Memory™	Automatic Identification
DS1986	64Kbit Add–Only Touch Memory™	Automatic Identification
DS1990A	Touch Serial Number™	Automatic Identification
DS1991	Touch MultiKey™	Automatic Identification
DS1992/DS1993	1Kbit/4Kbit Touch Memory™	Automatic Identification
DS1994	4Kbit Plus Time Touch Memory™	Automatic Identification
DS1995	16Kbit Touch Memory™	Automatic Identification
DS1996	64Kbit Touch Memory™	Automatic Identification
DS2009	512 x 9 FIFO Chip	Timekeeping and NV SRAM
DS2010	1024 x 9 FIFO Chip	Timekeeping and NV SRAM
DS2011	2048 x 9 FIFO Chip	Timekeeping and NV SRAM

PART NUMBER	DESCRIPTION	DATA BOOK
DS2012	4096 x 9 FIFO Chip	Timekeeping and NV SRAM
DS2016	2K x 8 3V Operation Static RAM	Timekeeping and NV SRAM
DS2064	8K x 8 3V Operation Static RAM	Timekeeping and NV SRAM
DS2105	SCSI Terminator	System Extension
DS21S07A	SCSI Terminator	System Extension
DS21S07C	SCSI Terminator	System Extension
DS2108	Differential SCSI Switchable Terminator	System Extension
DS2109	Plug and Play SCSI Terminator	System Extension
DS211	4 Driver/5 Receiver RS–232 Serial Port	PC Data Book
DS2110	Plug and Play SCSI Terminator with EEPROM	System Extension
DS2112	BTL Terminator	System Extension
DS2130Q	Voice Messaging Processor	Telecommunications
DS2132A/Q	Digital Answering Machine Processor	Telecommunications
DS2141A	T1 Controller	Telecommunications
DS21Q41B	Quad T1 Framer	Telecommunications
DS2143/DS2143Q	E1 Controller	Telecommunications
DS21Q43A	Quad E1 Framer	Telecommunications
DS2151Q	T1 Single–Chip Transceiver	Telecommunications
DS2153Q	E1 Single–Chip Transceiver	Telecommunications
DS2164Q	G.726 ADPCM Processor	Telecommunications
DS2165/DS2165Q	16/24/32Kbps ADPCM Processor	Telecommunications
DS2172	Bit Error Rate Tester (BERT)	Telecommunications
DS2175	T1/CEPT Elastic Store	Telecommunications
DS2176	T1 Receive Buffer	Telecommunications
DS2180A	T1 Transceiver	Telecommunications
DS2181A	CEPT Primary Rate Transceiver	Telecommunications
DS2182A	T1 Line Monitor	Telecommunications
DS2186	Transmit Line Interface	Telecommunications
DS2187	Receive Line Interface	Telecommunications
DS2188	T1/CEPT Jitter Attenuator	Telecommunications
DS222	Dual RS–232 Transmitter/Receiver with Shutdown	Telecommunications
DS2223/DS2224	EconoRAM	Automatic Identification
DS2227	Flexible NV SRAM Stik	Timekeeping and NV SRAM
DS2229	Word–Wide 8 Meg SRAM Stik	Timekeeping and NV SRAM
DS2250(T)	Soft Microcontroller	Soft Microcontroller
DS2251(T)	128K Soft Microcontroller	Soft Microcontroller
DS2252(T)	Secure Microcontroller	Soft Microcontroller
DS2282	T1 FDL Controller/Monitor Stik	Telecommunications
DS229	RS–232 Transmitter/Receiver	System Extension
DS2290	T1 Isolation Stik	Telecommunications
DS2291	T1 Long Loop Stik	Telecommunications
DS232A	Dual RS–232 Transmitter/Receiver	System Extension
DS233A	Dual RS–232 Transmitter/Receiver	System Extension
DS2401	Silicon Serial Number	Automatic Identification
DS2404	EconoRAM Time Chip	Timekeeping and NV SRAM
DS2404S–C01	Dual Port Memory Plus Time	Automatic Identification
DS2405	Addressable Switch	Automatic Identification
DS2407	Dual Addressable Switch Plus 1K–Bit Memory	Automatic Identification
DS2430A	256–Bit 1–Wire™ EEPROM	Automatic Identification

PART NUMBER	DESCRIPTION	DATA BOOK
DS2434	Battery Identification Chip	System Extension
DS2435	Battery Identification Chip with Time/Temperature Histogram	System Extension
DS2501–UNW/DS2502–UNW	UniqueWare™ Add–Only Touch Memory	Automatic Identification
DS2502	1Kbit Add–Only Memory	Automatic Identification
DS2505	16Kbit Add–Only Memory	Automatic Identification
DS2506	64Kbit Add–Only Memory	Automatic Identification
DS5000(T)	Soft Microcontroller	Soft Microcontroller
DS5000FP	Soft Microcontroller Chip	Soft Microcontroller
DS5000TK	Evaluation Kit	Soft Microcontroller
DS5001FP	128K Soft Micro Chip	Soft Microcontroller
DS5002FP	Secure Micro	Soft Microcontroller
DS80C310	High–Speed Micro	High–Speed Microcontroller
DS80C320	High–Speed Micro	High–Speed Microcontroller
DS80C323	Low–Power Micro	High–Speed Microcontroller
DS83C520	ROM High–Speed Micro	High–Speed Microcontroller
DS87C520	EPROM High–Speed Micro	High–Speed Microcontroller
DS87C530	EPROM Micro with Real Time Clock	High–Speed Microcontroller
DS9000	Bytewide Cable Harness	Timekeeping and NV SRAM
DS9002	Cartridge Housing	Timekeeping and NV SRAM
DS9003	Cartridge Proto Board	Timekeeping and NV SRAM
DS9091K	1–Wire™ MicroLAN™ Evaluation Kit	Automatic Identification
DS9092	Touch Memory Probe	Automatic Identification
DS9092K	Touch Memory Starter Kit	Automatic Identification
DS9092R	Touch Port	Automatic Identification
DS9093x	Touch Memory Mount Products	Automatic Identification
DS9094	MicroCan Clip	Automatic Identification
DS9096P	Touch Memory Adhesive Pads	Automatic Identification
DS9097/DS9097E	Touch COM Port Adapter	Automatic Identification
DS9098	MicroCan Retainer	Automatic Identification
DS9100	Touch and Hold Probe Stampings	Automatic Identification
DS9101	Multi–Purpose Clip	Automatic Identification
DS9103K	Touch Memory Access Control Demo Kit	Automatic Identification

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1200	10–Pin DIP	0 to 70	DS1200	
	10–Pin DIP	–40 to +85	DS1200N	
	16–Pin SOIC	0 to 70	DS1200S	
	16–Pin SOIC	–40 to +85	DS1200SN	
DS1201	Electronic Key/Tag	0 to 70	DS1201	
DS1202	8–Pin DIP	0 to 70	DS1202	24 x 8 RAM
	8–Pin DIP	–40 to +85	DS1202N	24 x 8 RAM
	8–Pin SOIC	0 to 70	DS1202S–8	24 x 8 RAM
	8–Pin SOIC	–40 to +85	DS1202SN–8	24 x 8 RAM
	16–Pin SOIC	0 to 70	DS1202S	24 x 8 RAM
	16–Pin SOIC	–40 to +85	DS1202SN	24 x 8 RAM
DS1213B	Socket	0 to 70	DS1213B	
DS1213C	Socket	0 to 70	DS1213C	
DS1213D	Socket	0 to 70	DS1213D	
DS1215	16–Pin DIP	0 to 70	DS1215	
	16–Pin DIP	–40 to +85	DS1215N	
	16–Pin SOIC	0 to 70	DS1215S	
DS1216B	28–Pin Socket	0 to 70	DS1216B	16K/64K RAM
DS1216C	28–Pin Socket	0 to 70	DS1216C	64K/256K RAM
DS1216D	32–Pin Socket	0 to 70	DS1216D	256K/1M RAM
DS1216E	28–Pin Socket	0 to 70	DS1216E	64K/256K ROM
DS1216F	32–Pin Socket	0 to 70	DS1216F	64K/256K/1M ROM
DS1217A		0 to +70	DS1217A 16K–25	16K Bit Density
		0 to +70	DS1217A 64K–25	64K Bit Density
		0 to +70	DS1217A 128K–25	128K Bit Density
		0 to +70	DS1217A 192K–25	192K Bit Density
		0 to +70	DS1217A 256K–25	256K Bit Density
DS1217M		0 to +70	DS1217M 512–25	512K Bit Density
		0 to +70	DS1217M 1–15	1 Megabit Density
		0 to +70	DS1217M 2–25	2 Megabit Density
		0 to +70	DS1217M 3–25	3 Megabit Density
		0 to +70	DS1217M 4–25	4 Megabit Density
DS1220AB/AD	24–Pin Encap. DIP	0 to +70	DS1220AB–200	5% tol. 200 ns
	24–Pin Encap. DIP	0 to +70	DS1220AB–150	5% tol. 150 ns
	24–Pin Encap. DIP	0 to +70	DS1220AB–120	5% tol. 120 ns
	24–Pin Encap. DIP	0 to +70	DS1220AB–100	5% tol. 100 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AB–200–IND	5% tol. 200 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AB–100–IND	5% tol. 100 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–200	10% tol. 200 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–150	10% tol. 150 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–120	10% tol. 120 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–100	10% tol. 100 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AD–200–IND	10% tol. 200 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AD–100–IND	10% tol. 100 ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1220Y	24–Pin Encap. DIP	0 to 70	DS1220Y–200	10% tol. 200 ns
	24–Pin Encap. DIP	0 to 70	DS1220Y–150	10% tol. 150 ns
	24–Pin Encap. DIP	0 to 70	DS1220Y–120	10% tol. 120 ns
	24–Pin Encap. DIP	0 to 70	DS1220Y–100	10% tol. 100 ns
	24–Pin Encap. DIP	–40 to +85	DS1220Y–200–IND	10% tol. 200 ns
	24–Pin Encap. DIP	–40 to +85	DS1220Y–100–IND	10% tol. 100 ns
DS1225AB/AD	28–Pin Encap. DIP	0 to 70	DS1225AB–200	5% tol. 200 ns
	28–Pin Encap. DIP	0 to 70	DS1225AB–150	5% tol. 150 ns
	28–Pin Encap. DIP	0 to 70	DS1225AB–85	5% tol. 85 ns
	28–Pin Encap. DIP	0 to 70	DS1225AB–70	5% tol. 70 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AB–200–IND	5% tol. 200 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AB–150–IND	5% tol. 150 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AB–70–IND	5% tol. 70 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–200	10% tol. 200 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–170	10% tol. 170 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–150	10% tol. 150 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–85	10% tol. 85 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–70	10% tol. 70 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AD–200–IND	10% tol. 200 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AD–150–IND	10% tol. 150 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AD–70–IND	10% tol. 70 ns
DS1225Y	28–Pin Encap. DIP	0 to 70	DS1225Y–200	10% tol. 200 ns
	28–Pin Encap. DIP	0 to 70	DS1225Y–170	10% tol. 170 ns
	28–Pin Encap. DIP	0 to 70	DS1225Y–150	10% tol. 150 ns
	28–Pin Encap. DIP	–40 to +85	DS1225Y–200–IND	10% tol. 200 ns
	28–Pin Encap. DIP	–40 to +85	DS1225Y–150–IND	10% tol. 150 ns
DS1230Y/AB	28–Pin Encap. DIP	0 to 70	DS1230AB–200	5% tol. 200 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–150	5% tol. 150 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–120	5% tol. 120 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–100	5% tol. 100 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–85	5% tol. 85 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–70	5% tol. 70 ns
	28–Pin Encap. DIP	–40 to +85	DS1230AB–200–IND	5% tol. 200 ns
	28–Pin Encap. DIP	–40 to +85	DS1230AB–120–IND	5% tol. 120 ns
	28–Pin Encap. DIP	–40 to +85	DS1230AB–70–IND	5% tol. 70 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–200	10% tol. 200 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–150	10% tol. 150 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–120	10% tol. 120 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–100	10% tol. 100 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–85	10% tol. 85 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–70	10% tol. 70 ns
	28–Pin Encap. DIP	–40 to +85	DS1230Y–200–IND	10% tol. 200 ns
	28–Pin Encap. DIP	–40 to +85	DS1230Y–120–IND	10% tol. 120 ns
	28–Pin Encap. DIP	–40 to +85	DS1230Y–70–IND	10% tol. 70 ns
	34–Pin LPM	0 to 70	DS1230BL–100	5% tol. 100 ns
	34–Pin LPM	0 to 70	DS1230BL–70	5% tol. 70 ns

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DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	34–Pin LPM	–40 to +85	DS1230BL–70–IND	5% tol 70 ns
	34–Pin LPM	0 to 70	DS1230YL–100	10% tol. 100 ns
	34–Pin LPM	0 to 70	DS1230YL–70	10% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1230YL–70–IND	10% tol 70 ns
DS1243Y	28–Pin Encap. DIP	0 to 70	DS1243Y–000	8K x 8 RAM; 200 ns
	28–Pin Encap. DIP	0 to 70	DS1243Y–120	8K x 8 RAM; 120 ns
	28–Pin Encap. DIP	0 to 70	DS1243Y–150	8K x 8 RAM; 150 ns
DS1244Y	28–Pin Encap. DIP	0 to 70	DS1244Y–000	32K x 8 RAM; 200 ns
	28–Pin Encap. DIP	0 to 70	DS1244Y–120	32K x 8 RAM; 120 ns
	28–Pin Encap. DIP	0 to 70	DS1244Y–150	32K x 8 RAM; 150 ns
DS1245Y/AB	32–Pin Encap. DIP	0 to 70	DS1245AB–120	5% tol. 120 ns
	32–Pin Encap. DIP	0 to 70	DS1245AB–100	5% tol. 100 ns
	32–Pin Encap. DIP	0 to 70	DS1245AB–85	5% tol. 85 ns
	32–Pin Encap. DIP	0 to 70	DS1245AB–70	5% tol. 70 ns
	32–Pin Encap. DIP	–40 to +85	DS1245AB–120–IND	5% tol. 120 ns
	32–Pin Encap. DIP	–40 to +85	DS1245AB–70–IND	5% tol. 70 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–120	10% tol. 120 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–100	10% tol. 100 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–85	10% tol. 85 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–70	10% tol. 70 ns
	32–Pin Encap. DIP	–40 to +85	DS1245Y–120–IND	10% tol. 120 ns
	32–Pin Encap. DIP	–40 to +85	DS1245Y–70–IND	10% tol. 70 ns
	34–Pin LPM	0 to 70	DS1245BL–100	5% tol. 100 ns
	34–Pin LPM	0 to 70	DS1245BL–70	5% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1245BL–70–IND	5% tol 70 ns
	34–Pin LPM	0 to 70	DS1245YL–100	10% tol. 100 ns
	34–Pin LPM	0 to 70	DS1245YL–70	10% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1245YL–70–IND	10% tol 70 ns
DS1248Y	32–Pin Encap. DIP	0 to 70	DS1248Y–000	128K x 8 RAM; 200 ns
	32–Pin Encap. DIP	0 to 70	DS1248Y–120	128K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1248Y–150	128K x 8 RAM; 150 ns
DS1249Y	32–Pin Encap. DIP	0 to 70	DS1249Y–100	10% tol. 100 ns
	32–Pin Encap. DIP	0 to 70	DS1249Y–85	10% tol. 85 ns
	32–Pin Encap. DIP	–40 to +85	DS1249Y–85–IND	10% tol. 85 ns
DS1250Y/AB	32–Pin Encap. DIP	0 to 70	DS1250AB–100	5% tol. 100 ns
	32–Pin Encap. DIP	0 to 70	DS1250AB–70	5% tol. 70 ns
	32–Pin Encap. DIP	–40 to +85	DS1250AB–70–IND	5% tol. 70 ns
	32–Pin Encap. DIP	0 to 70	DS1250Y–100	10% tol. 100 ns
	32–Pin Encap. DIP	0 to 70	DS1250Y–70	10% tol. 70 ns
	32–Pin Encap. DIP	–40 to +85	DS1250Y–70–IND	10% tol. 70 ns
	34–Pin LPM	0 to 70	DS1250BL–100	5% tol. 100 ns
	34–Pin LPM	0 to 70	DS1250BL–70	5% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1250BL–70–IND	5% tol. 70 ns
	34–Pin LPM	0 to 70	DS1230YL–100	10% tol. 100 ns
	34–Pin LPM	0 to 70	DS1230YL–70	10% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1250YL–70–IND	10% tol. 70 ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1258Y/AB	40–Pin Encap. DIP	0 to 70	DS1258AB–100	5% tol. 100 ns
	40–Pin Encap. DIP	0 to 70	DS1258AB–70	5% tol. 70 ns
	40–Pin Encap. DIP	–40 to +85	DS1258AB–70–IND	5% tol. 70 ns
	40–Pin Encap. DIP	0 to 70	DS1258Y–100	10% tol. 100 ns
	40–Pin Encap. DIP	0 to 70	DS1258Y–70	10% tol. 70 ns
	40–Pin Encap. DIP	–40 to +85	DS1258Y–70–IND	10% tol. 70 ns
DS1259	16–Pin DIP	0 to 70	DS1259	
	16–Pin DIP	–40 to +85	DS1259N	
	16–Pin SOIC	0 to 70	DS1259S	
	16–Pin SOIC	–40 to +85	DS1259SN	
DS1260		0 to 70	DS1260–25	250 mAHr
		0 to 70	DS1260–50	500 mAHr
		0 to 70	DS1260–100	1000 mAHr
DS1280	44–Pin Flat Pack	0 to 70	DS1280FP–44	
	80–Pin Flat Pack	0 to 70	DS1280FP–80	
DS1283	28–Pin DIP	0 to 70	DS1283	50 X 8 RAM
	28–Pin DIP	–40 to +85	DS1283N	50 x 8 RAM
	28–Pin SOIC	0 to 70	DS1283S	50 X 8 RAM
	28–Pin SOIC	–40 to +85	DS1283SN	50 x 8 RAM
DS1284	28–Pin DIP	0 to 70	DS1284	50 X 8 RAM
	28–Pin PLCC	0 to 70	DS1284Q	50 X 8 RAM
	28–Pin PLCC	–40 to +85	DS1284QN	50 X 8 RAM
DS1286	28–Pin Encap. DIP	0 to 70	DS1286	50 X 8 RAM
DS12885	24–Pin DIP	0 to 70	DS12885	114 X 8 RAM
	24–Pin SOIC	0 to 70	DS12885S	114 x 8 RAM
	28–Pin PLCC	0 to 70	DS12885Q	114 X 8 RAM
	28–Pin PLCC	–40 to +85	DS12885QN	114 x 8 RAM
	32–Pin TQFP	0 to 70	DS12885T	114 x 8 RAM
DS12887	24–Pin Encap. DIP	0 to 70	DS12887	114 X 8 RAM
DS12887A	24–Pin Encap. DIP	0 to 70	DS12887A	114 X 8 RAM
DS1302	8–Pin DIP	0 to 70	DS1302	31 x 8 RAM
	8–Pin DIP	–40 to +85	DS1302N	31 x 8 RAM
	8–Pin SOIC	0 to 70	DS1302S	31 x 8 RAM
	8–Pin SOIC	–40 to +85	DS1302SN	31 x 8 RAM
	8–Pin SOIC	0 to 70	DS1302Z	31 x 8 RAM
	8–Pin SOIC	–40 to +85	DS1302ZN	31 x 8 RAM
DS1305	16–Pin DIP	0 to 70	DS1305	96 x 8 RAM
	16–Pin DIP	–40 to +85	DS1305N	96 x 8 RAM
	20–Pin TSSOP	0 to 70	DS1305E	96 x 8 RAM
	20–Pin TSSOP	0 to 70	DS1305EN	96 x 8 RAM
DS1307	8–Pin DIP	0 to 70	DS1307	56 x 8 RAM
	8–Pin DIP	–45 to +85	DS1307N	56 x 8 RAM
	8–Pin SOIC	0 to 70	DS1307Z	56 x 8 RAM
	8–Pin SOIC	–40 to +85	DS1307ZN	56 x 8 RAM

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1315	16–Pin DIP	0 to 70	DS1315	
	16–Pin DIP	–40 to +85	DS1315N	
	16–Pin SOIC	0 to 70	DS1315S	
	16–Pin SOIC	–40 to +85	DS1315SN	
	20–Pin TSSOP	0 to 70	DS1315E	
	20–Pin TSSOP	–45 to +85	DS1315EN	
DS1330Y/AB	34–Pin LPM	0 to 70	DS1330BL–100	5% tol. 100 ns
	34–Pin LPM	0 to 70	DS1330BL–70	5% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1330BL–70–IND	5% tol. 70 ns
	34–Pin LPM	0 to 70	DS1330YL–100	10% tol. 100 ns
	34–Pin LPM	0 to 70	DS1330YL–70	10% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1330YL–70–IND	10% tol. 70 ns
DS1345Y/AB	34–Pin LPM	0 to 70	DS1345BL–100	5% tol. 100 ns
	34–Pin LPM	0 to 70	DS1345BL–70	5% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1345BL–70–IND	5% tol. 70 ns
	34–Pin LPM	0 to 70	DS1345YL–100	10% tol. 100 ns
	34–Pin LPM	0 to 70	DS1345YL–70	10% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1345YL–70–IND	10% tol. 70 ns
DS1350Y/AB	34–Pin LPM	0 to 70	DS1350BL–100	5% tol. 100 ns
	34–Pin LPM	0 to 70	DS1350BL–70	5% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1350BL–70–IND	5% tol. 70 ns
	34–Pin LPM	0 to 70	DS1350YL–100	10% tol. 100 ns
	34–Pin LPM	0 to 70	DS1350YL–70	10% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1350YL–70–IND	10% tol. 70 ns
DS1380	24–Pin DIP	0 to 70	DS1380	
	24–Pin SOIC	0 to 70	DS1380S	
DS1381	24–Pin Encap. DIP	0 to 70	DS1381	
DS1384	44–Pin QFP	0 to 70	DS1384FP–150	50 x 8 RAM; 150 ns
	44–Pin QFP	0 to 70	DS1384FP–120	50 x 8 RAM; 120 ns
	44–Pin TQFP	0 to 70	DS1384T–150	50 x 8 RAM; 150 ns
	44–Pin TQFP	0 to 70	DS1384T–120	50 x 8 RAM; 120 ns
DS1385	24–Pin DIP	0 to 70	DS1385	4K x 8 RAM
	28–Pin SOIC	0 to 70	DS1385S	4K x 8 RAM
DS1386	32–Pin Encap. DIP	0 to 70	DS1386–8–120	8K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1386–8–150	8K x 8 RAM; 150 ns
	32–Pin Encap. DIP	0 to 70	DS1386–32–120	32K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1386–32–150	32K x 8 RAM; 150 ns
DS1387	24–Pin Encap. DIP	0 to 70	DS1387	4K x 8 RAM
DS14285	24–Pin DIP	0 to 70	DS14285	
	24–Pin SOIC	0 to 70	DS14285S	
	28–Pin PLCC	0 to 70	DS14285Q	
DS14287	24–Pin Encap. DIP	0 to 70	DS14287	
DS1485	24–Pin DIP	0 to 70	DS1485	8K x 8 RAM
	28–Pin SOIC	0 to 70	DS1485S	8K x 8 RAM
DS1486	32–Pin Encap. DIP	0 to 70	DS1486–120	128K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1486–150	128K x 8 RAM; 150 ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1488	24–Pin Encap. DIP	0 to 70	DS1488	8K x 8 RAM
DS1585	28–Pin DIP	0 to 70	DS1585	8K x 8 RAM
	28–Pin SOIC	0 to 70	DS1585S	8K x 8 RAM
DS1587	28–Pin Encap. DIP	0 to 70	DS1587	8K x 8 RAM
DS1602	8–Pin DIP	–40 to +85	DS1602	
	8–Pin SOIC	–40 to +85	DS1602S	
DS1603	7–Pin Encap. SIP	0 to 70	DS1603	
DS1608	16–Pin DIP	0 to 70	DS1608	512 x 8 RAM
	16–Pin SOIC	0 to 70	DS1608S	512 x 8 RAM
DS1609	24–Pin DIP	–40 to +85	DS1609	
	24–Pin SOIC	–40 to +85	DS1609S	
DS1613C	Socket	0 to 70	DS1613C	
DS1613D	Socket	0 to 70	DS1613D	
DS1630Y/AB	28–Pin Encap. DIP	0 to 70	DS1630AB–120	5% tol. 120 ns
	28–Pin Encap. DIP	0 to 70	DS1630AB–100	5% tol. 100 ns
	28–Pin Encap. DIP	0 to 70	DS1630AB–85	5% tol. 85 ns
	28–Pin Encap. DIP	0 to 70	DS1630AB–70	5% tol. 70 ns
	28–Pin Encap. DIP	–40 to +85	DS1630AB–70–IND	5% tol. 70 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–120	10% tol. 120 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–100	10% tol. 100 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–85	10% tol. 85 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–70	10% tol. 70 ns
	28–Pin Encap. DIP	–40 to +85	DS1630Y–70–IND	10% tol. 70 ns
	34–Pin LPM	0 to 70	DS1630BL–100	5% tol. 100 ns
	34–Pin LPM	0 to 70	DS1630BL–70	5% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1630BL–70–IND	5% tol. 70 ns
	34–Pin LPM	0 to 70	DS1630YL–100	10% tol. 100 ns
	34–Pin LPM	0 to 70	DS1630YL–70	10% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1630YL–70–IND	10% tol. 70 ns
DS1642	24–Pin Encap. DIP	0 to 70	DS1642–120	2K x 8 RAM; 120 ns
	24–Pin Encap. DIP	0 to 70	DS1642–150	2K x 8 RAM; 150 ns
DS1643	28–Pin Encap. DIP	0 to 70	DS1643–120	8K x 8 RAM; 120 ns
	28–Pin Encap. DIP	0 to 70	DS1643–150	8K x 8 RAM; 150 ns
	26–Pin LPM	0 to 70	DS1643L–120	8K x 8 RAM; 120 ns
	26–Pin LPM	0 to 70	DS1643L–150	8K x 8 RAM; 150 ns
DS1644	28–Pin Encap. DIP	0 to 70	DS1644–120	32K x 8 RAM; 120 ns
	28–Pin Encap. DIP	0 to 70	DS1644–150	32K x 8 RAM; 150 ns
	34–Pin LPM	0 to 70	DS1644L–120	32K x 8 RAM; 120 ns
	34–Pin LPM	0 to 70	DS1644L–150	32K x 8 RAM; 150 ns
DS1645Y/AB	32–Pin Encap. DIP	0 to 70	DS1645AB–120	5% tol. 120 ns
	32–Pin Encap. DIP	0 to 70	DS1645AB–100	5% tol. 100 ns
	32–Pin Encap. DIP	0 to 70	DS1645AB–85	5% tol. 85 ns
	32–Pin Encap. DIP	0 to 70	DS1645AB–70	5% tol. 70 ns
	32–Pin Encap. DIP	–40 to +85	DS1645AB–70–IND	5% tol. 70 ns
	32–Pin Encap. DIP	0 to 70	DS1645Y–120	10% tol. 120 ns
	32–Pin Encap. DIP	0 to 70	DS1645Y–100	10% tol. 100 ns

ORDERING INFORMATION

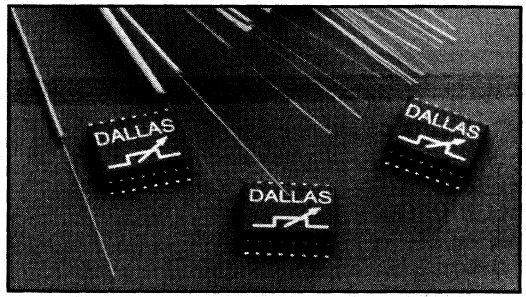
DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	32–Pin Encap. DIP	0 to 70	DS1645Y–85	10% tol. 85 ns
	32–Pin Encap. DIP	0 to 70	DS1645Y–70	10% tol. 70 ns
	32–Pin Encap. DIP	–40 to +85	DS1645Y–70–IND	10% tol. 70 ns
	34–Pin LPM	0 to 70	DS1645BL–100	5% tol. 100 ns
	34–Pin LPM	0 to 70	DS1645BL–70	5% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1645BL–70–IND	5% tol. 70 ns
	34–Pin LPM	0 to 70	DS1645YL–100	10% tol. 100 ns
	34–Pin LPM	0 to 70	DS1645YL–70	10% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1645YL–70–IND	10% tol. 70 ns
DS1645EE	32–Pin Encap. DIP	0 to 70	DS1645EE–100	10% tol. 100 ns
	32–Pin Encap. DIP	0 to 70	DS1645EE–85	10% tol. 85 ns
	32–Pin Encap. DIP	0 to 70	DS1645EE–70	10% tol. 70 ns
	32–Pin Encap. DIP	–40 to +85	DS1645EE–70–IND	10% tol. 70 ns
DS1646	32–Pin Encap. DIP	0 to 70	DS1646–120	128K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1646–150	128K x 8 RAM; 150 ns
	34–Pin LPM	0 to 70	DS1646L–120	128K x 8 RAM; 120 ns
	34–Pin LPM	0 to 70	DS1646L–150	128K x 8 RAM; 150 ns
DS1647	32–Pin Encap. DIP	0 to 70	DS1647–150	128K x 8 RAM; 150 ns
	32–Pin Encap. DIP	0 to 70	DS1647–120	128K x 8 RAM; 120 ns
	34–Pin LPM	0 to 70	DS1647L–150	128K x 8 RAM; 150 ns
	34–Pin LPM	0 to 70	DS1647L–120	128K x 8 RAM; 120 ns
DS1650Y/AB	32–Pin Encap. DIP	0 to 70	DS1650AB–100	5% tol. 100 ns
	32–Pin Encap. DIP	0 to 70	DS1650AB–85	5% tol. 85 ns
	32–Pin Encap. DIP	0 to 70	DS1650AB–70	5% tol. 70 ns
	32–Pin Encap. DIP	–40 to +85	DS1650AB–70–IND	5% tol. 70 ns
	32–Pin Encap. DIP	0 to 70	DS1650Y–100	10% tol. 100 ns
	32–Pin Encap. DIP	0 to 70	DS1650Y–85	10% tol. 85 ns
	32–Pin Encap. DIP	0 to 70	DS1650Y–70	10% tol. 70 ns
	32–Pin Encap. DIP	–40 to +85	DS1650Y–70–IND	10% tol. 70 ns
	34–Pin LPM	0 to 70	DS1650BL–100	5% tol. 100 ns
	34–Pin LPM	0 to 70	DS1650BL–70	5% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1650BL–70–IND	5% tol. 70 ns
	34–Pin LPM	0 to 70	DS1650YL–100	10% tol. 100 ns
	34–Pin LPM	0 to 70	DS1650YL–70	10% tol. 70 ns
	34–Pin LPM	–40 to +85	DS1650YL–70–IND	10% tol. 70 ns
DS1658Y/AB	40–Pin Encap. DIP	0 to 70	DS1658AB–100	5% tol. 100 ns
	40–Pin Encap. DIP	0 to 70	DS1658AB–70	5% tol. 70 ns
	40–Pin Encap. DIP	–40 to +85	DS1658AB–70–IND	5% tol. 70 ns
	40–Pin Encap. DIP	0 to 70	DS1658Y–100	10% tol. 100 ns
	40–Pin Encap. DIP	0 to 70	DS1658Y–70	10% tol. 70 ns
	40–Pin Encap. DIP	–40 to +85	DS1658Y–70–IND	10% tol. 70 ns
DS1670	20–Pin SOIC	0 to 70	DS1670S	
	20–Pin TSSOP	0 to 70	DS1670E	

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1685	24–Pin DIP	0 to 70	DS1685–3	3 volt
	24–Pin DIP	0 to 70	DS1685–5	5 volt
	24–Pin TSSOP	0 to 70	DS1685E–3	3 volt
	24–Pin TSSOP	0 to 70	DS1685E–5	5 volt
	28–Pin PLCC	0 to 70	DS1685Q–3	3 volt
	28–Pin PLCC	0 to 70	DS1685Q–5	5 volt
	24–Pin SOIC	0 to 70	DS1685S–3	3 volt
	24–Pin SOIC	0 to 70	DS1685S–5	5 volt
DS1687	24–Pin Encap. DIP	0 to 70	DS1687–3	3 volt
	24–Pin Encap. DIP	0 to 70	DS1687–5	5 volt
DS1688	28–Pin DIP	0 to 70	DS1688	
	28–Pin SOIC	0 to 70	DS1688S	
DS1689	28–Pin DIP	0 to 70	DS1689	114 x 8 RAM
	28–Pin SOIC	0 to 70	DS1689S	114 x 8 RAM
DS1691	28–Pin Encap. DIP	0 to 70	DS1691	
DS1693	28–Pin Encap. DIP	0 to 70	DS1693	114 x 8 RAM
DS17285	24–Pin DIP	0 to 70	DS17285–3	3 volt
	24–Pin DIP	0 to 70	DS17285–5	5 volt
	28–Pin TSOP	0 to 70	DS17285E–3	3 volt
	28–Pin TSOP	0 to 70	DS17285E–5	5 volt
	24–Pin SOIC	0 to 70	DS17285S–3	3 volt
	24–Pin SOIC	0 to 70	DS17285S–5	5 volt
DS17287	24–Pin Encap. DIP	0 to 70	DS17287–3	3 volt
	24–Pin Encap. DIP	0 to 70	DS17287–5	5 volt
DS17485	24–Pin DIP	0 to 70	DS17485–3	3 volt
	24–Pin DIP	0 to 70	DS17485–5	5 volt
	28–Pin TSOP	0 to 70	DS17485E–3	3 volt
	28–Pin TSOP	0 to 70	DS17485E–5	5 volt
	24–Pin SOIC	0 to 70	DS17485S–3	3 volt
	24–Pin SOIC	0 to 70	DS17485S–5	5 volt
DS17487	24–Pin Encap. DIP	0 to 70	DS17487–3	3 volt
	24–Pin Encap. DIP	0 to 70	DS17487–5	5 volt
DS17885	24–Pin DIP	0 to 70	DS17885–3	3 volt
	24–Pin DIP	0 to 70	DS17885–5	5 volt
	28–Pin TSOP	0 to 70	DS17885E–3	3 volt
	28–Pin TSOP	0 to 70	DS17885E–5	5 volt
	24–Pin SOIC	0 to 70	DS17885S–3	3 volt
	24–Pin SOIC	0 to 70	DS17885S–5	5 volt
DS17887	24–Pin Encap. DIP	0 to 70	DS17887–3	3 volt
	24–Pin Encap. DIP	0 to 70	DS17887–5	5 volt
DS2009	28–Pin DIP (600 MIL)	0 to 70	DS2009–35	35 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2009N–35	35 ns

ORDERING INFORMATION

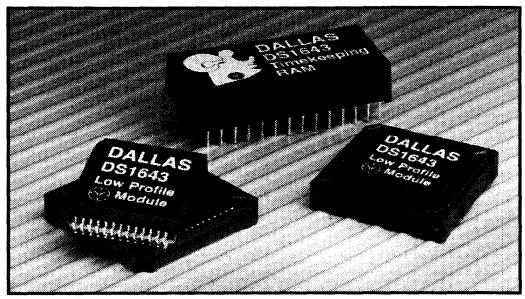
DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	28–Pin DIP (600 MIL)	–40 to +85	DS2009N–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–35	35 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–65	65 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–80	80 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–120	120 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009DN–35	35 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009DN–50	50 ns
	32–Pin PLCC	0 to 70	DS2009R–35	35 ns
	32–Pin PLCC	0 to 70	DS2009R–50	50 ns
	32–Pin PLCC	0 to 70	DS2009R–65	65 ns
	32–Pin PLCC	0 to 70	DS2009R–80	80 ns
	32–Pin PLCC	0 to 70	DS2009R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2009RN–35	35 ns
	32–Pin PLCC	–40 to +85	DS2009RN–50	50 ns
DS2010	28–Pin DIP (600 MIL)	0 to 70	DS2010–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2010N–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–65	65 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–80	80 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–120	120 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2010DN–50	50 ns
	32–Pin PLCC	0 to 70	DS2010R–50	50 ns
	32–Pin PLCC	0 to 70	DS2010R–65	65 ns
	32–Pin PLCC	0 to 70	DS2010R–80	80 ns
	32–Pin PLCC	0 to 70	DS2010R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2010RN–50	50 ns
DS2011	28–Pin DIP (600 MIL)	0 to 70	DS2011–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2011N–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–65	65 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–80	80 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–120	120 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2011DN–50	50 ns
	32–Pin PLCC	0 to 70	DS2011R–50	50 ns
	32–Pin PLCC	0 to 70	DS2011R–65	65 ns
	32–Pin PLCC	0 to 70	DS2011R–80	80 ns
	32–Pin PLCC	0 to 70	DS2011R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2011RN–50	50 ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS2012	28–Pin DIP (600 MIL)	0 to 70	DS2012–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2012N–50	50 ns
	32–Pin PLCC	0 to 70	DS2012R–50	50 ns
	32–Pin PLCC	0 to 70	DS2012R–65	65 ns
	32–Pin PLCC	0 to 70	DS2012R–80	80 ns
	32–Pin PLCC	0 to 70	DS2012R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2012RN–50	50 ns
DS2013	28–Pin DIP (600 MIL)	0 to 70	DS2013–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2013–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2013–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2013–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2013N–50	50 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–50	50 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–65	65 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–80	80 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–120	120 ns
	32–Pin DIP (300 MIL)	–40 to +85	DS2013DN–50	50 ns
DS2016	24–Pin DIP	–40 to +85	DS2016	100 ns
	24–Pin SOIC	–40 to +85	DS2016S	100 ns
DS2064	28–Pin DIP	–40 to +85	DS2064–200	200 ns
	28–Pin SOIC	–40 to +85	DS2064S–200	200 ns
DS2227	STIK	0 to 70	DS2227–120	120 ns
	STIK	0 to 70	DS2227–100	100 ns
	STIK	0 to 70	DS2227–70	70 ns
DS2229	STIK	0 to 70	DS2229–85	85 ns
DS2404	16–Pin DIP	0 to 70	DS2404	512 x 8 RAM
	16–Pin SOIC	0 to 70	DS2404S	512 x 8 RAM
	16–Pin SSOP	0 to 70	DS2404B	512 x 8 RAM
DS9000			DS9000	
DS9002			DS9002	
DS9003			DS9003	



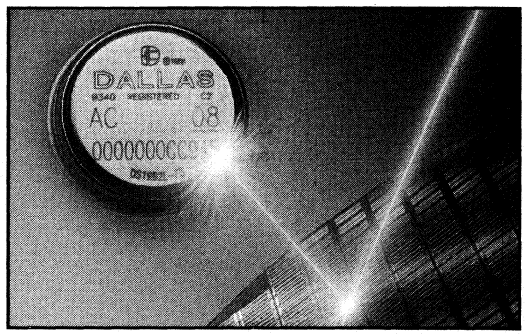
Silicon Timed Circuits

Silicon Timed Circuits (often referred to as delay lines) are chips that make subtle adjustments to the timing of high-performance electronics so that they will perform optimally. Because of the precision that lasers provide, some Silicon Timed Circuits can make timing adjustments down to a fraction of a nanosecond, which is the time it takes light to travel about a foot. For more information, call our Timing Problem Hotline at (214) 450-5348.



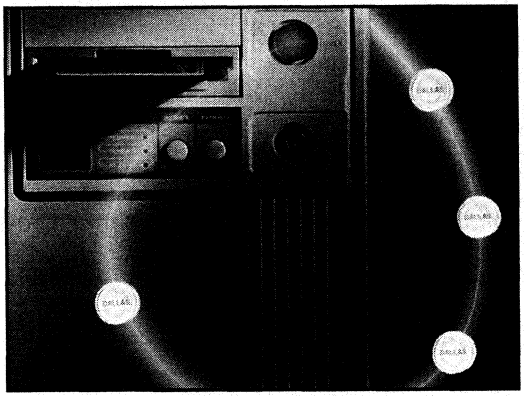
Timekeeping

A self-contained lithium energy source in conjunction with a silicon chip and quartz form a permanently powered clock/calendar within a single component. Various computer interfaces are available including phantom, serial, PC DOS, and bytewide memory.



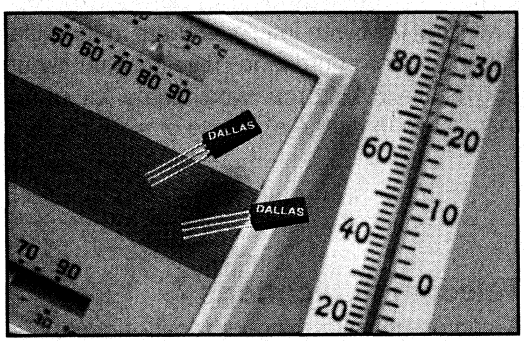
Automatic Identification

Touch Memory™ is a self-stick, Silicon Label™ in a stainless steel can. This MicroCan™ provides all the advantages canning has to offer, such as low cost, ruggedness, and the ability to preserve contents. The MicroCan's greatest advantage, however, is that a standalone chip can leave the confines of the computer and travel virtually anywhere to bring digital data to the point of use. Information can be updated time after time while the label is still affixed to its object. Wherever the silicon-labelled object goes, information is served up on the spot without recourse to remote networks. This family also includes low-cost memory chips in T0-92 packages.



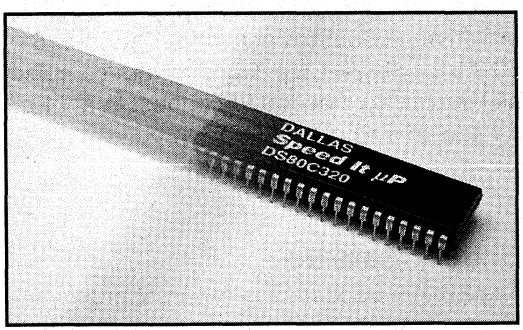
Software Authorization

Software Authorization products protect software applications from unauthorized execution and provide a means for PC and network access control. Software protection is achieved by using a Button as the "on" switch for a software application. The presence of a Button and validity of its contents determine the right to use. Buttons are very effective for implementing time- or count-based metering as a way of extending the temporary right to use software while maintaining protection control.



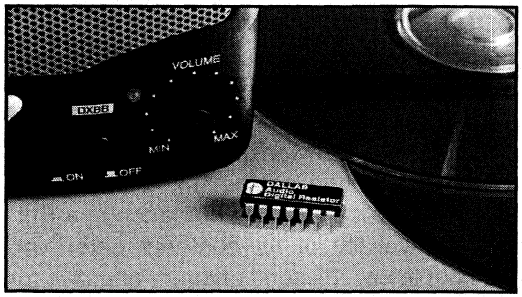
Thermal Management

Dallas Semiconductor makes thermal management easy with its line of direct-to-digital temperature sensors. These sensors provide a digital reading of temperature directly, eliminating the need for A/D converters dedicated to temperature measurement. Factory-calibrated to relieve the user of linearity corrections and other compensation, Dallas' sensors provide a range and accuracy unparalleled in the industry.



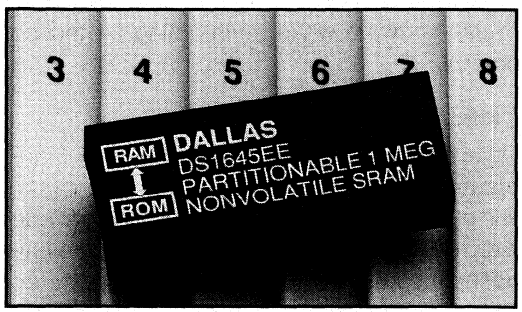
Microcontrollers

The DS80C320 High-Speed Micro is an 8051 family device that offers the highest performance in the industry for an 8-bit microcontroller. Pin- and instruction set-compatible with the standard 80C32, the High-Speed Micro uses only 4 clocks per instruction, as compared with 12 on other 8051's. Our DS500x Soft Micros convert industry-standard bytewide SRAM into high-performance, nonvolatile read/write storage.



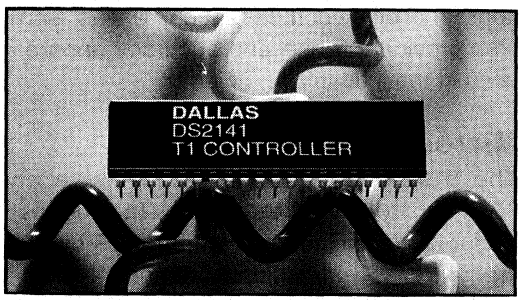
System Extension

These products add a variety of special features to systems without encumbering design. A digital potentiometer is an all-silicon version of an electrical element used in almost all electronic equipment. CPU supervisors monitor vital conditions for a microprocessor.



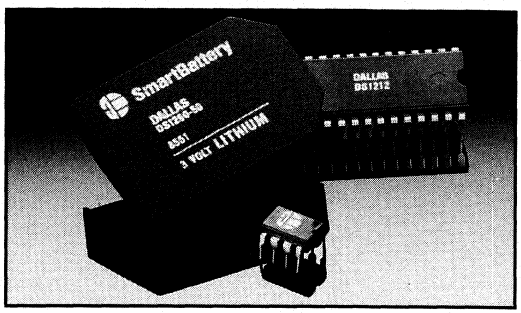
Nonvolatile RAM

Dallas Semiconductor has combined its circuitry and understanding of ultra low-power CMOS SRAM with improvements in long-life lithium power sources to develop a family of nonvolatile RAMs that retain data for more than 10 years in the absence of main power.



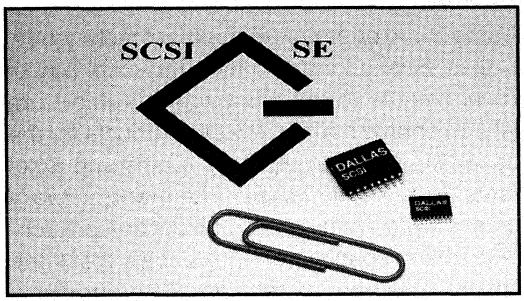
Telecommunications

A comprehensive product family addresses the requirements of high-speed, digital voice/data transmission and monitoring in T1, CEPT, or Primary Rate ISDN networks. The DS2151/53 T1/E1 Single-Chip Transceivers combine all the circuitry needed to connect to a T1 or E1 line in a single package.



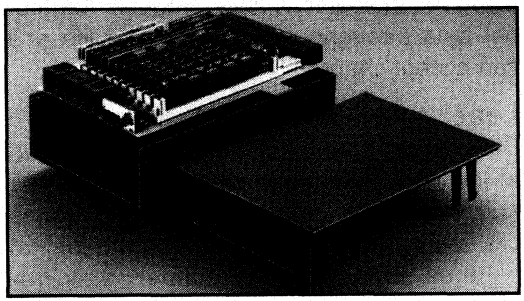
Battery Backup

The Battery Backup chip set crashproofs microprocessor-based systems, ensuring that no information is lost when main power fails. When power returns, computing resumes as if the failure had not occurred.



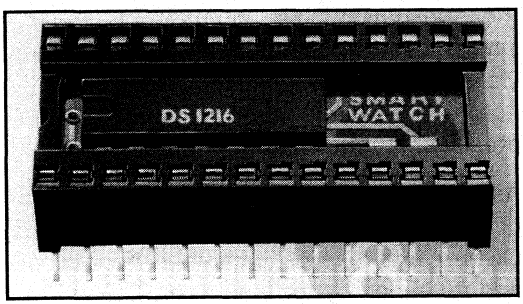
Bus Terminators

Bus termination products provide precise tolerance for high performance systems. SCSI terminators support all parallel SCSI standards including SCSI-3 Parallel Interface (SPI) and SCSI-3 Fast-20. The BTL terminator enhances Futurebus+ and BTL backplane designs by eliminating the specialized 2.1V supply.



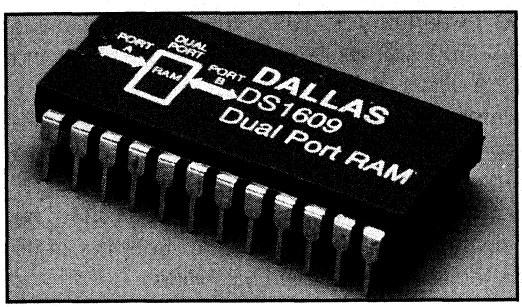
SIP Stik Prefabs

SIP Stiks are pretested subassemblies that snap into locking connectors for rapid construction of electronic systems. SIP Stiks increase density over traditional packing schemes five times by taking advantage of three, rather than the standard two, dimensions. SIP Stiks insert perpendicularly into the motherboard, making efficient use of the height dimension.



Intelligent Sockets

Intelligent Sockets incorporate active electronics in connectors that can be plugged into a system. Each adds an important capability without requiring substantive changes in the system. Some products in this family safeguard data in RAM for more than 10 years in the absence of external power. Others can time stamp and date events as well as nonvolatize RAM.



Multiport Memory

A complete family of FIFOs features identical pinouts that allow them to be interchanged. Designed for first-in, first-out processing for storing and retrieving data, the products are dual-ported for simultaneous reads and writes.

Dallas Semiconductor Corporation designs, manufactures, and markets electronic chips and chip-based subsystems. Founded in 1984, the Company uses customer problems as an entry point to develop products with widespread applications. The Company is committed to new product development as a means to increase future revenues and to diversify its markets, products, and customers.

Advanced technologies have given the Company a competitive edge over traditional approaches to semiconductors. Combining lithium energy cells with low-power CMOS chips powers chips for the useful life of the equipment. Direct laser writing enhances chip capabilities with high levels of precision and unique identities.

In its 11-year history, Dallas Semiconductor has developed 215 base products with over 1,000 variations shipped to more than 8,000 customers worldwide. A direct sales force and distribution network sell to original equipment manufacturers (OEMs) in personal computers and workstations, scientific and medical equipment, industrial controls, automatic identification, telecommunications, consumer electronics, and other markets.

Sales for 1994 totaled $181,432,000. Dallas Semiconductor has 850 employees. On March 19, 1990, the Company started trading on the New York Stock Exchange under the symbol DS.

TECHNOLOGY

Dallas Semiconductor's special technologies make possible Soft Silicon™ solutions—dynamic, flexible, chip-based products that can be molded in the final manufacturing stages or during use. Soft Silicon is made possible by lithium energy and direct laser writing.

Lithium

Using micro energy management techniques, Dallas Semiconductor has reduced power requirements to the point where a miniature lithium energy source powers products for the useful life of the equipment. Chips and Stiks (snap-in subassemblies) are made virtually crashproof with minimum current design techniques and special freshness seals that keep lithium cells from expending any energy until power is applied for the first time. Through these technologies, Dallas products remember data throughout their operating life and can accept change.

Laser

Direct laser writing makes each chip unique at low cost. A sub-micron positioning laser and control software developed at Dallas can engrave individual chips with digital patterns. This ability to routinely alter, reconfigure, or program individual chips after completion of wafer fabrication broadens the application base of products having similar design. Direct laser writing allows Dallas Semiconductor to develop highly accurate products for applications where precision is paramount.

As a result of these Late Definition technologies, exact chip definition can be left to the OEM. Certain chips can even be defined and redefined by the end system itself.

MANUFACTURING AND FACILITIES

As of January 1, 1995, the Company owns 342,500 square feet of building space and 22.9 acres of land in Dallas. The Company's wafer fabrication facility is a model of efficiency. In order to add capacity for growth the Company built a new advanced wafer fabrication facility that began production in 1994. The new fab is an important asset in terms of its capacity and process capabilities.

QUALITY SYSTEM

Product quality at Dallas Semiconductor results from a combination of design techniques, vendor controls, manufacturing methods, process monitors, and quality control inspections. SPC monitors placed at strategic points ensure that potential defects are detected promptly.

QUALITY CONTROL PROCESSES

- *Incoming Quality Control (IQC):* Piece parts and raw materials are inspected by IQC. New vendors and piece parts receive a First Article Inspection; subsequent incoming materials receive a sample inspection per MIL–STD–105.
- *In–Process Inspections:* Each manufacturing operation inspects its own work, ensuring immediate feedback and preventing deviations from going undetected due to subsequent processing.
- *Statistical Process Control (SPC):* Implemented in manufacturing, this process determines what inputs to the product flow are critical and how to track and control those inputs. Quality Engineering provides training, computer analysis, and feedback to manufacturing.
- *In–Process Sample Tests:* In order to guarantee the accuracy and completeness of in–process inspections and SPC monitors, QC Toll Gates at strategic locations perform sample inspections per MIL–STD–105.

RELIABILITY SYSTEM

Reliability is accomplished through a rigorous, comprehensive methodology of qualifying, analyzing, and monitoring new equipment, processes, products, and packages. A state–of–the–art environmental facility allows accelerated stresses to be performed and monitored in–house. In addition, a metallurgical laboratory has been equipped to perform real-time x–ray, x–ray florescence, and solderability measurements.

To minimize the human influence on the outcome of the reliability activity, a dedicated group of technicians and assistants handle all reliability stressing and testing. Reliability data resides on a customized computer–based tracking and retrieval system. Technical support includes oven and chamber calibrations, 100% electrical board checks, and strict electrostatic protection.

PRODUCT QUALIFICATION

Product qualification activity at Dallas Semiconductor involves a series of accelerated stress tests applied to production–ready material and follows a defined qualification plan. Random samples from at least three production lots, equally representing the production version of the product, are tested to meet reliability requirements. Any device failures detected during production qualification or subsequent monitoring are fully analyzed in our Failure Analysis Laboratory.

Products at Dallas Semiconductor fall into one of three classifications: Prototype or Engineering Sample, Prequal, and Fully Qualified.

- *Prototype or Engineering Sample:* Prototype products have not been fully characterized to all data sheet limits. However, based upon limited data, these products will meet data sheet limits. Final test and all processes used to manufacture the product are under engineering control. Qualification of the product has not started. The brand on prototype products will be PROTO or ES.
- *Prequal:* Prequal products meet prototype requirements and are characterized to all data sheet limits. Final test and all processes used to manufacture the product are stable and under manufacturing control. Qualification of the product has started.
- *Fully Qualified:* Fully qualified products meet prototype and prequal requirements. The qualification requirements given in the next section have been completed. Product must statistically meet reliability failure rates and quality requirements as established by Quality and Reliability Engineering.

Tables 1, 2 and 3 list the tests which a Dallas Semiconductor product must pass in order to be classified as fully qualified.

RELIABILITY MONITOR PROGRAM

In order to maintain continuous qualification status on all products, Dallas Semiconductor has implemented an extensive Reliability Monitor Program (RMP). The RMP monitors all design, wafer fabrication, and assembly processes in the qualified products database. Product is selected monthly from finished goods and subjected to a series of reliability tests similar to those used in the original qualification. Any failures generated from these tests require analysis to root cause and corrective action.

Data from the RMP is published quarterly and is available on demand.

FULL QUALIFICATION REQUIREMENTS FOR INTEGRATED CIRCUIT PRODUCTS Table 1

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Infant Life	125°C, 7.0V	48 Hr.	0.3%
High Temperature Operating Life	125°C, 5.5V	1000 Hr.	*0.4%
Use Condition Prediction	55°C, 5.5V	10 years	50 Fits
High Voltage Life	125°C, 7.0V	1000 Hr.	*0.4%
High Temperature Storage	150°C, No Bias	1000 Hr.	2.0%
Temperature Humidity Bias	85°C/85% RH, 5.5V	1000 Hr.	1.0%
Autoclave	121°C, 2 ATM Steam, Unbiased	168 Hr.	1.5%
Temperature Cycle	–55°C to +125°C	1000 cycle	1.0%
X–Ray	MIL–STD–883 Method 2012		15%
Bond Pull	MIL–STD–883 Method 2011	Premold	1.5%
Dimensions	MIL–STD–883 Method 2016		15%
Lead Integrity	MIL–STD–883 Method 2004		3.0%
Solderability	MIL–STD–883 Method 2003	8 Hr. Steamage	3.0%
ESD	MIL–STD–883 Method 3015		> ±1000 volts
Latch–up	JEDEC Std. 17		> 100 mW/pin

* Combined high voltage life and operating life requirement.

FULL QUALIFICATION REQUIREMENTS FOR MODULE PRODUCTS Table 2

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Use Condition Prediction	55°C, 5.5V	10 years	50 Fits
High Temperature Storage	85°C, No Bias	1000 Hr.	2.0%
*Temperature Humidity Bias	85°C/85% RH, 5.5V	959 Hr.	1.0%
Temperature Cycle	–40°C to +85°C	1000 cycle	1.0%
X–Ray	MIL–STD–883 Method 2012		15%
Dimensions	MIL–STD–883 Method 2016		15%
Lead Integrity	MIL–STD–883 Method 2004		3.0%
Solderability	MIL–STD–883 Method 2003	8 Hr. Steamage	3.0%

* Selected products.

FULL QUALIFICATION REQUIREMENTS FOR SIP STIK AND TOUCH MEMORY PRODUCTS Table 3

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
High Temperature Storage	85°C, No Bias	1000 Hr.	7.0%
Temperature Humidity	60°C/90% RH	288 Hr.	7.0%
Temperature Cycle	–40°C to +85°C	500 cycle	7.0%

NONVOLATILE SRAM

2

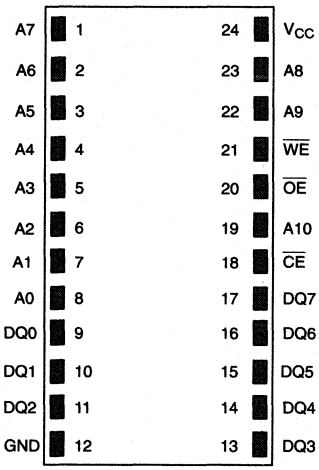
DALLAS SEMICONDUCTOR

DS1220AB/AD
16K Nonvolatile SRAM

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 2K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- JEDEC standard 24–pin DIP package
- Read and write access times as fast as 100 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1220AD)
- Optional ±5% V_{CC} operating range (DS1220AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



24-PIN ENCAPSULATED PACKAGE
720 MIL EXTENDED

PIN DESCRIPTION

A_0-A_{10}	–	Address Inputs
DQ_0-DQ_7	–	Data In/Data Out
$\overline{CE}$	–	Chip Enable
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
V_{CC}	–	Power (+5V)
GND	–	Ground

DESCRIPTION

The DS1220AB and DS1220AD are 16,384-bit, fully static, nonvolatile SRAMs organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent data corruption. The NV SRAMs can be used in place of existing 2K x 8 SRAMs directly conforming to the popular bytewide 24-pin DIP standard. The devices also match the pinout of the 2716 EPROM and the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1220AB and DS1220AD execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 11 address inputs (A_0-A_{10}) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1220AB and DS1220AD execute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1220AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5V. The DS1220AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1220AB and 4.5 volts for the DS1220AD.

FRESHNESS SEAL

Each DS1220 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1220AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1220AD Power Supply Voltage	V_{CC}	4.50	5.0	5.50	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 10% for DS1220AD)
(t_A: See Note 10) (V_{CC}=5V ± 5% for DS1220AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @2.4V	I_{OH}	-1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC}=200ns (Commercial)	I_{CC01}			75	mA	
Operating Current t_{CYC}=200ns (Industrial)	I_{CC01}			85	mA	
Write Protection Voltage (DS1220AB)	V_{TP}	4.5	4.62	4.75	V	
Write Protection Voltage (DS1220AD)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

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AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10% for DS1220AD)
(t_A: See Note 10) (V_{CC}=5.0V ± 5% for DS1220AB)

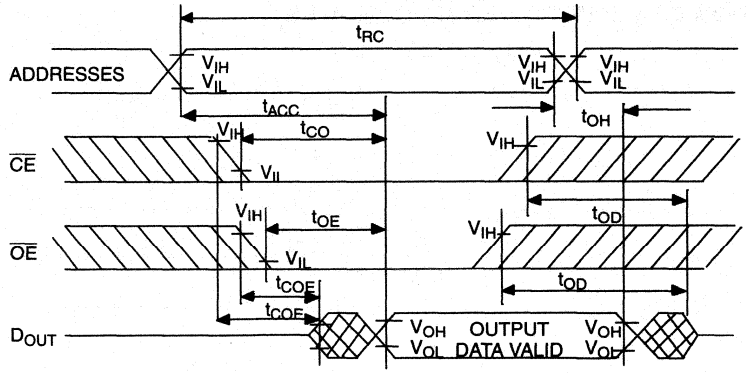
PARAMETER	SYMBOL	DS1220AB–100 DS1220AD–100		DS1220AB–120 DS1220AD–120		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	100		120		ns	
Access Time	t_{ACC}		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		120		ns	
Write Pulse Width	t_{WP}	75		90		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	0 10		0 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	4
Data Setup Time	t_{DS}	40		50		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER	SYMBOL	DS1220AB–150 DS1220AD–150		DS1220AB–200 DS1220AD–200		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		150		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	0 10		0 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	4
Data Setup Time	t_{DS}	60		50		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

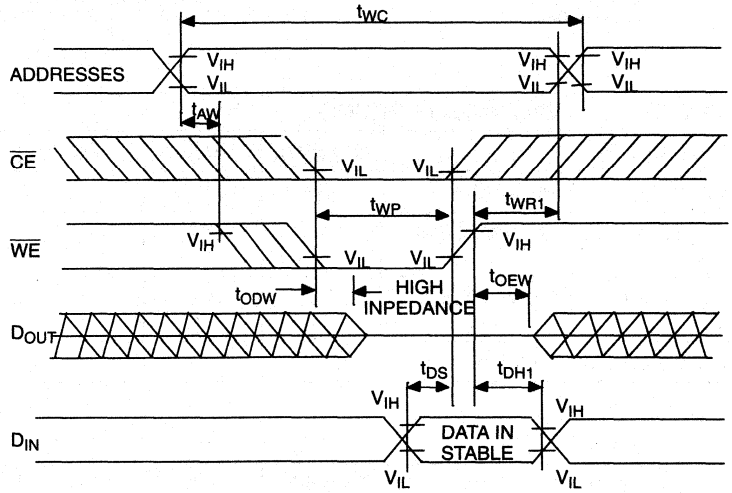
2

READ CYCLE



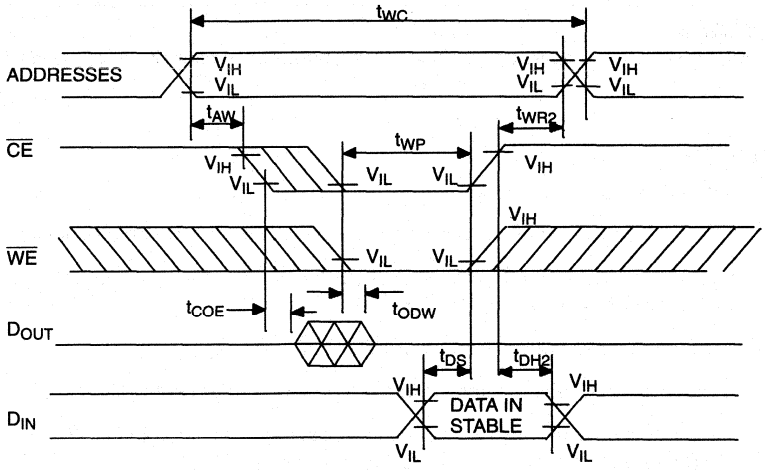
SEE NOTE 1

WRITE CYCLE 1



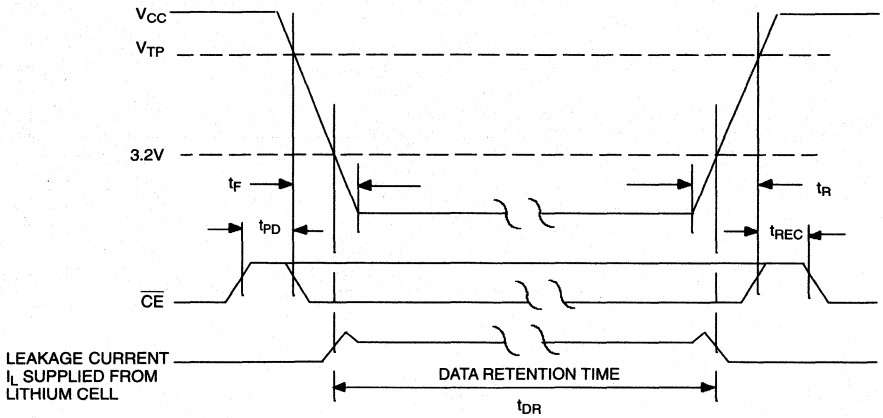
SEE NOTES 2, 3, 4, 6, 7 AND 8

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7 AND 8

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	300			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}	2		125	ms	

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in the battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.

7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1220AB and each DS1220AD has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
14. DS1220AB and DS1220AD modules are recognized by Underwriters Laboratory (U.L.®) under file E99151.

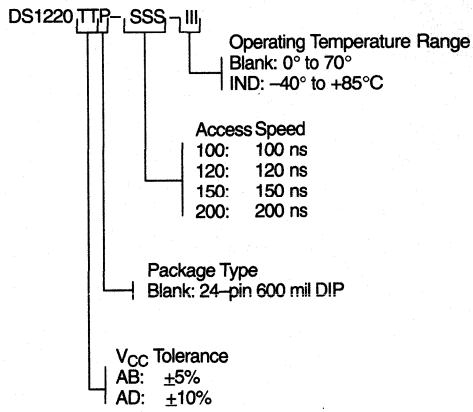
DC TEST CONDITIONS

Outputs Open
All Voltages Are Referenced to Ground

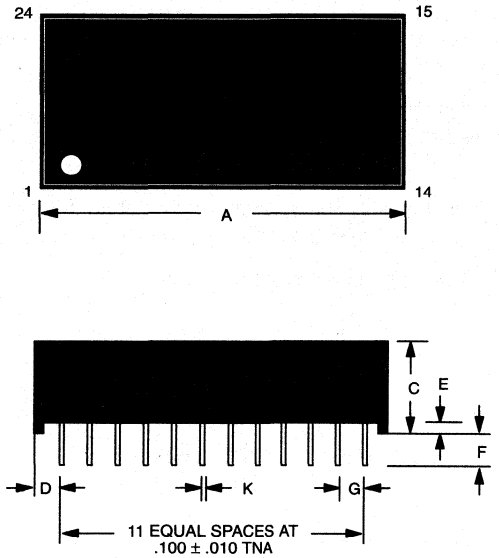
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 – 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

ORDERING INFORMATION



DS1220AB/AD NONVOLATILE SRAM, 24-PIN 720 MIL EXTENDED MODULE



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.320	1.340
MM	33.53	34.04
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.390	0.415
MM	9.91	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DALLAS SEMICONDUCTOR

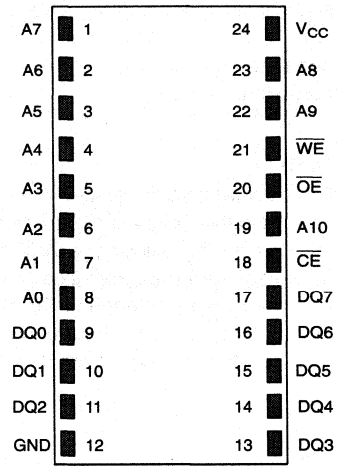
DS1220Y
16K Nonvolatile SRAM

2

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 2K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- JEDEC standard 24–pin DIP package
- Read and write access times as fast as 100 ns
- Full ± 10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



24–PIN ENCAPSULATED PACKAGE
720 MIL EXTENDED

PIN DESCRIPTION

A_0-A_{10}	–	Address Inputs
DQ_0-DQ_7	–	Data In/Data Out
$\overline{CE}$	–	Chip Enable
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
V_{CC}	–	Power (+5V)
GND	–	Ground

DESCRIPTION

The DS1220Y 16K Nonvolatile SRAM is a 16,384-bit, fully static, nonvolatile RAM organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. The NV SRAM can be used in place of existing 2K x 8 SRAMs directly conforming to the popular bytewide 24-pin DIP standard. The DS1220Y also matches the pinout of the 2716 EPROM or the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1220Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 11 address inputs (A_0-A_{10}) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1220Y executes a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1220Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1220Y constantly monitors V_{CC}. Should the supply voltage decay, the NV SRAM automatically write protects itself, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}	V	
Input Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		2.0	4.0	mA	
Operating Current t_{CYC}=200ns (Commercial)	I_{CCO1}			75	mA	
Operating Current t_{CYC}=200ns (Industrial)	I_{CCO1}			85	mA	
Write Protection Voltage	V_{TP}		4.25		V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

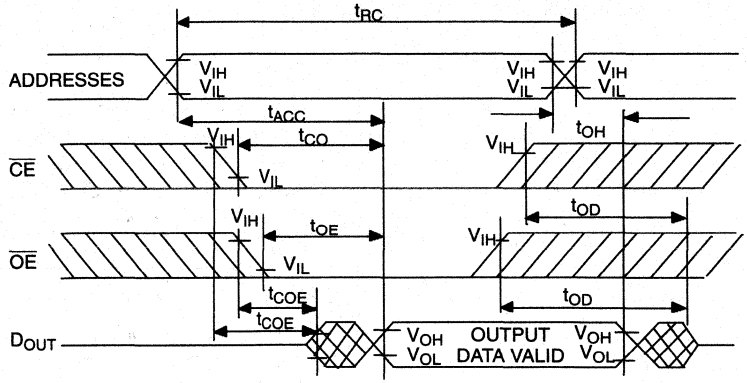
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYM	DS1220Y-100		DS1220Y-120		DS1220Y-150		DS1220Y-200		UNITS	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	100		120		150		200		ns	
Access Time	t_{ACC}		100		120		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		5		ns	
Write Cycle Time	t_{WC}	100		120		150		200		ns	
Write Pulse Width	t_{WP}	75		90		100		150		ns	3
Address Setup Time	t_{AW}	0		0		0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	0 10		0 10		0 10		0 10		ns ns	11 12
Output High Z from $\overline{WE}$	t_{ODW}		35		35		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		5		ns	5
Data Setup Time	t_{DS}	40		50		60		80		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		0 10		0 10		ns ns	11 12

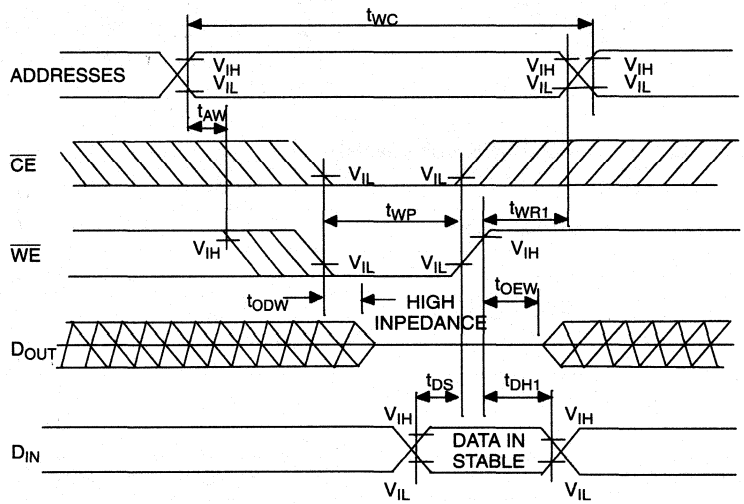
2

READ CYCLE



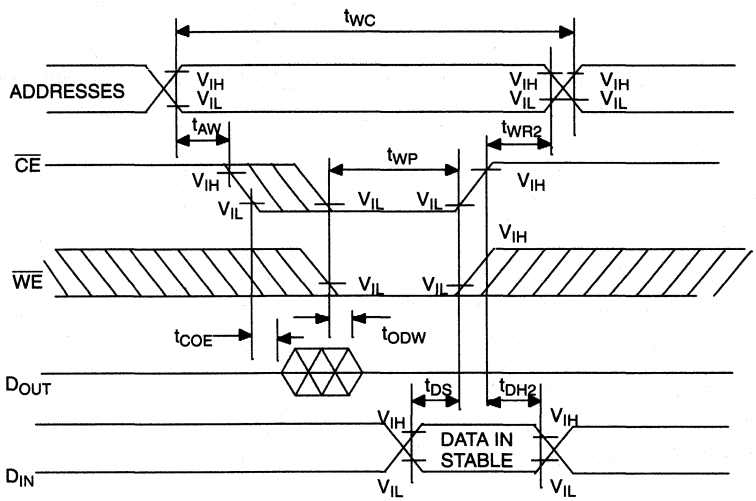
SEE NOTE 1

WRITE CYCLE 1



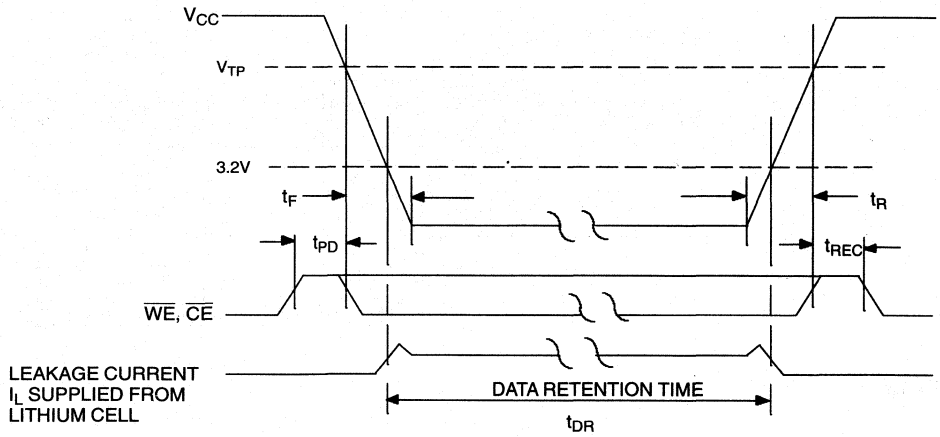
SEE NOTES 2, 3, 4, 6, 7 AND 8

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7 AND 8

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0		µs	10
V_{CC} Slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	100		µs	
V_{CC} Slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	0		µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}		2	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10		years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during a write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state during this period.

7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1220Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. In a power down condition the voltage on any pin may not exceed the voltage of V_{CC}.
11. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
12. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
13. DS1220Y modules are recongnized by Underwriters Laboratory (U.L.®) under file E99151 (R).

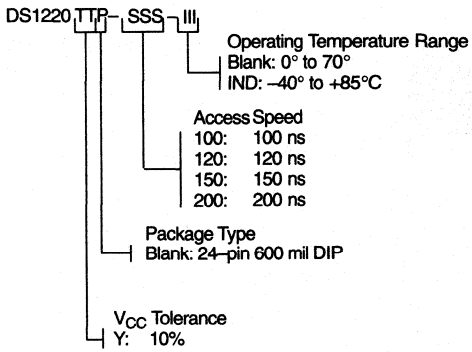
DC TEST CONDITIONS

Outputs open.
All voltages are referenced to ground.

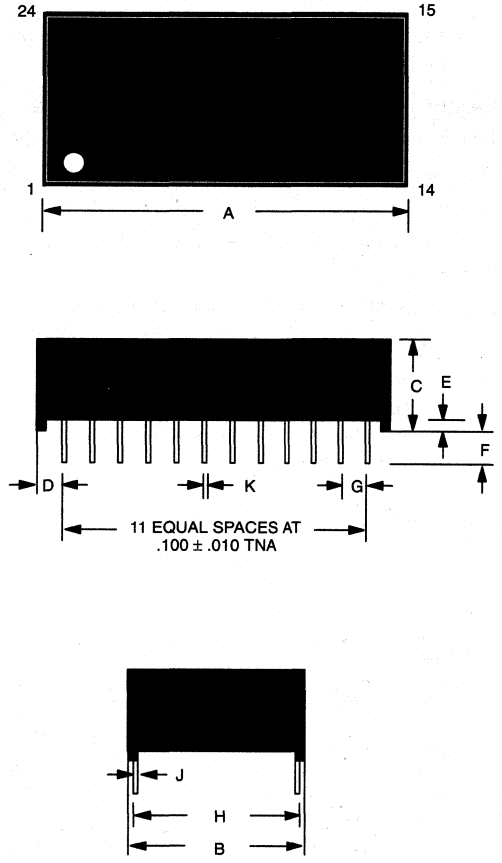
AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input:1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

ORDERING INFORMATION



DS1220Y NONVOLATILE SRAM, 24-PIN 720 MIL EXTENDED MODULE



PKG	24–PIN	
DIM	MIN	MAX
A IN.	1.320	1.340
MM	33.53	34.04
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.390	0.415
MM	9.91	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DALLAS SEMICONDUCTOR

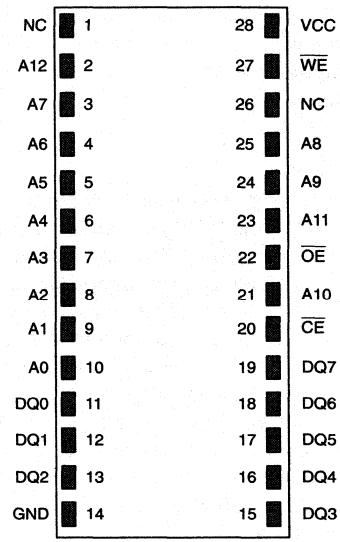
DS1225AB/AD
64K Nonvolatile SRAM

2

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- JEDEC standard 28–pin DIP package
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1225AD)
- Optional ±5% V_{CC} operating range (DS1225AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
720 MIL EXTENDED

PIN DESCRIPTION

A0 - A12	–	Address Inputs
DQ0-DQ7	–	Data In/Data Out
$\overline{CE}$	–	Chip Enable
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
V_{CC}	–	Power (+5V)
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS1225AB and DS1225AD are 65,536-bit, fully static, nonvolatile SRAMs organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent data corruption. The NV SRAMs can be used in place of existing 8K x 8 SRAMs directly conforming to the popular bytewide 28-pin DIP standard. The devices also match the pinout of the 2764 EPROM and the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1225AB and DS1225AD execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 13 address inputs (A_0-A_{12}) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1225AB and DS1225AD execute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1225AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1225AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1225AB and 4.5 volts for the DS1225AD.

FRESHNESS SEAL

Each DS1225 is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1225AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1225AD Power Supply Voltage	V_{CC}	4.50	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 10% for DS1225AD)
(t_A: See Note 10) (V_{CC}=5V ± 5% for DS1225AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE}$>V_{IH} <V_{CC}	I_{IO}	-1.0		+1.0	µA	
Output Current @2.4V	I_{OH}	-1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC}=200ns (Commercial)	I_{CC01}			75	mA	
Operating Current t_{CYC}=200ns (Industrial)	I_{CC01}			85	mA	
Write Protection Voltage (DS1225AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1225AD)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(t_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

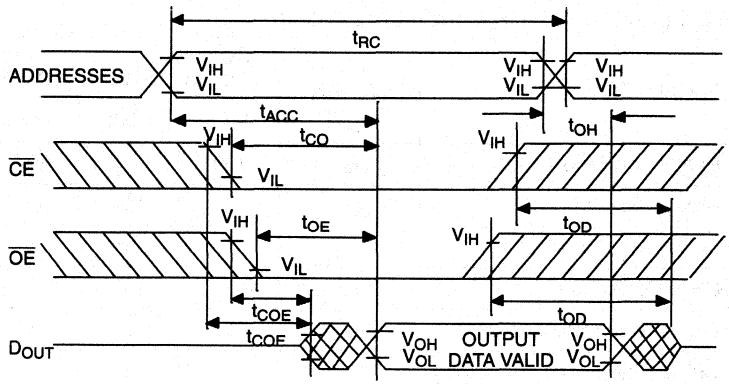
(V_{CC}=5V ± 5% for DS1225AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1225AD)

PARAMETER	SYMBOL	DS1225AB-70 DS1225AD-70		DS1225AB-85 DS1225AD-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		ns	
Access Time	t_{ACC}		70		85	ns	
OE to Output Valid	t_{OE}		35		45	ns	
CE to Output Valid	t_{CO}		70		85	ns	
OE or CE to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		85		ns	
Write Pulse Width	t_{WP}	55		65		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	0 10		0 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		30	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		35		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

AC ELECTRICAL CHARACTERISTICS (cont'd)

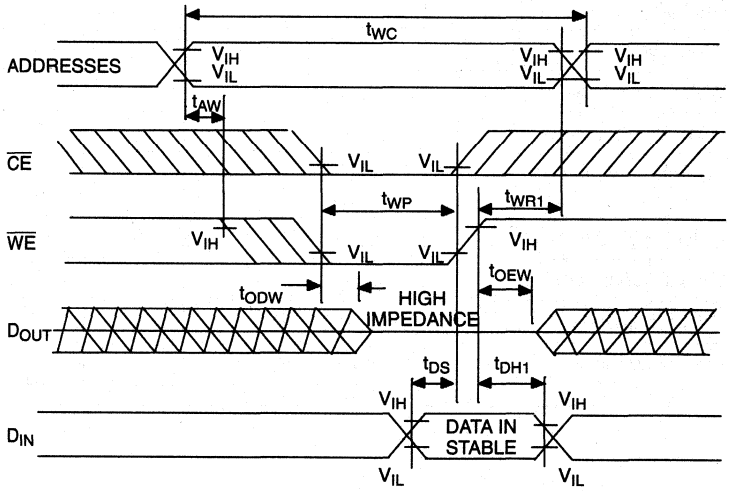
PARAMETER	SYMBOL	DS1225AB-150 DS1225AD-150		DS1225AB-200 DS1225AD-200		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
OE to Output Valid	t_{OE}		70		100	ns	
CE to Output Valid	t_{CO}		150		200	ns	
OE or CE to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		100		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	0 10		0 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	60		80		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

READ CYCLE



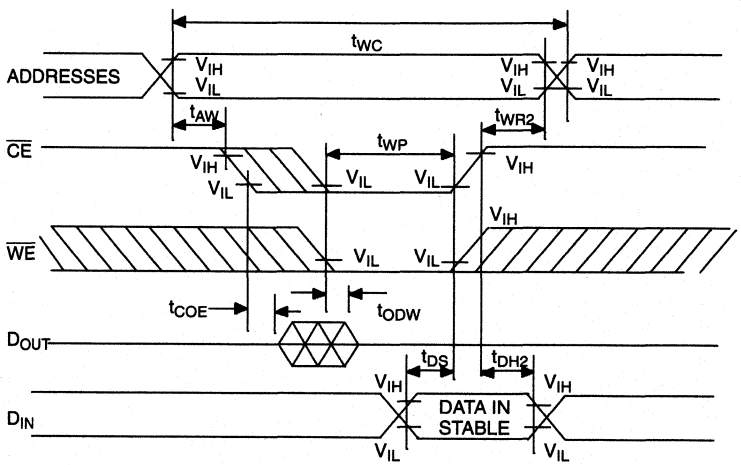
SEE NOTE 1

WRITE CYCLE 1



SEE NOTES 2, 3, 4, 6, 7 AND 8

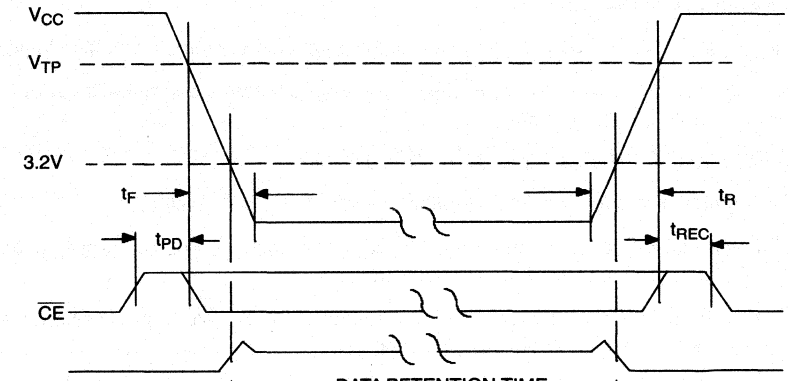
WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7 AND 8

2

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} Slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	300			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}	2		125	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1225AB and each DS1225AD has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
14. DS1225AB and DS1225AD modules are recognized by Underwriters Laboratory (U.L.®) under file E99151.

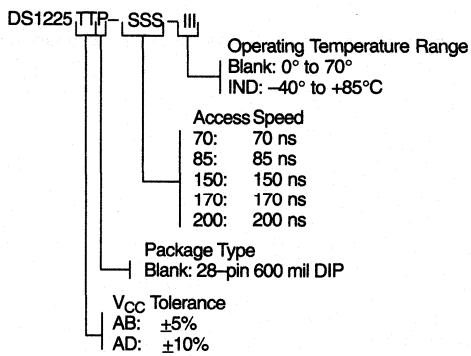
DC TEST CONDITIONS

Outputs Open
All Voltages Are Referenced to Ground

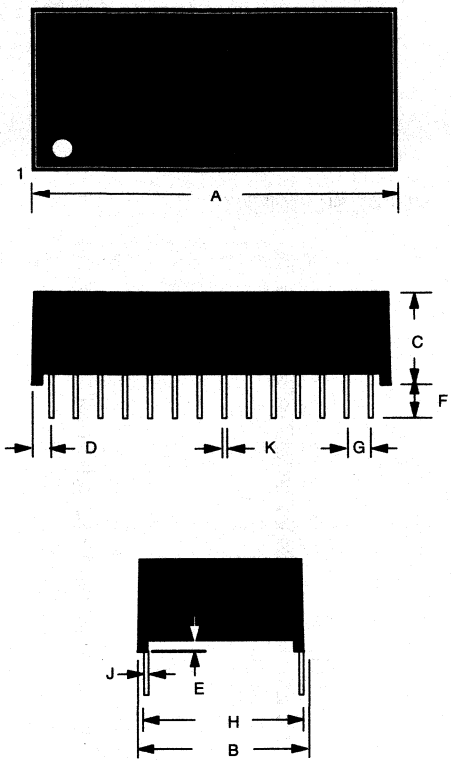
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 – 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

ORDERING INFORMATION



DS1225AB/AD NONVOLATILE SRAM, 28-PIN 720 MIL EXTENDED MODULE



PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

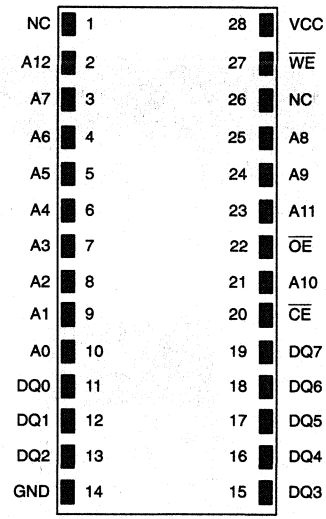
DALLAS SEMICONDUCTOR

DS1225Y
64K Nonvolatile SRAM

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- JEDEC standard 28–pin DIP package
- Read and write access times as fast as 150 ns
- Full ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
720 MIL EXTENDED

PIN DESCRIPTION

A_0 - A_{12}	–	Address Inputs
DQ_0-DQ_7	–	Data In/Data Out
$\overline{CE}$	–	Chip Enable
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
V_{CC}	–	Power (+5V)
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS1225Y 64K Nonvolatile SRAM is a 65,536-bit, fully static, nonvolatile RAM organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. The NV SRAM can be used in place of existing 8K x 8 SRAMs directly conforming to the popular bytewide 28-pin DIP standard. The DS1225Y also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1225Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 13 address inputs (A_0-A_{12}) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1225Y executes a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1225Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1225Y constantly monitors V_{CC}. Should the supply voltage decay, the NV SRAM automatically write protects itself, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}	V	
Input Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5	10	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3	5	mA	
Operating Current t_{CYC}=200ns (Commercial)	I_{CCO1}			75	mA	
Operating Current t_{CYC}=200ns (Industrial)	I_{CCO1}			85	mA	
Write Protection Voltage	V_{TP}		4.25		V	10

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

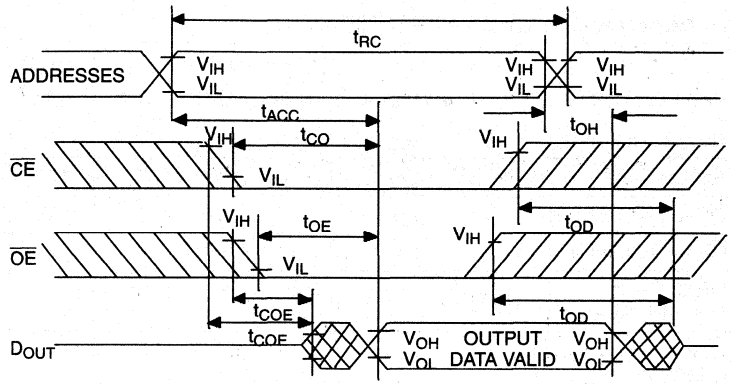
PARAMETER	SYMBOL	DS1225Y-150		DS1225Y-170		DS1225Y-200		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	150		170		200		ns	
Access Time	t_{ACC}		150		170		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		80		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		170		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	150		170		200		ns	
Write Pulse Width	t_{WP}	100		120		150		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	0 10		0 10		0 10		ns ns	11 12
Output High Z from $\overline{WE}$	t_{ODW}		35		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	60		70		80		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		0 10		ns ns	11 12

CAPACITANCE

(t_A = 25°C)

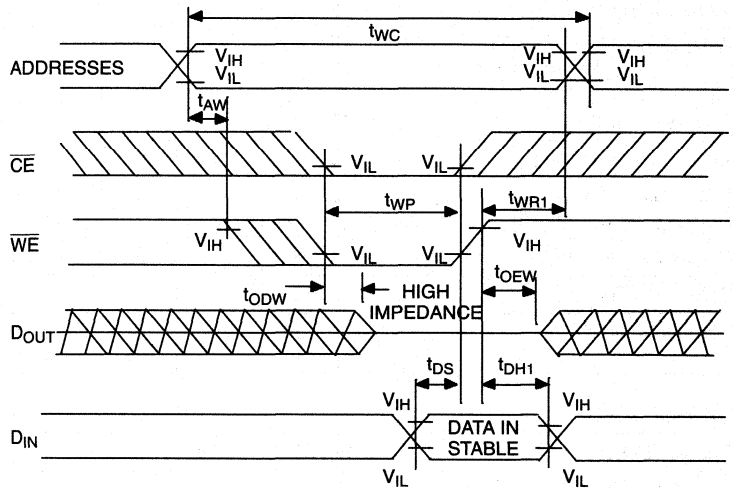
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Input/Output Capacitance	$C_{I/O}$			10	pF	

READ CYCLE



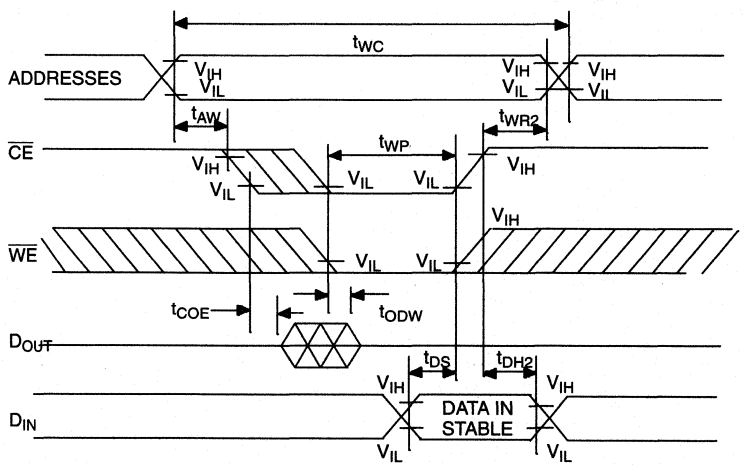
SEE NOTE 1

WRITE CYCLE 1



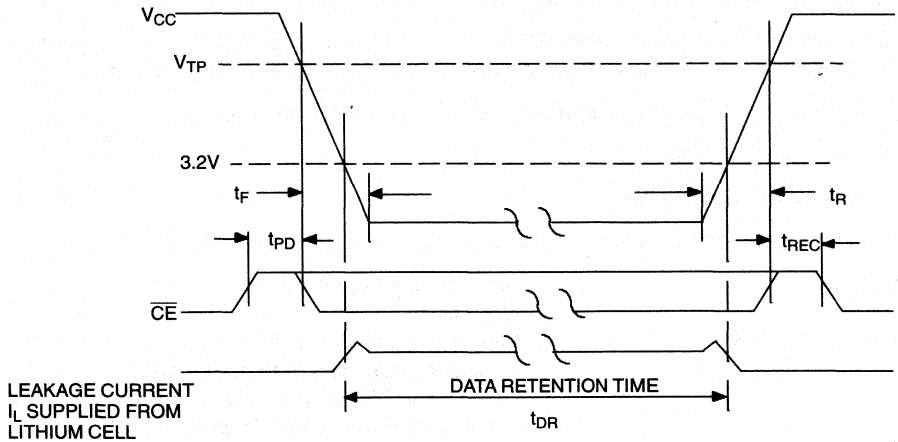
SEE NOTE 2, 3, 4, 6, 7 AND 8

WRITE CYCLE 2



SEE NOTE 2, 3, 4, 6, 7 AND 8

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

PARAMETER	SYM	MIN	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0		µs	10
V_{CC} Slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	100		µs	
V_{CC} Slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	0		µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}		2	ms	

(t_A = 25°C)

PARAMETER	SYM	MIN	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10		years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during a write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.

8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1225Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
11. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
12. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
13. DS1225Y modules are recongnized by Underwriters Laboratory (U.L.®) under file E99151 (R).

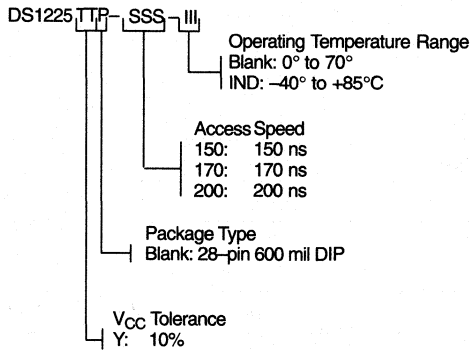
DC TEST CONDITIONS

Outputs open.
All voltages are referenced to ground.

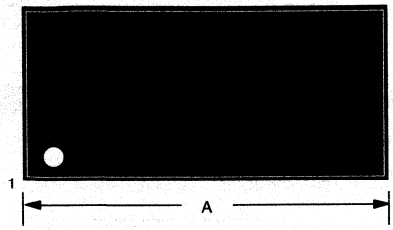
AC TEST CONDITIONS

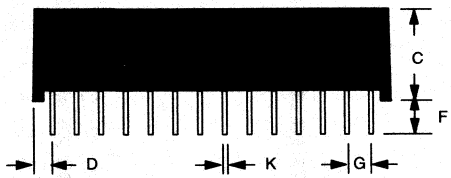
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input:1.5V Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

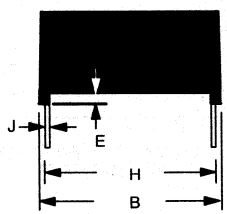
ORDERING INFORMATION



DS1225Y NONVOLATILE SRAM, 28-PIN 720 MIL EXTENDED MODULE







PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DALLAS SEMICONDUCTOR

DS1230Y/AB
256K Nonvolatile SRAM

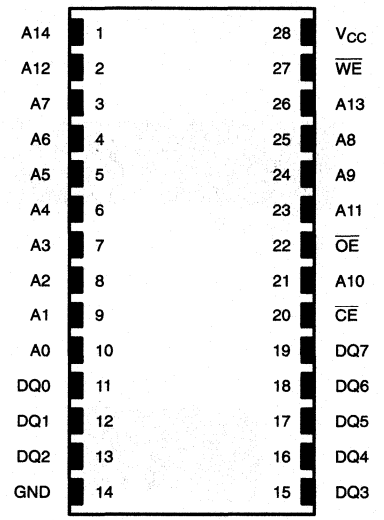
FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- DIP-package devices directly replace 32K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1230Y)
- Optional ±5% V_{CC} operating range (DS1230AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND
- JEDEC standard 28-pin DIP package
- Low Profile Module (LPM) package
  - Fits into standard 68-pin PLCC surface-mountable sockets
  - 250 mil package height

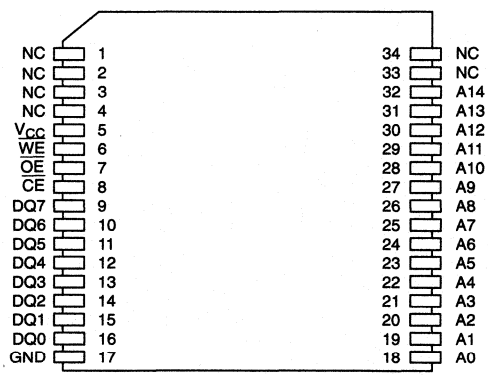
PIN DESCRIPTION

A0 - A14	-	Address Inputs
DQ0 - DQ7	-	Data In/Data Out
$\overline{CE}$	-	Chip Enable
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
V_{CC}	-	Power (+5V)
GND	-	Ground

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED



34–PIN LOW PROFILE MODULE (LPM)

DESCRIPTION

The DS1230 256K Nonvolatile SRAMs are 262,144-bit, fully static, nonvolatile SRAMs organized as 32,768 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. DIP-package DS1230 devices can be used in place of existing 32K x 8 static RAMs directly conforming to the popular bytewide 28-pin DIP standard. The DIP devices also match the pinout of 28256 EEPROMs, allowing direct substitution while enhancing performance. DS1230 devices in the Low Profile Module package are specifically designed for surface-mount applications. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1230 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 15 address inputs (A_0 - A_{14}) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1230 devices execute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1230AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1230Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1230AB and 4.5 volts for the DS1230Y.

FRESHNESS SEAL

Each DS1230 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than 4.25 volts, the lithium energy source is enabled for battery back-up operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C, -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C, -40°C to +85°C for IND parts
Soldering Temperature	260°C For 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1230AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1230Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1230AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1230Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1230AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1230Y)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1230AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1230Y)

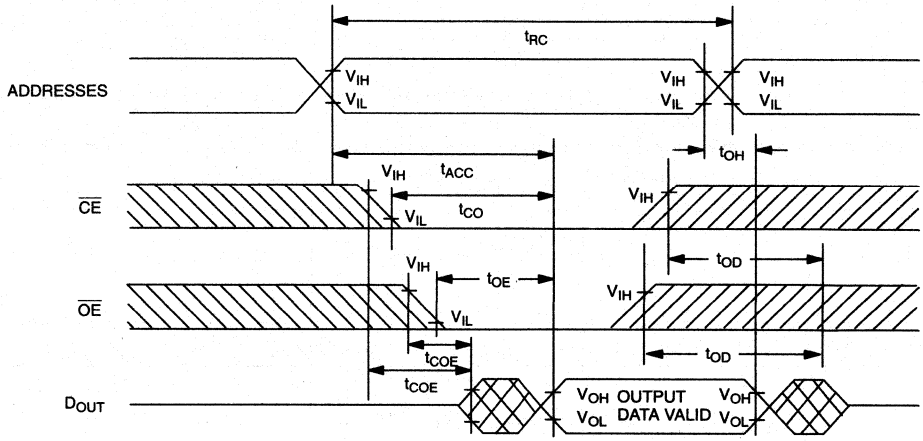
PARAMETER	SYMBOL	DS1230Y-70 DS1230AB-70		DS1230Y-85 DS1230AB-85		DS1230Y-100 DS1230AB-100		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		100		ns	
Access Time	t_{ACC}		70		85		100	ns	
OE to Output Valid	t_{OE}		35		45		50	ns	
CE to Output Valid	t_{CO}		70		85		100	ns	
OE or CE to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	70		85		100		ns	
Write Pulse Width	t_{WP}	55		65		75		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15		5 15		5 15		ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		30		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	30		35		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		0 10		ns	12 13

AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER	SYMBOL	DS1230Y-120 DS1230AB-120		DS1230Y-150 DS1230AB-150		DS1230Y-200 DS1230AB-200		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
OE to Output Valid	t_{OE}		60		70		100	ns	
CE to Output Valid	t_{CO}		120		150		200	ns	
OE or CE to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		100		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15		5 15		5 15		ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		35		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	50		60		80		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		0 10		ns	12 13

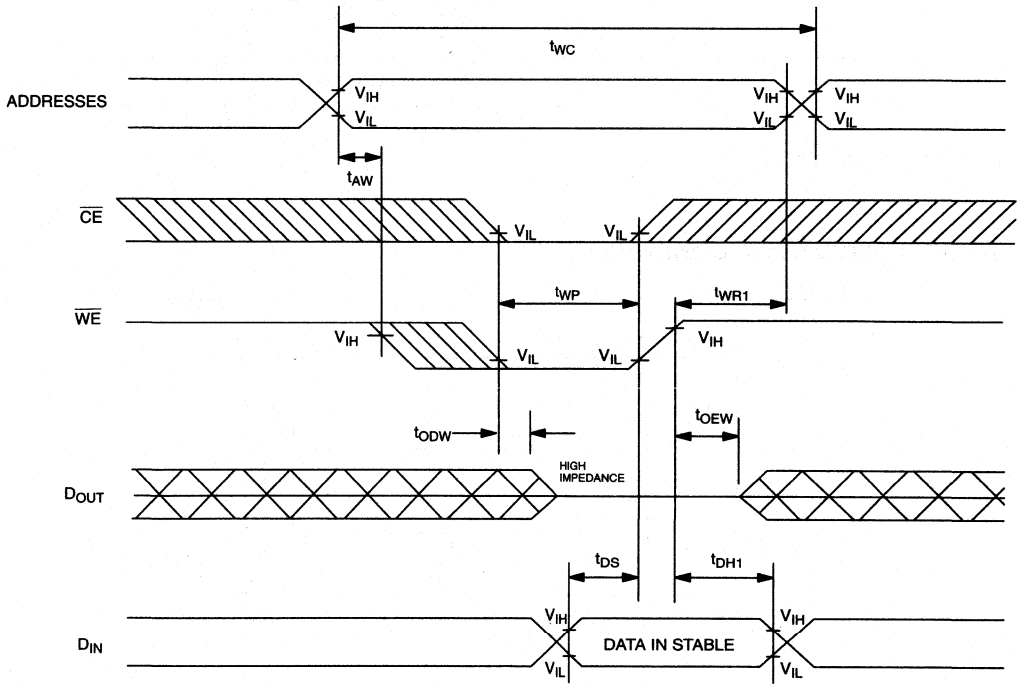
2

READ CYCLE



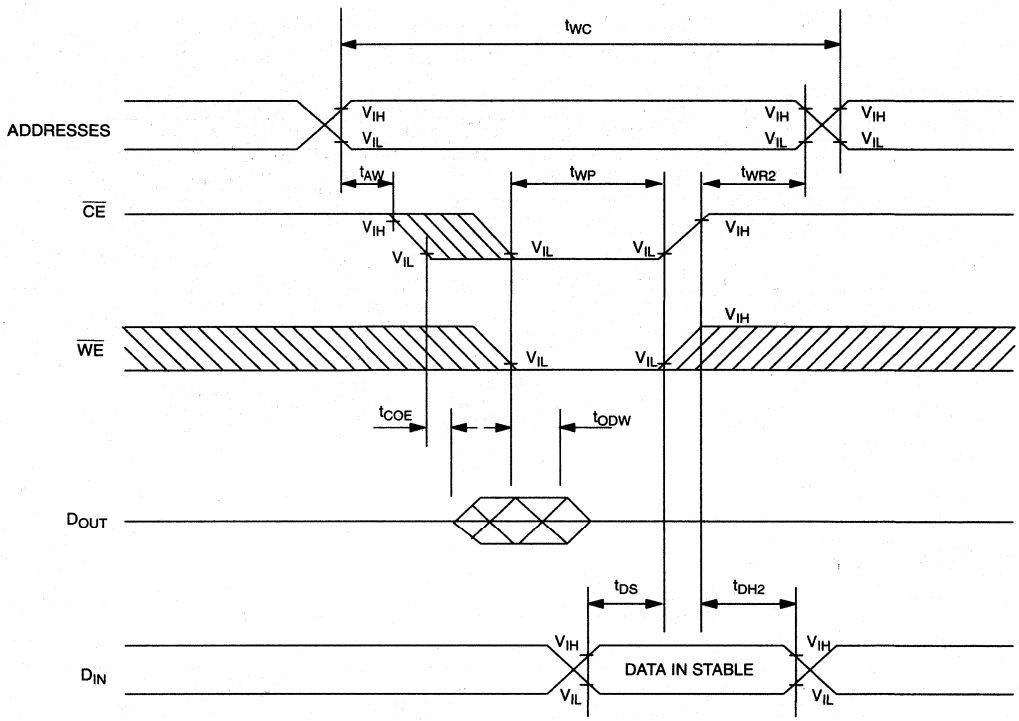
SEE NOTE 1

WRITE CYCLE 1



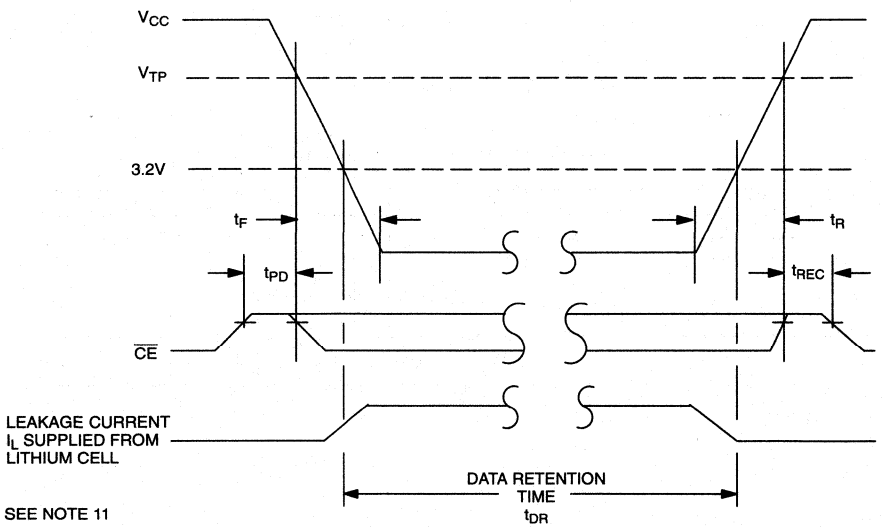
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE, at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	300			µs	
CE, at V_{IH} after Power-Up	t_{REC}	2		125	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1230Y has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1} and t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2} and t_{DH2} are measured from $\overline{CE}$ going high.
14. DS1230 modules are recognized by Underwriters Laboratory (U.L.®) under file E99151.

DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

AC TEST CONDITIONS

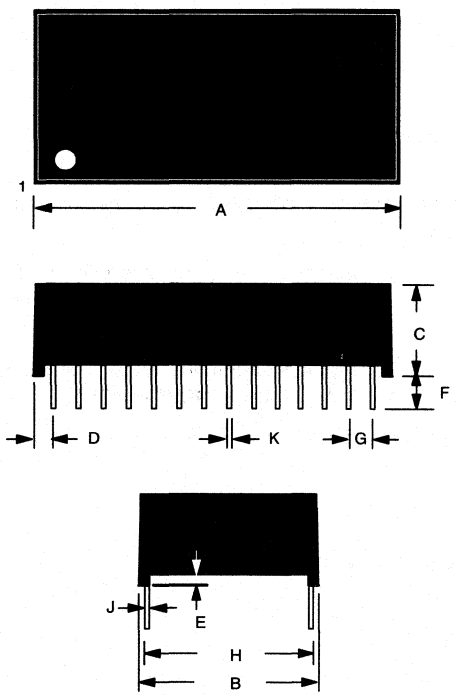
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION

DS1230 T T P – SSS – III

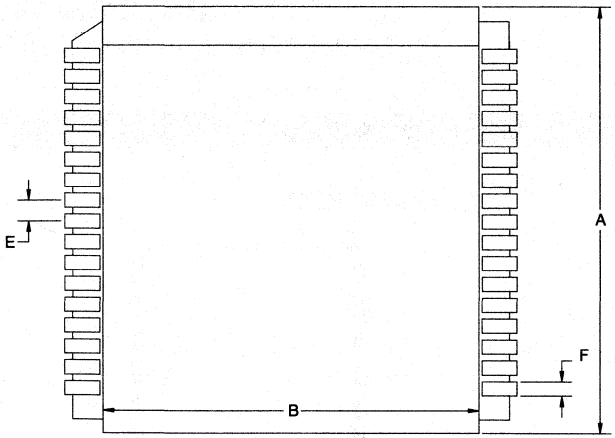
- III: Operating Temperature Range
  - blank: 0° to 70°
  - IND: –40° to 85°C
- SSS: Access Speed
  - 70: 70 ns
  - 85: 85 ns
  - 100: 100 ns
  - 120: 120 ns
  - 150: 150 ns
  - 200: 200 ns
- TTP: Package Type
  - blank: 28–pin 600 mil DIP
  - L: 34–pin Low Profile Module
- T: V_{CC} Tolerance
  - Y: ± 10%
  - AB: ± 5%

DS1230Y/AB NONVOLATILE SRAM, 28–PIN 740 MIL EXTENDED MODULE

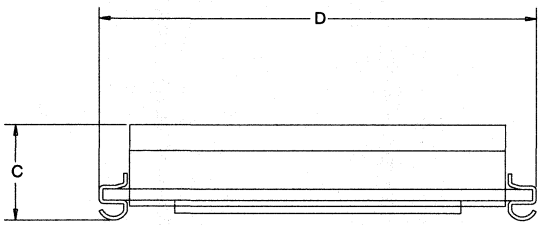


PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.480	1.500
MM	37.60	38.10
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.355	0.375
MM	9.02	9.52
D IN.	0.080	0.110
MM	2.03	2.79
E IN.	0.015	0.025
MM	0.38	0.63
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1230Y/AB 34–PIN LOW PROFILE MODULE (LPM)



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.050 BSC	
F	0.015	0.025



Suggested 68–pin PLCC surface mountable sockets with leads on two sides only are:

McKenzie	34P–SMT–3
Harwin	HIS–40001–04
Robinson Nugent	PLCC–34–SMT
Dallas Semiconductor	DS34PIN–PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.

DALLAS SEMICONDUCTOR

DS1245Y/AB
1024K Nonvolatile SRAM

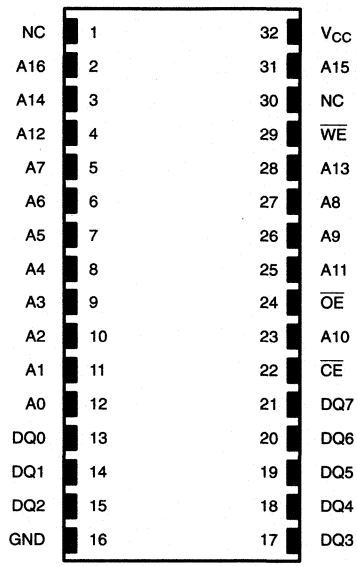
FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- DIP–package devices directly replace 128K x 8 volatile static RAM
- Unlimited write cycles
- Low-power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Full ±10% V_{CC} operating range (DS1245Y)
- Optional ±5% V_{CC} operating range (DS1245AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND
- JEDEC standard 32–pin DIP package
- Low Profile Module (LPM) package
  - Fits into standard 68–pin PLCC surface–mountable sockets
  - 250 mil package height

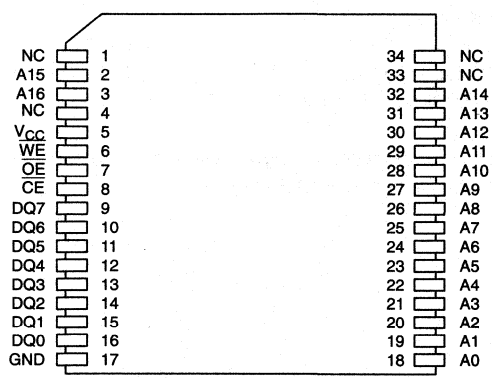
PIN DESCRIPTION

A0 - A16	-	Address Inputs
DQ0 - DQ7	-	Data In/Data Out
$\overline{CE}$	-	Chip Enable
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
V_{CC}	-	Power (+5V)
GND	-	Ground
NC	-	No Connect

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED



34–PIN LOW PROFILE MODULE (LPM)

DESCRIPTION

The DS1245 1024K Nonvolatile SRAMs are 1,048,576-bit, fully static, nonvolatile SRAMs organized as 131,072 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. DIP-package DS1245 devices can be used in place of existing 128K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. DS1245 devices in the Low Profile Module package are specifically designed for surface mount applications. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1245 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 17 address inputs (A_0 - A_{16}) defines which of the 131,072 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1245 devices excute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1245AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1245Y provides full functional capability for V_{CC} greater than 4.5V and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1245AB and 4.5 volts for the DS1245Y.

FRESHNESS SEAL

Each DS1245 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C, –40°C to +85°C for Ind parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for Ind parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1245Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1245AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1245AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1245Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	–1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	–1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	–1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$=2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$=V_{CC}–0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1245Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1245AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

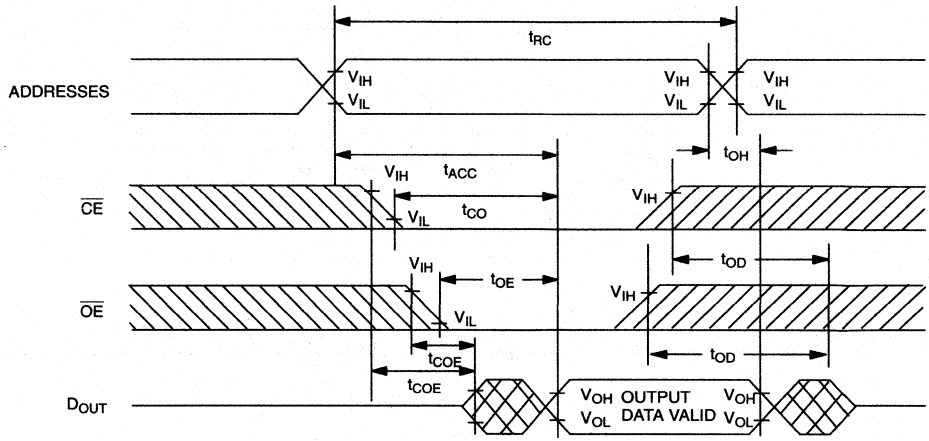
(V_{CC}=5V ± 5% for DS1245AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1245Y)

PARAMETER	SYMBOL	DS1245Y-70 DS1245AB-70		DS1245Y-85 DS1245AB-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		ns	
Access Time	t_{ACC}		70		85	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		45	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		85	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		85		ns	
Write Pulse Width	t_{WP}	55		65		ns	3
Address Setup time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15		5 15		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		30	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		35		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

AC ELECTRICAL CHARACTERISTICS (cont'd)

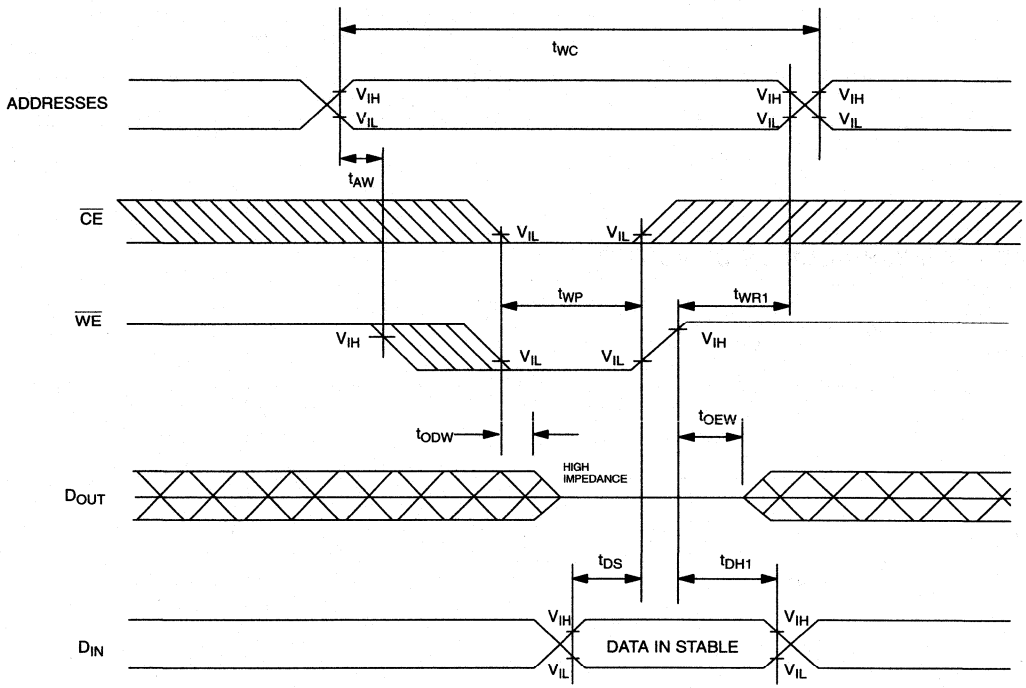
PARAMETER	SYMBOL	DS1245Y-100 DS1245AB-100		DS1245Y-120 DS1245AB-120		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	100		120		ns	
Access Time	t_{ACC}		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		120		ns	
Write Pulse Width	t_{WP}	75		90		ns	3
Address Setup time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15		5 15		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	40		50		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

READ CYCLE



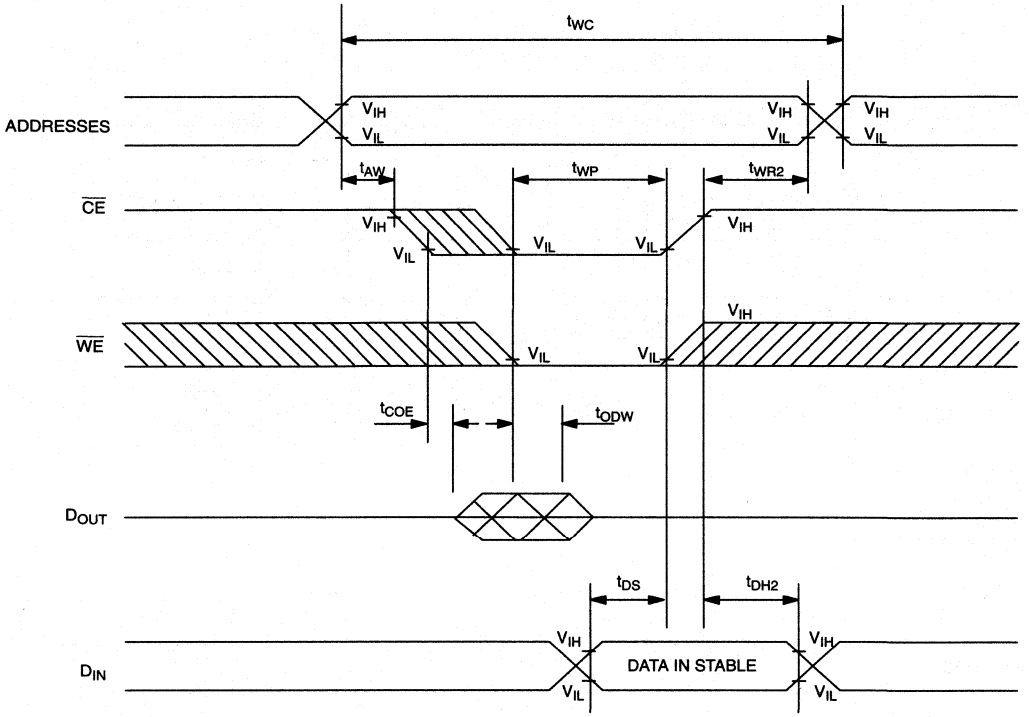
SEE NOTE 1

WRITE CYCLE 1



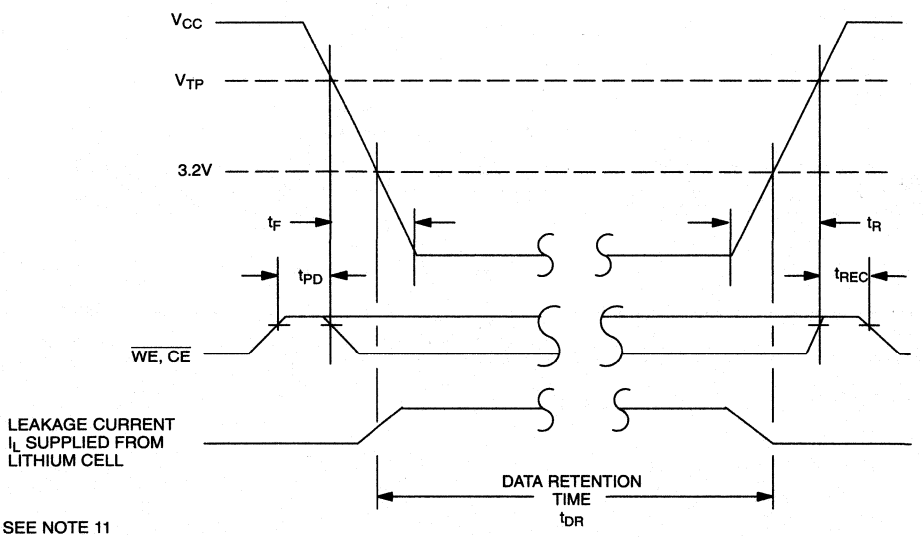
SEE NOTES 2, 3, 4, 6, 7, 8, and 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8, and 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power–Down	t_{PD}	0			µs	11
V_{CC} slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	300			µs	
$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power–Up	t_{REC}	2		125	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1245 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
14. DS1245 modules are recognized by Underwriters Laboratory (U.L.®) under file E99151.

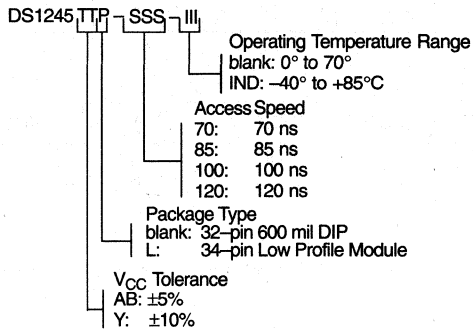
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

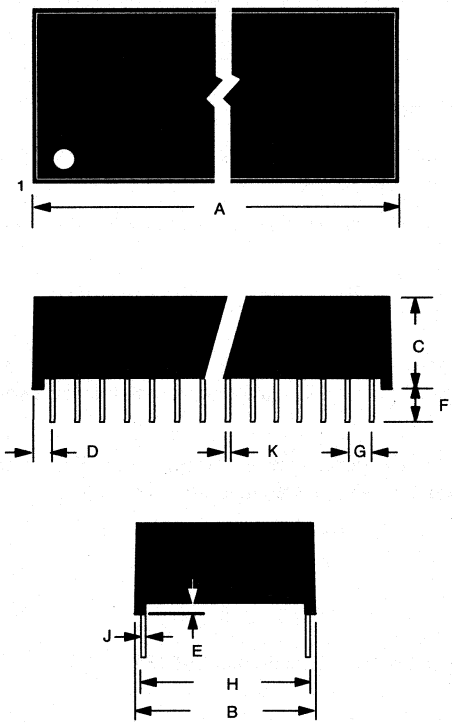
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION

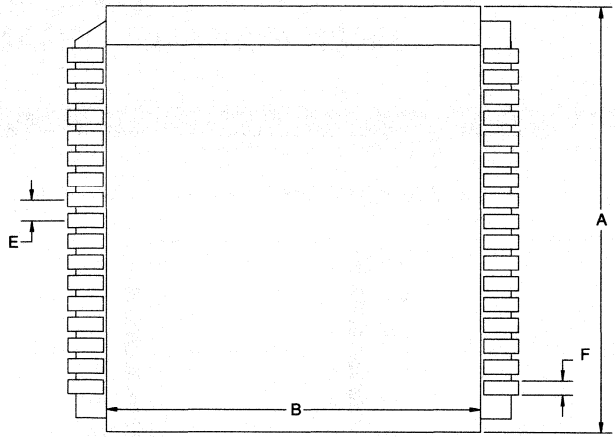


DS1245Y/AB NONVOLATILE SRAM, 32–PIN 740 MIL EXTENDED MODULE

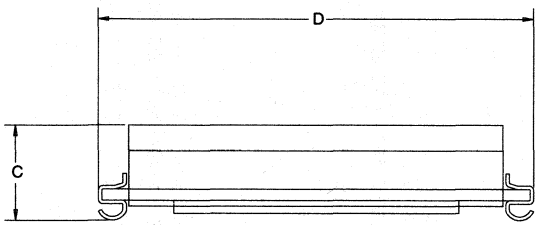


PKG	32-PIN	
DIM	MIN	MAX
A IN.	1.680	1.700
MM	42.67	43.18
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.355	0.375
MM	9.02	9.52
D IN.	0.080	0.110
MM	2.03	2.79
E IN.	0.015	0.025
MM	0.38	0.63
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1245Y/AB 34-PIN LOW PROFILE MOFULE (LPM)



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.050 BSC	
F	0.015	0.025



Suggested 68–pin PLCC surface mountable sockets with leads on two sides only are:

McKenzie	34P–SMT–3
Harwin	HIS–40001–04
Robinson Nugent	PLCC–34–SMT
Dallas Semiconductor	DS34PIN–PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.

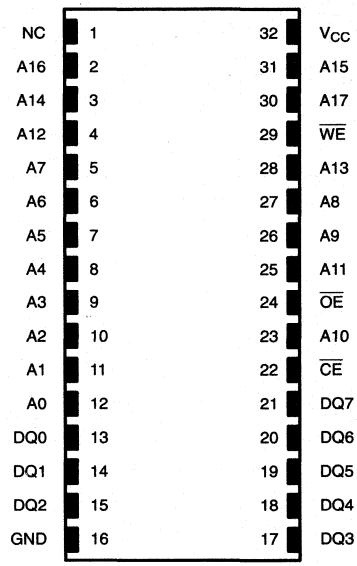
DALLAS SEMICONDUCTOR

DS1249Y
2048K Nonvolatile SRAM

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 256K x 8 volatile static RAM
- Unlimited write cycles
- Low-power CMOS
- JEDEC standard 32–pin DIP package
- Read and write access times as fast as 85 ns
- Full ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



32–PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED, LONG

PIN DESCRIPTION

A0 - A17	–	Address Inputs
DQ0 - DQ7	–	Data In/Data Out
$\overline{CE}$	–	Chip Enable
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
V_{CC}	–	Power (+5V)
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS1249Y 2048K Nonvolatile SRAM is a 2,097,152-bit, fully static, nonvolatile SRAM organized as 262,144 words by 8 bits. The DS1249Y has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. The NV SRAM can be used in place of existing 256K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

READ MODE

The DS1249Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 18 address inputs (A_0 - A_{17}) defines which of the 262,144 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1249Y executes a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1249Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.37 volts nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the NV SRAM automatically write protects itself, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C, –40°C to +85°C for Ind parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for Ind parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	–2.0		+2.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	–2.0		+2.0	µA	
Output Current @ 2.4V	I_{OH}	–1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$=2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$=V_{CC}–0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(t_A = 25°C)

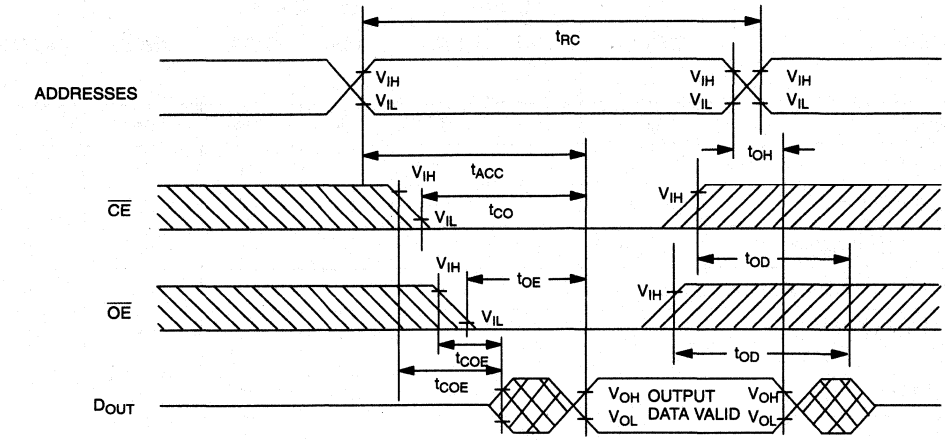
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		10	20	pF	
Input/Output Capacitance	$C_{I/O}$		10	20	pF	

AC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CC}=5V ± 10%)

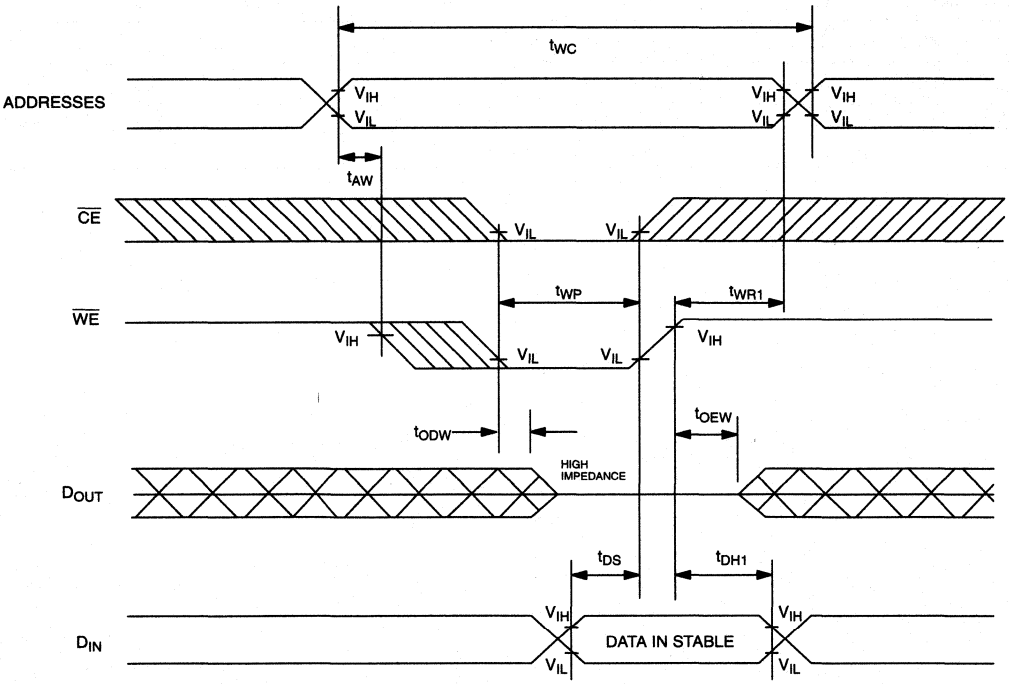
PARAMETER	SYMBOL	DS1249Y-85		DS1249Y-100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	85		100		ns	
Access Time	t_{ACC}		85		100	ns	
$\overline{OE}$ to Output Valid	t_{OE}		45		50	ns	
$\overline{CE}$ to Output Valid	t_{CO}		85		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		30		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	85		100		ns	
Write Pulse Width	t_{WP}	65		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15		5 15		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		30		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	35		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

READ CYCLE



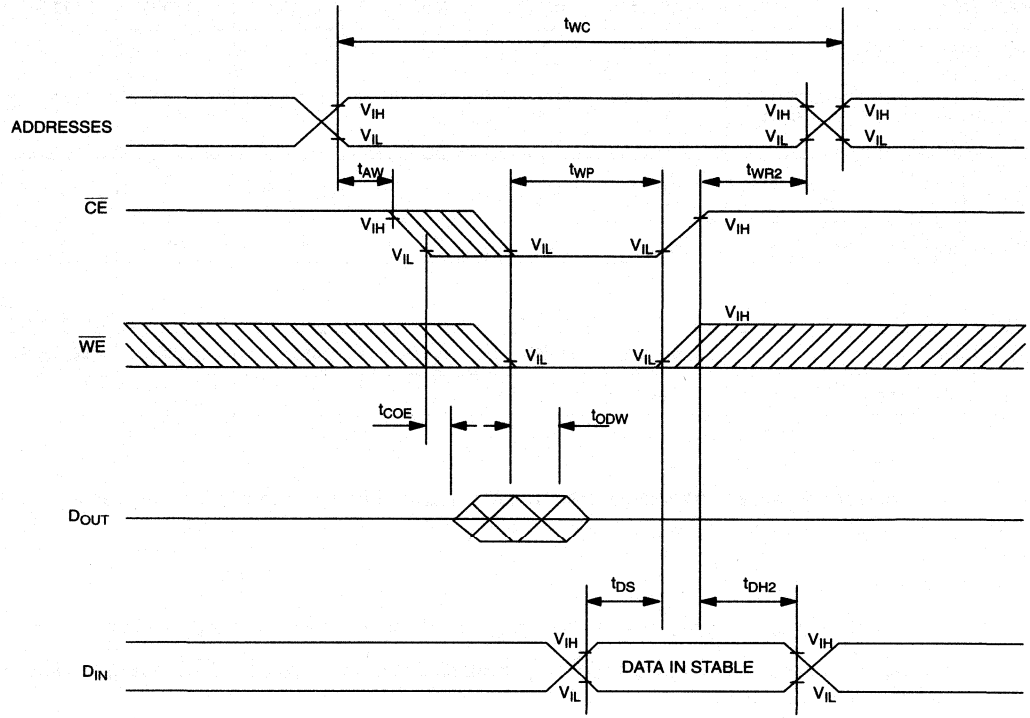
SEE NOTE 1

WRITE CYCLE 1



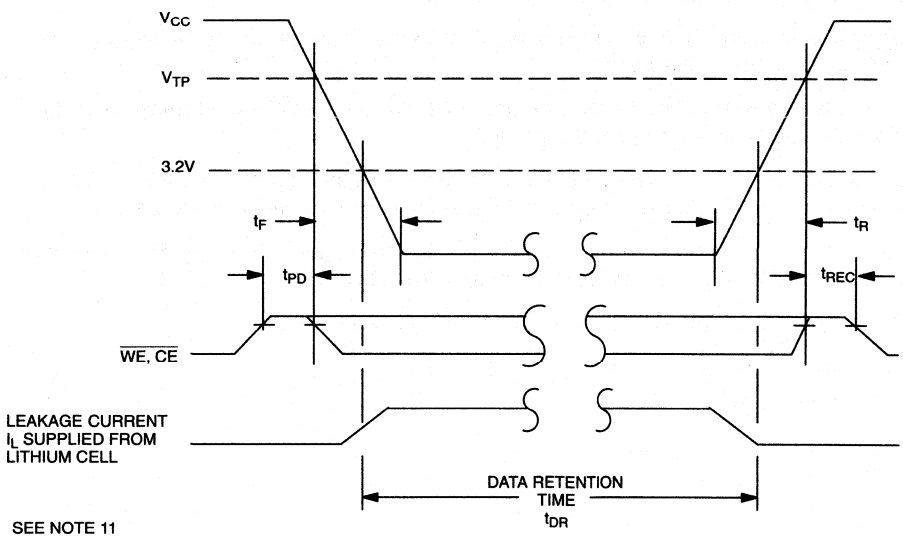
SEE NOTES 2, 3, 4, 6, 7, 8, and 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power–Down	t_{PD}	0			µs	11
V_{CC} slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	300			µs	
$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power–Up	t_{REC}	2		10	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1249Y is marked with a 4–digit date code AABB, AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C for industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.

DC TEST CONDITIONS

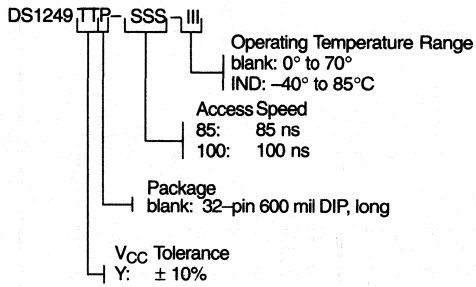
Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

AC TEST CONDITIONS

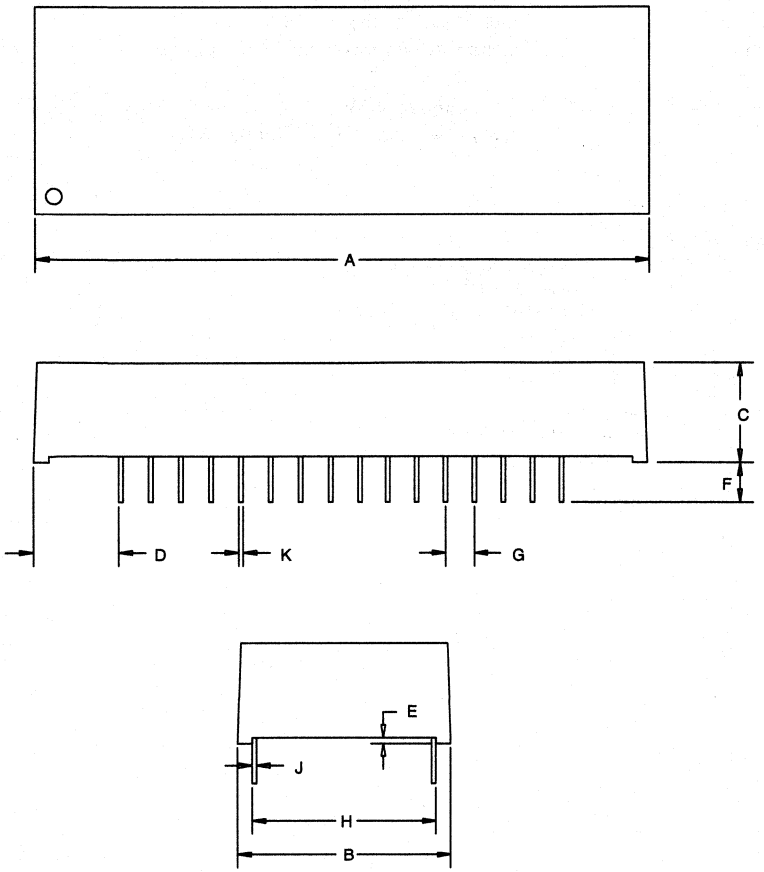
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

2

ORDERING INFORMATION



DS1249Y NONVOLATILE SRAM, 32–PIN 740 MIL EXTENDED LONG MODULE



PKG	32-PIN	
DIM	MIN	MAX
A IN. MM	2.080 52.83	2.100 53.34
B IN. MM	0.715 18.16	0.740 18.80
C IN. MM	0.345 8.76	0.365 9.27
D IN. MM	0.280 7.11	0.310 7.49
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.120 3.05	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.590 14.99	0.630 16.00
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.43	0.025 0.58

DALLAS SEMICONDUCTOR

DS1250Y/AB
4096K Nonvolatile SRAM

2

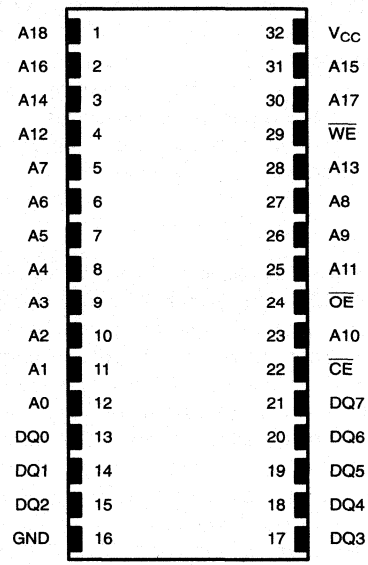
FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 512K x 8 volatile static RAM
- Unlimited write cycles
- Low-power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Full ±10% V_{CC} operating range (DS1250Y)
- Optional ±5% V_{CC} operating range (DS1250AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND
- JEDEC standard 32–pin DIP package
- Low Profile Module (LPM) package
  - Fits into standard 68–pin PLCC surface–mountable sockets
  - 250 mil package height

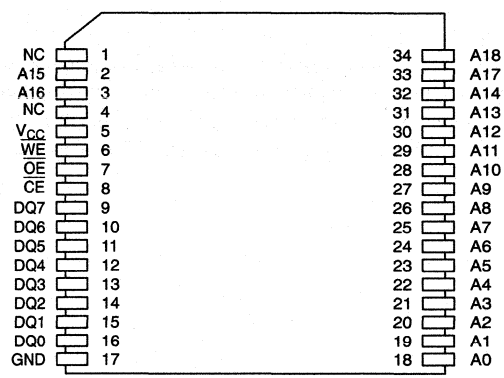
PIN DESCRIPTION

A0 - A18	-	Address Inputs
DQ0 - DQ7	-	Data In/Data Out
$\overline{CE}$	-	Chip Enable
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
V_{CC}	-	Power (+5V)
GND	-	Ground

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED



34–PIN LOW PROFILE MODULE (LPM)

DESCRIPTION

The DS1250 4096K Nonvolatile SRAMs are 4,194,304-bit, fully static, nonvolatile SRAMs organized as 524,288 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. DIP-package DS1250 devices can be used in place of existing 512K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. DS1250 devices in the Low Profile Module package are specifically designed for surface mount applications. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1250 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 17 address inputs (A_0 - A_{16}) defines which of the 131,072 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1250 devices excute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1250AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1250Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1250AB and 4.5 volts for the DS1250Y.

FRESHNESS SEAL

Each DS1250 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C, –40°C to +85°C for Ind parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for Ind parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1250Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1250AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1250AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1250Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	–1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	–1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	–1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$=2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$=V_{CC}–0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1250Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1250AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE

(t_A = 25°C)

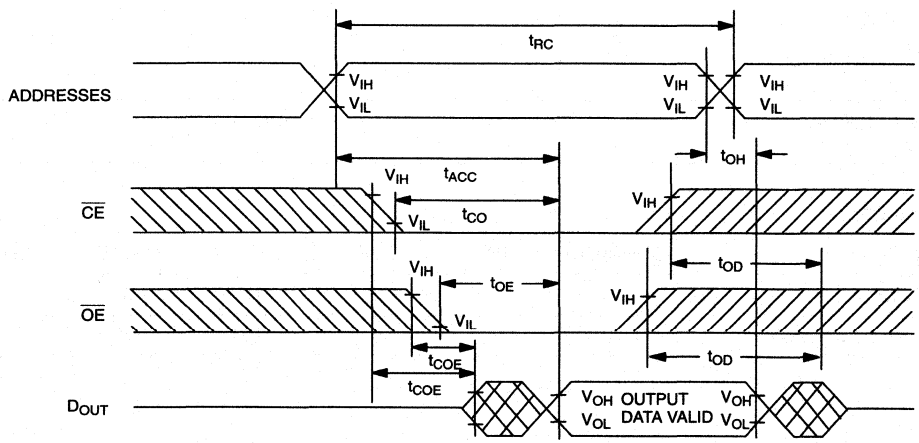
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1250AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1250Y)

PARAMETER	SYMBOL	DS1250Y–70 DS1250AB–70		DS1250Y–100 DS1250AB–100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Access Time	t_{ACC}		70		100	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		50	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		100		ns	
Write Pulse Width	t_{WP}	55		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15		5 15		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

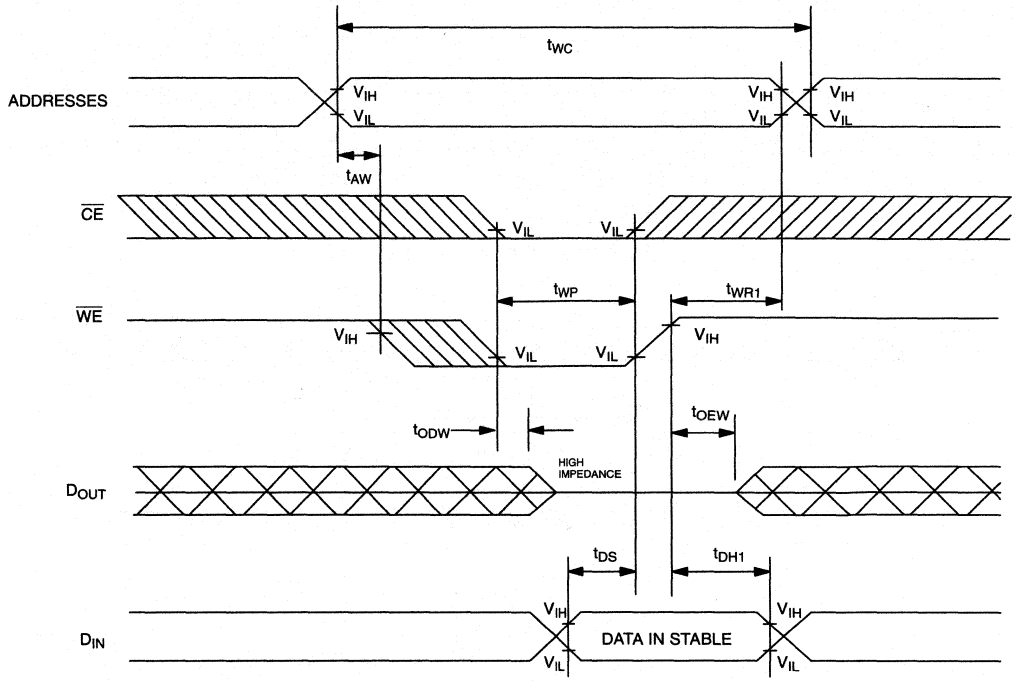
READ CYCLE



SEE NOTE 1

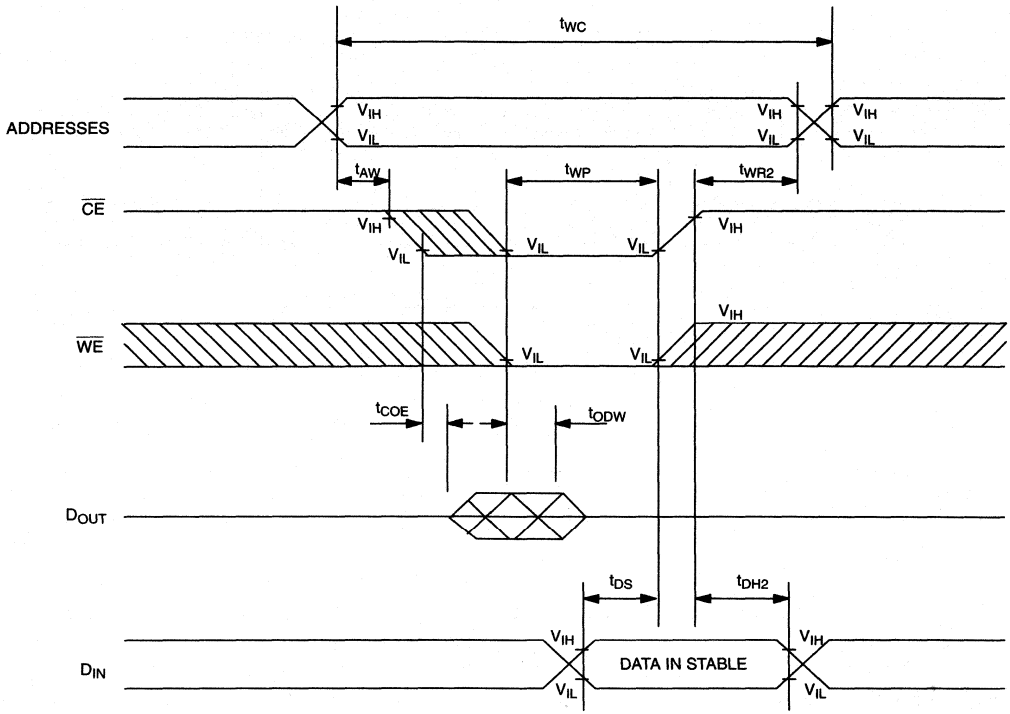
2

WRITE CYCLE 1



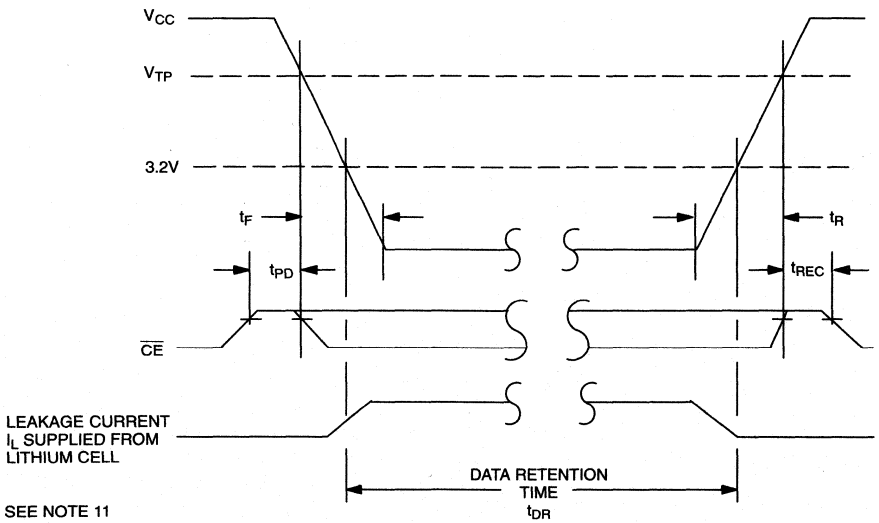
SEE NOTES 2, 3, 4, 6, 7, 8, AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8, AND 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power–Down	t_{PD}	0			µs	11
V_{CC} Slew from V_{TP} to 0V	t_F	300			µs	
V_{CC} Slew from 0V to V_{TP}	t_R	300			µs	
$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power–Up	t_{REC}	2		125	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the later of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1250 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For standard products, this range is 0°C to 70°C. For industrial products (IND), this range is – 40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.

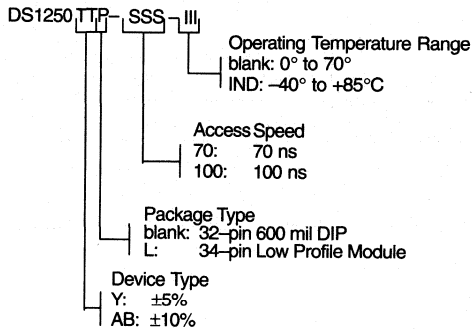
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

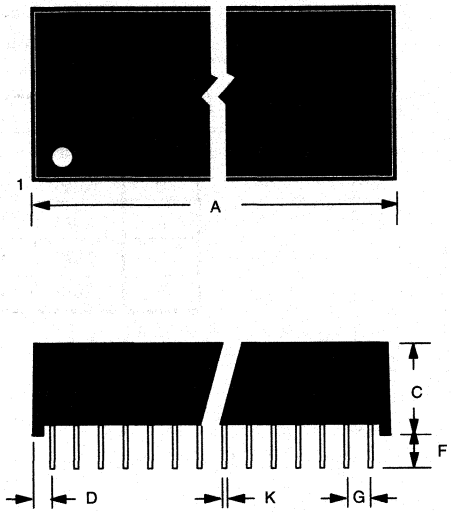
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION

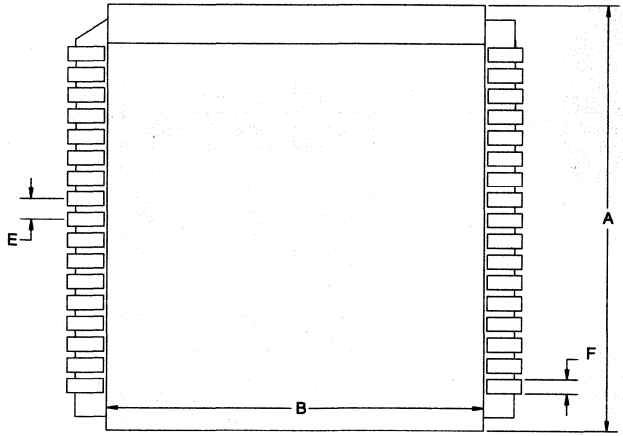


DS1250Y/AB NONVOLATILE SRAM 32–PIN 740 MIL EXTENDED MODULE

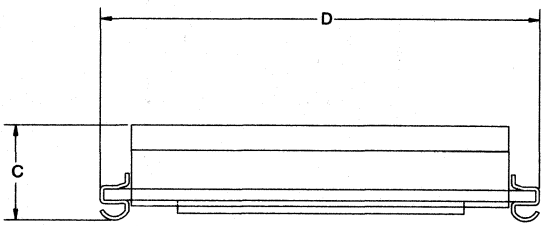


PKG	32-PIN	
DIM	MIN	MAX
A IN.	1.680	1.700
MM	42.67	43.18
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.355	0.375
MM	9.02	9.52
D IN.	0.080	0.110
MM	2.03	2.79
E IN.	0.015	0.025
MM	0.38	0.63
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1250Y/AB 34-PIN LOW PROFILE MODULE (LPM)



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
D	0.047	0.053
F	0.015	0.025



Suggested 68–pin PLCC surface mountable sockets with leads on two sides only are:

McKenzie	34P–SMT–3
Harwin	HIS–40001–04
Robinson Nugent	PLCC–34–SMT
Dallas Semiconductor	DS34PIN–PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.

DALLAS SEMICONDUCTOR

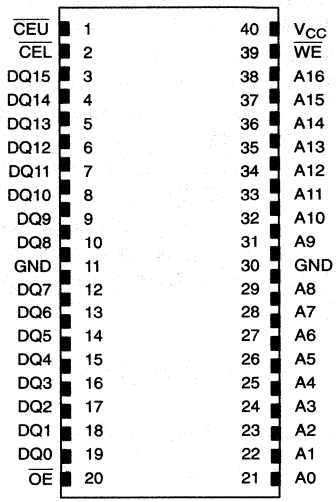
DS1258Y/AB
128K x 16 Nonvolatile SRAM

2

FEATURES

- 10 year minimum data retention in the absence of external power
- Data is automatically protected during a power loss
- Separate upper byte and lower byte chip select inputs
- Unlimited write cycles
- Low–power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% operating range (DS1258Y)
- Optional ±5% operating range (DS1258AB)
- Optional industrial temperature range of –40°C to 85°C, designated IND

PIN ASSIGNMENT



40–PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED

PIN DESCRIPTION

A0–A16	–	Address Inputs
DQ0–DQ15	–	Data In/Data Out
$\overline{CEU}$	–	Chip Enable Upper Byte
$\overline{CEL}$	–	Chip Enable Lower Byte
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
V_{CC}	–	Power Supply (+5V)
GND	–	Ground

DESCRIPTION

The DS1258 128K x 16 Nonvolatile SRAMs are 2,097,152 bit fully static, nonvolatile SRAMs, organized as 131,072 words by 16 bits. Each NV SRAM has a self contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out–of–tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. DIP–package DS1258 devices can be used in place of solutions which build nonvolatile 128K x 16 memory by utilizing a variety of discrete components. There is no limit to the number of write cycles which the DS1658Y/AB can accept, and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1258 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and either/both of $\overline{CEU}$ or $\overline{CEL}$ (Chip Enables) are active (low) and $\overline{OE}$ (Output Enable) is active (low). The unique address specified by the 17 address inputs (A0–A16) defines which of the 131,072 words of data is accessed. The status of $\overline{CEU}$ and $\overline{CEL}$ determines whether all or part of the addressed word is accessed. If $\overline{CEU}$ is active with $\overline{CEL}$ inactive, then only the upper byte of the addressed word is accessed. If $\overline{CEU}$ is inactive with $\overline{CEL}$ active, then only the lower byte of the addressed word is accessed. If both the $\overline{CEU}$ and $\overline{CEL}$ inputs are active (low), then the entire 16 bit word is accessed. Valid data will be available to the 16 data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CEU}$, $\overline{CEL}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$, $\overline{CEU}$, and $\overline{CEL}$ access times are not satisfied, then data access must be measured from the later occuring signal, and the limiting parameter is either t_{CO} for $\overline{CEU}$, $\overline{CEL}$, or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1258 devices execute a write cycle whenever $\overline{WE}$ and either/both of $\overline{CEU}$ or $\overline{CEL}$ are active (low) after address inputs are stable. The unique address specified by the 17 address inputs (A0–A16) defines which of the 131,072 words of data is accessed. The status of $\overline{CEU}$ and $\overline{CEL}$ determines whether all or part of the addressed word is accessed. If $\overline{CEU}$ is active with $\overline{CEL}$ inactive, then only the upper byte of the addressed word is accessed. If $\overline{CEU}$ is inactive with $\overline{CEL}$ active, then only the lower byte of the addressed word is accessed. If both the $\overline{CEU}$ and $\overline{CEL}$ inputs are active (low), then the entire 16–bit word is accessed. The write cycle is terminated by the earlier rising edge of $\overline{CEU}$ and/or $\overline{CEL}$, or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CEU}$ and/or $\overline{CEL}$, and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

READ/WRITE FUNCTION Table 1

$\overline{OE}$	$\overline{WE}$	$\overline{CEL}$	$\overline{CEU}$	V_{CC} CURRENT	DQ0–DQ7	DQ8–DQ15	CYCLE PERFORMED
H	H	X	X	I_{CCO}	High–Z	High–Z	Output Disabled
L	H	L	L	I_{CCO}	Output	Output	Read Cycle
L	H	L	H		Output	High–Z	
L	H	H	L		High–Z	Output	
X	L	L	L	I_{CCO}	Input	Input	Write Cycle
X	L	L	H		Input	High–Z	
X	L	H	L		High–Z	Input	
X	X	H	H	I_{CCS}	High–Z	High–Z	Output Disabled

DATA RETENTION MODE

The DS1258AB provides full functional capability for V_{CC} greater than 4.75 volts, and write protects by 4.5 volts. The DS1258Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1258AB and 4.5 volts for the DS1258Y.

FRESHNESS SEAL

The DS1258 devices are shipped from Dallas Semiconductor with the lithium energy sources disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to +70°C, –40°C to +85°C for IND parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1258Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1258AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1258AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1258Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-2.0		+2.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CEU}$, $\overline{CEL}$=2.2V	I_{CCS1}		10	20	mA	
Standby Current $\overline{CEU}$, $\overline{CEL}$=V_{CC} - 0.5V	I_{CCS2}		6	10	mA	
Operating Current	I_{CCO1}			170	mA	
Write Protection Voltage (DS1258Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1258AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE

(t_A = 25°C)

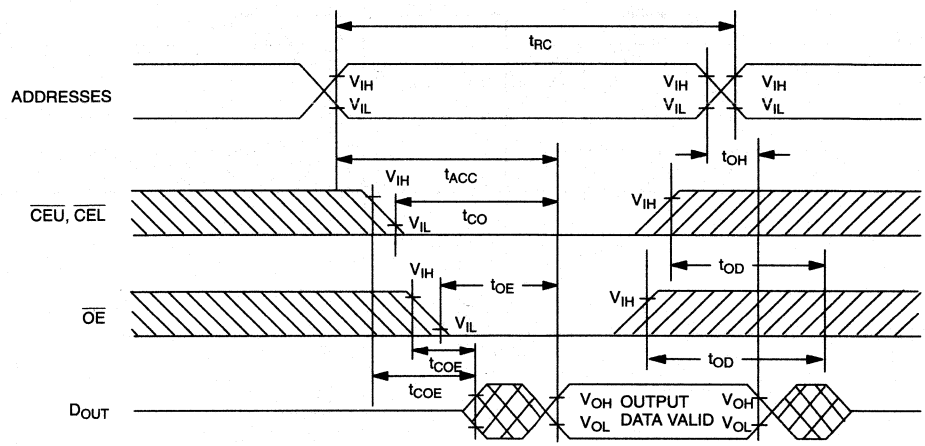
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		20	25	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1258AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1258Y)

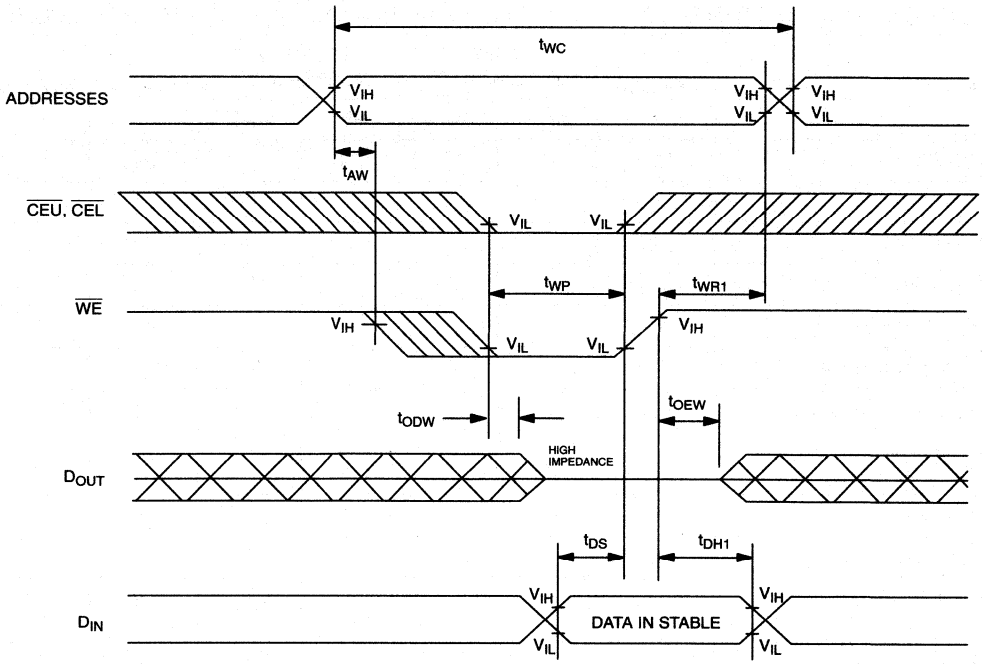
PARAMETER	SYMBOL	DS1258Y–70 DS1258AB–70		DS1258Y–100 DS1258AB–100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Access Time	t_{ACC}		70		100	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		50	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		100		ns	
Write Pulse Width	t_{WP}	55		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15		5 15		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

READ CYCLE



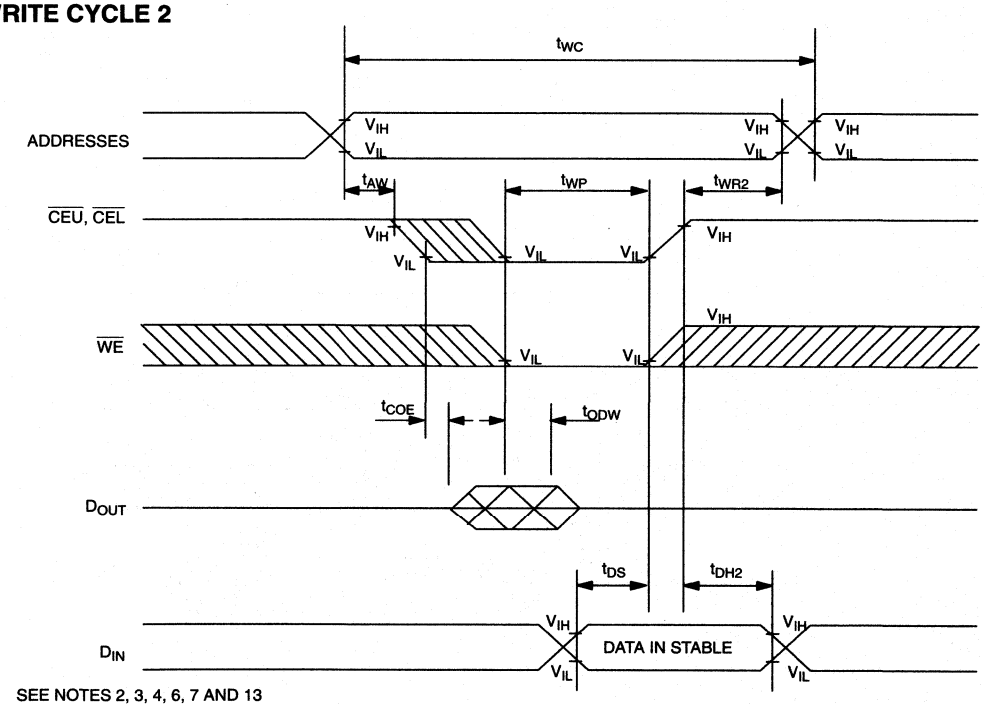
SEE NOTE 1

WRITE CYCLE 1



SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

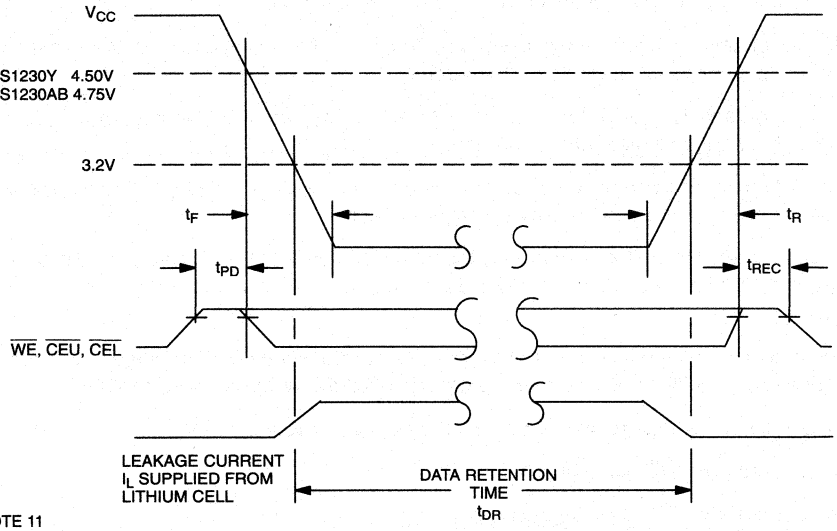
WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7 AND 13

2

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEU}$, $\overline{CEL}$, $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} Slew from V_{TP} to 0V	t_F	300			µs	
V_{CC} Slew from 0V to V_{TP}	t_R	300			µs	
$\overline{CEU}$, $\overline{CEL}$ or at V_{IH} after Power-Up	t_{REC}	2		125	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CEU}$ or $\overline{CEL}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CEU}$, $\overline{CEL}$ or $\overline{WE}$ going low to the earlier of $\overline{CEU}$, $\overline{CEL}$ or $\overline{WE}$ going high.

4. t_{DS} is measured from the earlier of $\overline{CEU}$ or $\overline{CEL}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CEU}$ or $\overline{CEL}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in the output buffers remain in a high impedance state during this period.
7. If the $\overline{CEU}$ or $\overline{CEL}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CEU}$ or $\overline{CEL}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1258 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For standard products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CEU}$ OR $\overline{CEL}$ going high.

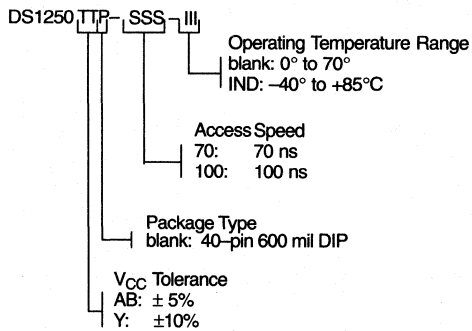
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All voltages are referenced to ground

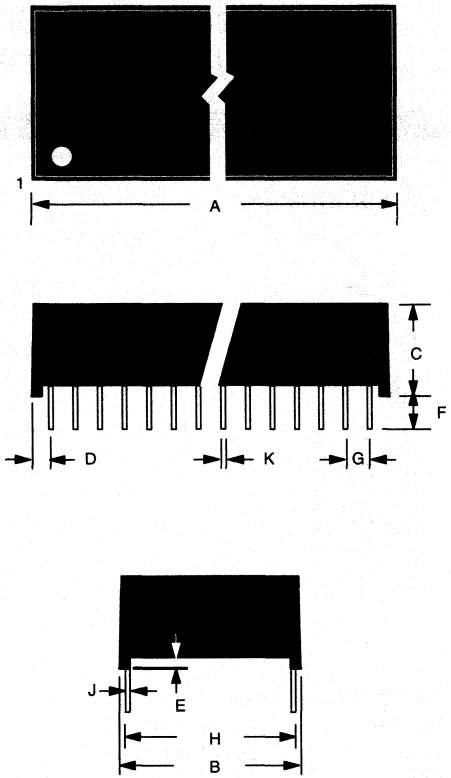
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels:
0.0 to 3.0 volts
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION



DS1258Y/AB NONVOLATILE SRAM 40–PIN 740 MIL EXTENDED MODULE



PKG	40-PIN	
DIM	MIN	MAX
A IN. MM	2.080 52.83	2.100 53.34
B IN. MM	0.715 18.16	0.740 18.80
C IN. MM	0.345 8.76	0.365 9.27
D IN. MM	0.085 2.16	0.115 2.92
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.120 3.05	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.43	0.025 0.58

PRELIMINARY

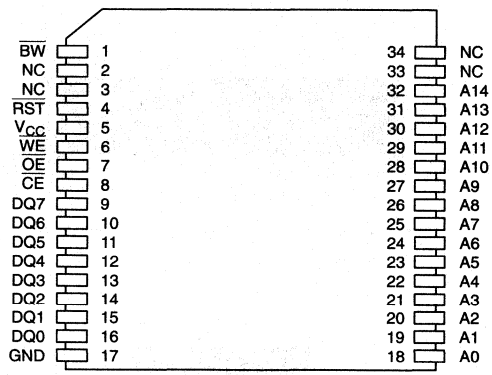
DALLAS SEMICONDUCTOR

DS1330Y/AB
256K Nonvolatile SRAM with Battery Monitor

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Replaces 32K x 8 volatile static RAM or EEPROM
- Monitors system V_{CC}, resets processor when power failure occurs and holds processor in reset during system power–up
- Monitors internal lithium battery and provides advanced warning of impending battery failure
- Unlimited write cycles
- Low–power CMOS operation
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1330Y)
- Optional ±5% V_{CC} operating range (DS1330AB)
- Low Profile Module package fits into standard 68–pin PLCC surface mountable sockets
- Optional industrial temperature range of –40°C to +85°C, designated IND

PIN ASSIGNMENT



34–PIN LOW PROFILE MODULE (LPM)

PIN DESCRIPTION

A0–A14	–	Address Inputs
DQ0–DQ7	–	Data In/Data Out
$\overline{CE}$	–	Chip Enable
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
$\overline{RST}$	–	Reset Output
$\overline{BW}$	–	Battery Warning Output
V_{CC}	–	+5 Volts
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS1330 256K Nonvolatile SRAMs are 262,144–bit, fully static, nonvolatile SRAMs organized as 32,768 words by 8 bits. Each NV SRAM has a self–contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out–of–tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. Additionally, the DS1330 devices have dedicated circuitry for monitoring the status of V_{CC} and the status of the internal lithium battery. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interfacing. The nonvolatile static RAMs can be used in place of 32K x 8 SRAM, EEPROM or Flash devices. DS1330 devices in the Low Profile Module package are specifically designed for surface mount applications.

READ MODE

The DS1330 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 15 address inputs (A_0 - A_{14}) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1330 devices excute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1330AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1330Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data.

During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for DS1330AB and 4.5 volts for the DS1330Y.

SYSTEM POWER MONITORING

DS1330 devices have the ability to monitor the external V_{CC} power supply. When an out–of–tolerance power supply condition is detected, the NV SRAMs warn a processor–based system of impending power failure by asserting $\overline{RST}$. On power up, $\overline{RST}$ is held active for 200 ms nominal to prevent system operation during power–on transients and to allow t_{REC} to expire. $\overline{RST}$ has an open–drain output driver.

BATTERY MONITORING

The DS1330 devices automatically perform periodic battery voltage monitoring on a 24 hour time interval. Such monitoring begins within t_{REC} after V_{CC} rises above V_{TP} and is suspended when power failure occurs.

After each 24 hour period has elapsed, the battery is connected to an internal 1MΩ test resistor for one second. During this one second, if battery voltage falls below the battery voltage trip point V_{BTP}, the battery warning output $\overline{BW}$ is asserted. Once asserted, $\overline{BW}$ remains active until the module is replaced. The battery is still retested after each V_{CC} power–up, however, even if $\overline{BW}$ is active. If the battery voltage is found to be higher than V_{BTP} during such testing, $\overline{BW}$ is de–asserted and regular 24–hour testing resumed. $\overline{BW}$ has an open–drain output driver.

FRESHNESS SEAL AND SHIPPING

Each DS1330 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C, -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C, -40°C to +85°C for IND parts
Soldering Temperature	260°C For 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1330AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1330Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1330AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1330Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	14
Output Current @ 0.4V	I_{OL}	2.0			mA	14
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		300	600	µA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		100	150	µA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1330AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1330Y)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

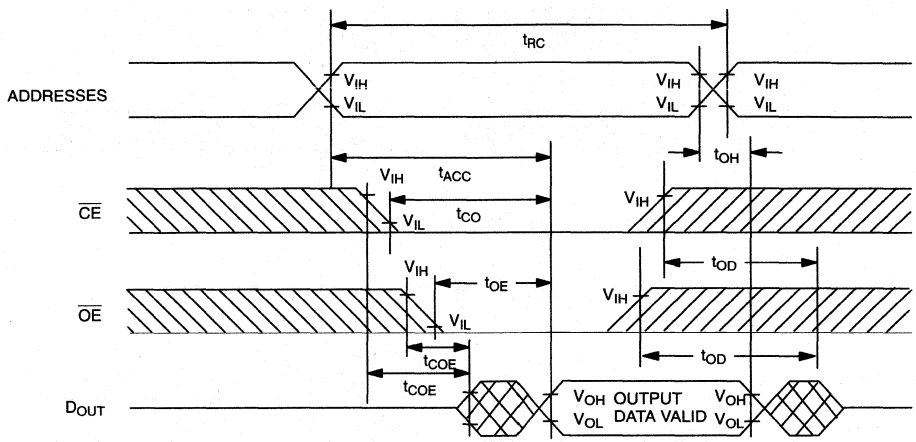
2

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1330AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1330Y)

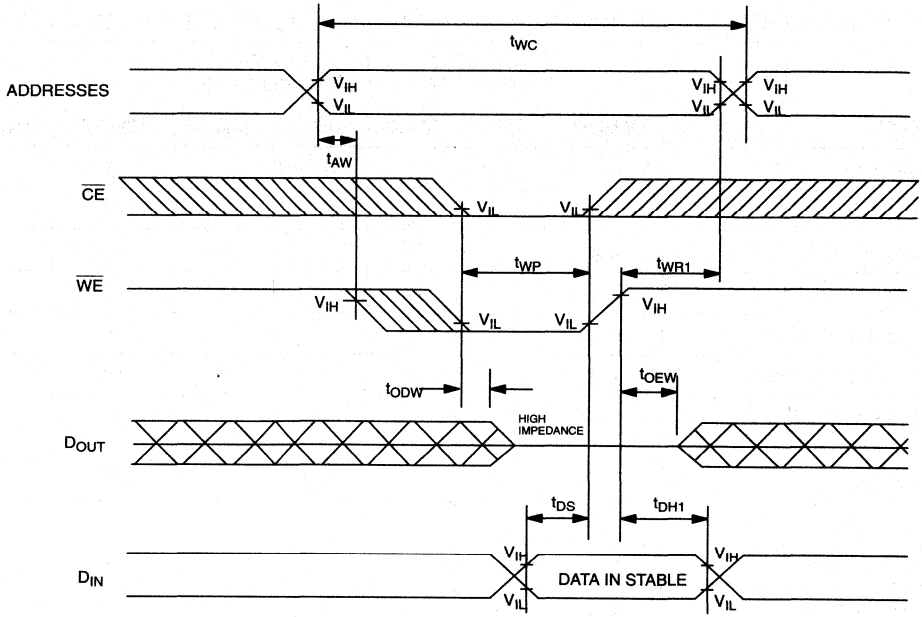
PARAMETER	SYMBOL	DS1330Y–70 DS1330AB–70		DS1330Y–100 DS1330AB–100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Access Time	t_{ACC}		70		100	ns	
OE to Output Valid	t_{OE}		35		50	ns	
CE to Output Valid	t_{CO}		70		100	ns	
OE or CE to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		100		ns	
Write Pulse Width	t_{WP}	55		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 10		5 10		ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 5		0 5		ns	12 13

READ CYCLE



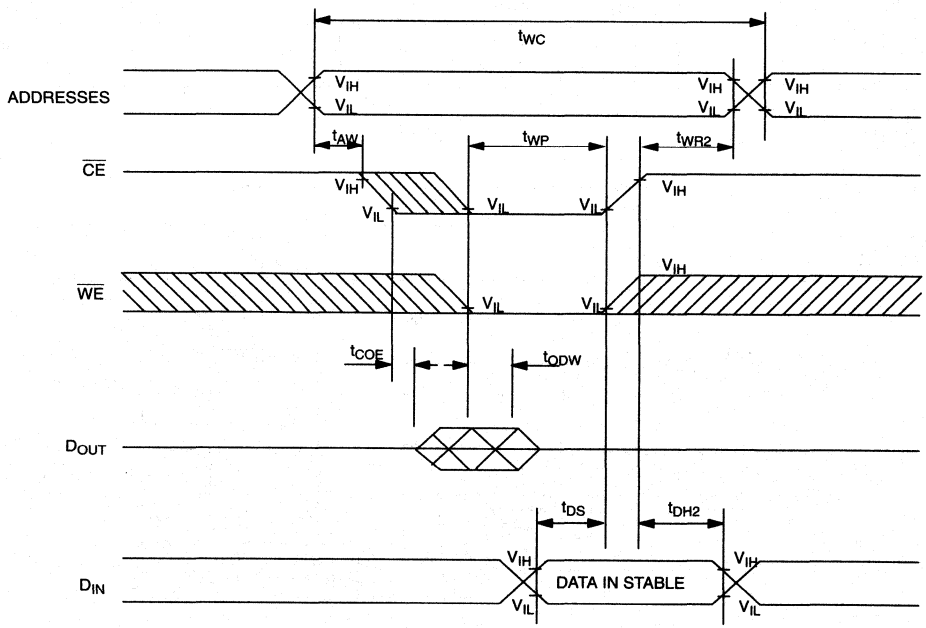
SEE NOTE 1

WRITE CYCLE 1



SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

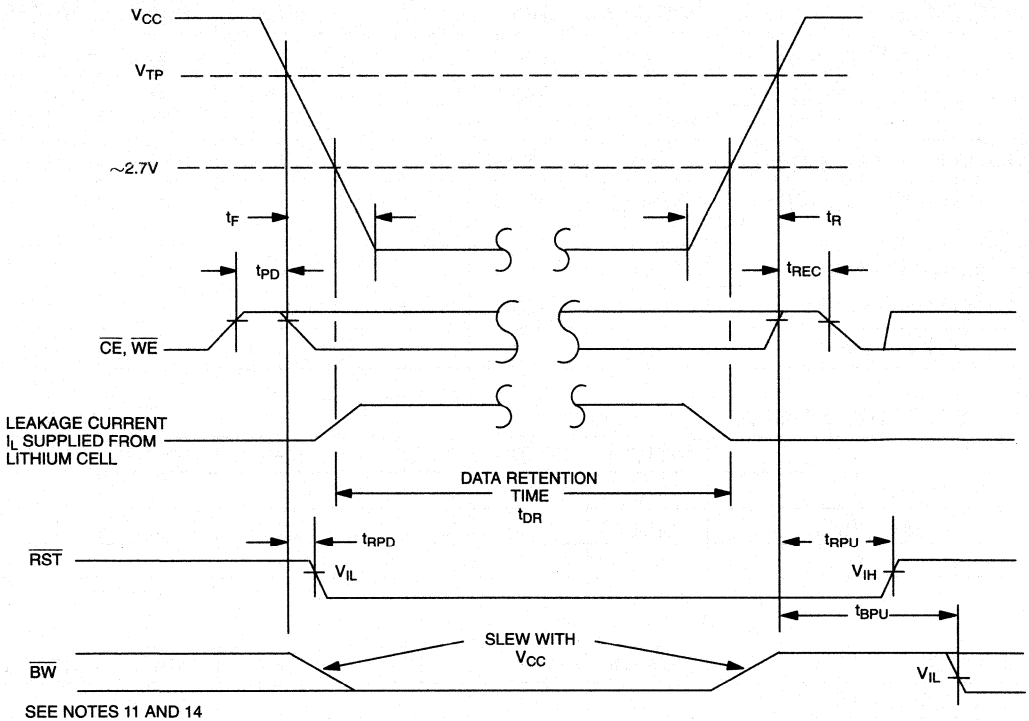
WRITE CYCLE 2



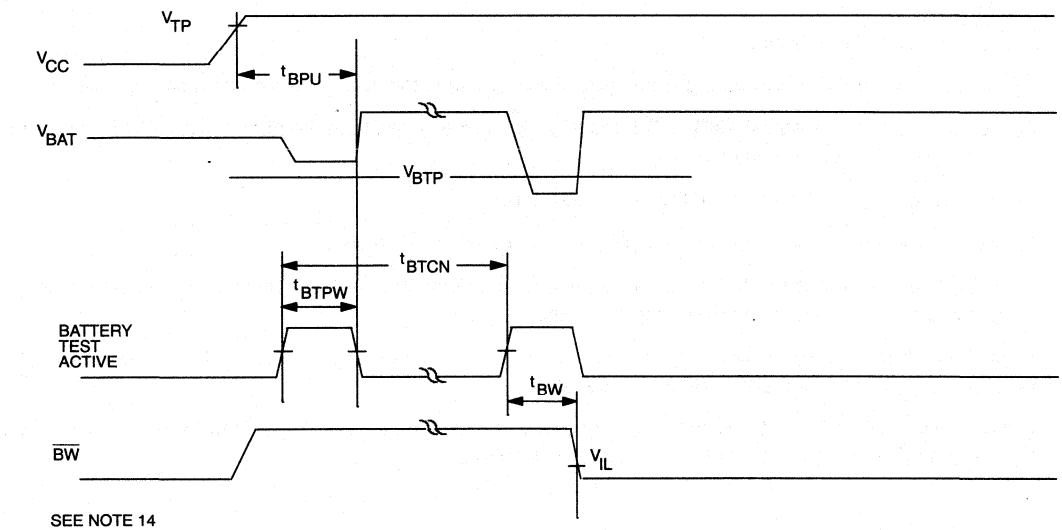
SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

2

POWER-DOWN/POWER-UP CONDITION



BATTERY WARNING DETECTION



POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	150			µs	
V_{CC} Fail Detect to $\overline{RST}$ Active	t_{RPD}	7		25	µs	14
V_{CC} slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	150			µs	
$\overline{CE}$, at V_{IH} after Power-Up	t_{REC}	2		125	ms	
V_{CC} Valid to $\overline{RST}$ Inactive	t_{RPU}	150	200	350	ms	14
V_{CC} Valid to $\overline{BW}$ Valid	t_{BPU}			1	s	14

BATTERY WARNING TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Test Cycle	t_{BTC}		24		hr	
Battery Test Pulse Width	t_{BTPW}			1	s	
Battery Test to $\overline{BW}$ Active	t_{BW}			1	s	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.

9. Each DS1330 has a built–in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1} and t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2} and t_{DH2} are measured from $\overline{CE}$ going high.
14. $\overline{RST}$ and $\overline{BW}$ are open–drain outputs, as such, cannot source current. External pull–up resistors should be connected to these pins for proper operation. Both pins will sink 10 mA.

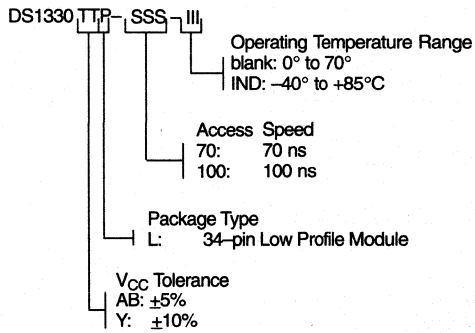
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

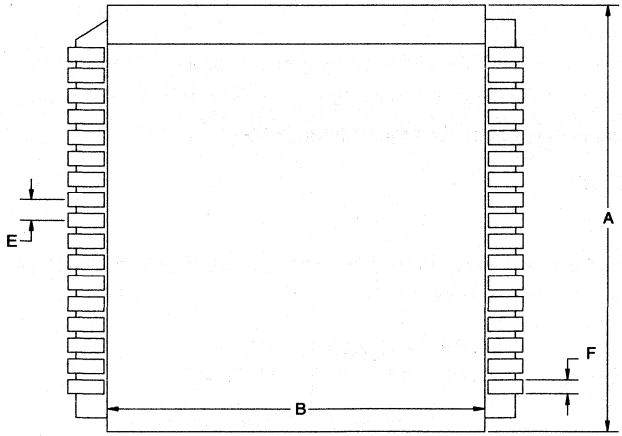
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

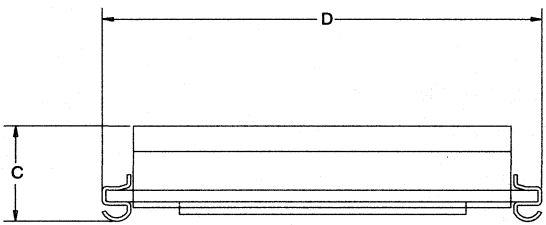
ORDERING INFORMATION



D1330Y/AB 34–PIN LOW PROFILE MODULE (LPM)



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.047	0.053
F	0.015	0.025



Suggested 68–pin PLCC surface mountable sockets with leads on two sides only are:

McKenzie	34P–SMT–3
Harwin	HIS–40001–04
Robin Nugent	PLCC–34–SMT
Dallas Semiconductor	DS34PIN–PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.

DALLAS SEMICONDUCTOR

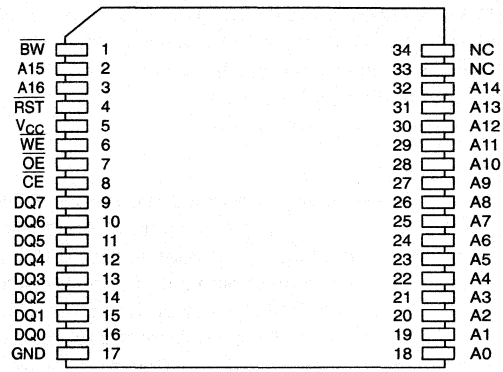
DS1345Y/AB
1024K Nonvolatile SRAM with Battery Monitor

2

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Replaces 128K x 8 volatile static RAM or EEPROM
- Monitors system V_{CC}, resets processor when power failure occurs and holds processor in reset during system power–up
- Monitors internal lithium battery and provides advanced warning of impending battery failure
- Unlimited write cycles
- Low–power CMOS operation
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1345Y)
- Optional ±5% V_{CC} operating range (DS1345AB)
- Low Profile Module package fits into standard 68–pin PLCC surface mountable sockets
- Optional industrial temperature range of –40°C to +85°C, designated IND

PIN ASSIGNMENT



34–PIN LOW PROFILE MODULE (LPM)

PIN DESCRIPTION

A0–A16	–	Address Inputs
DQ0–DQ7	–	Data In/Data Out
$\overline{CE}$	–	Chip Enable
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
$\overline{RST}$	–	Reset Output
$\overline{BW}$	–	Battery Warning Output
V_{CC}	–	+5 Volts
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS1345 1024K Nonvolatile SRAMs are 1,048,576–bit, fully static, nonvolatile SRAMs organized as 131,072 words by 8 bits. Each NV SRAM has a self–contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out–of–tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. Additionally, the DS1345 devices have dedicated circuitry for monitoring the status of V_{CC} and the status of the internal lithium battery. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interfacing. The nonvolatile static RAMs can be used in place of 128K x 8 SRAM, EEPROM or Flash devices. DS1345 devices in the Low Profile Module package are specifically designed for surface mount applications.

READ MODE

The DS1345 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 17 address inputs (A_0 - A_{16}) defines which of the 131,072 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1345 devices excute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1345AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1345Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data.

During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for DS1345AB and 4.5 volts for the DS1345Y.

SYSTEM POWER MONITORING

DS1345 devices have the ability to monitor the external V_{CC} power supply. When an out–of–tolerance power supply condition is detected, the NV SRAMs warn a processor–based system of impending power failure by asserting $\overline{RST}$. On power up, $\overline{RST}$ is held active for 200 ms nominal to prevent system operation during power–on transients and to allow t_{REC} to expire. $\overline{RST}$ has an open–drain output driver.

BATTERY MONITORING

The DS1345 devices automatically perform periodic battery voltage monitoring on a 24 hour time interval. Such monitoring begins within t_{REC} after V_{CC} rises above V_{TP} and is suspended when power failure occurs.

After each 24 hour period has elapsed, the battery is connected to an internal 1MΩ test resistor for one second. During this one second, if battery voltage falls below the battery voltage trip point V_{BTP}, the battery warning output $\overline{BW}$ is asserted. Once asserted, $\overline{BW}$ remains active until the module is replaced. The battery is still retested after each V_{CC} power–up, however, even if $\overline{BW}$ is active. If the battery voltage is found to be higher than V_{BTP} during such testing, $\overline{BW}$ is de–asserted and regular 24–hour testing resumed. $\overline{BW}$ has an open–drain output driver.

FRESHNESS SEAL AND SHIPPING

Each DS1345 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C, -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C, -40°C to +85°C for IND parts
Soldering Temperature	260°C For 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1345AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1345Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1345AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1345Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	14
Output Current @ 0.4V	I_{OL}	2.0			mA	14
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		300	600	µA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		100	150	µA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1345AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1345Y)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(t_A = 25°C)

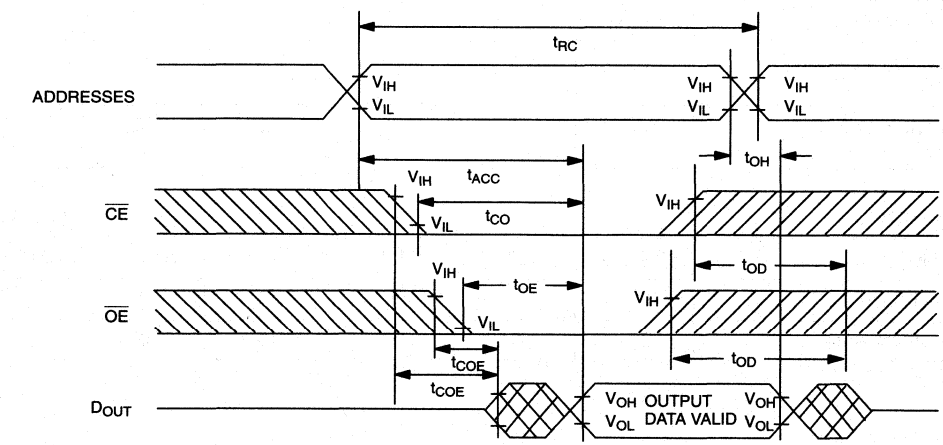
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1345AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1345Y)

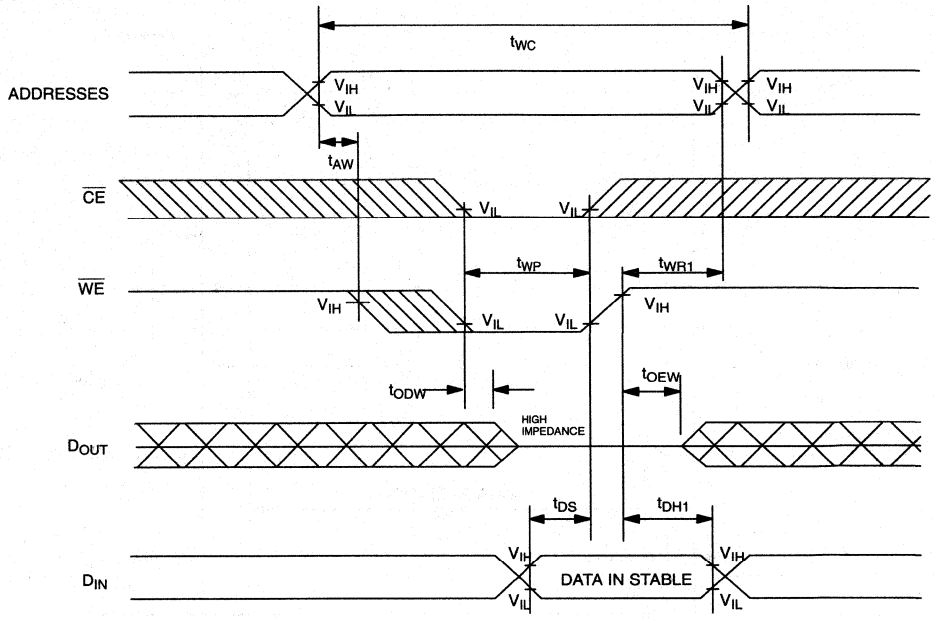
PARAMETER	SYMBOL	DS1345Y–70 DS1345AB–70		DS1345Y–100 DS1345AB–100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Access Time	t_{ACC}		70		100	ns	
OE to Output Valid	t_{OE}		35		50	ns	
CE to Output Valid	t_{CO}		70		100	ns	
OE or CE to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		100		ns	
Write Pulse Width	t_{WP}	55		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 10		5 10		ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 5		0 5		ns	12 13

READ CYCLE



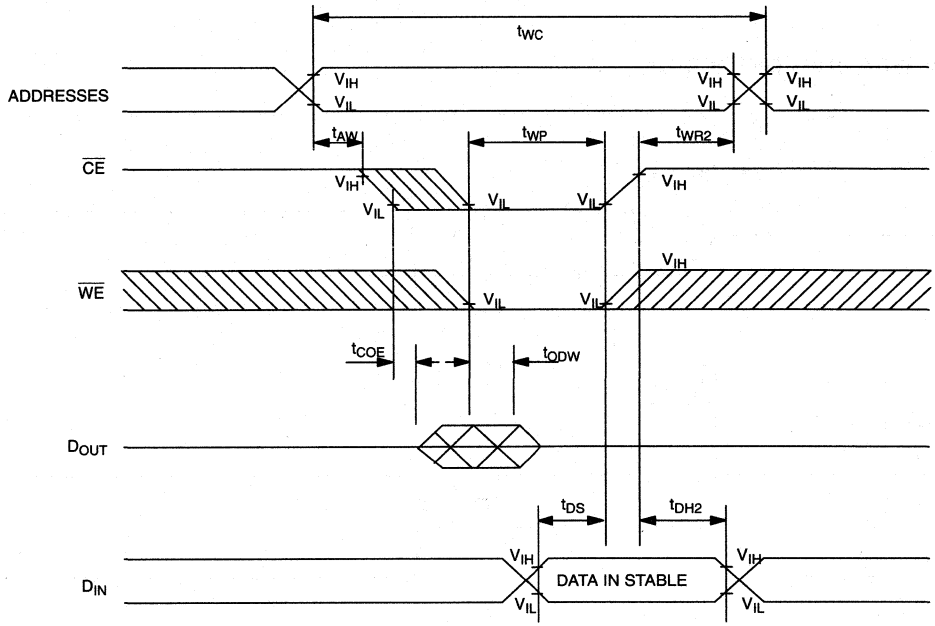
SEE NOTE 1

WRITE CYCLE 1



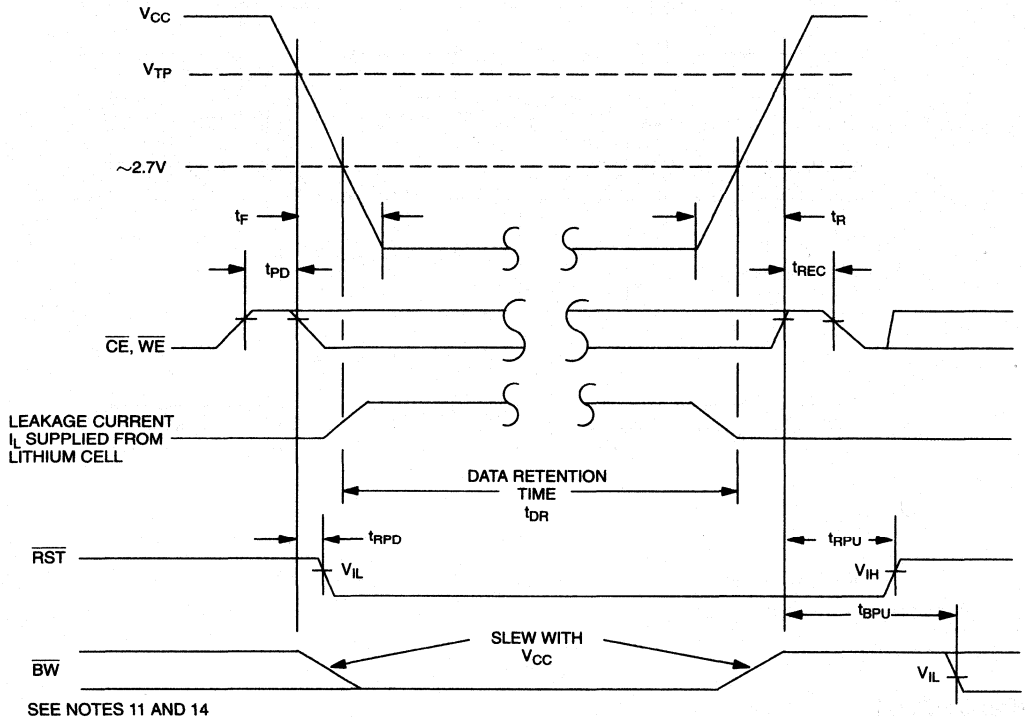
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2

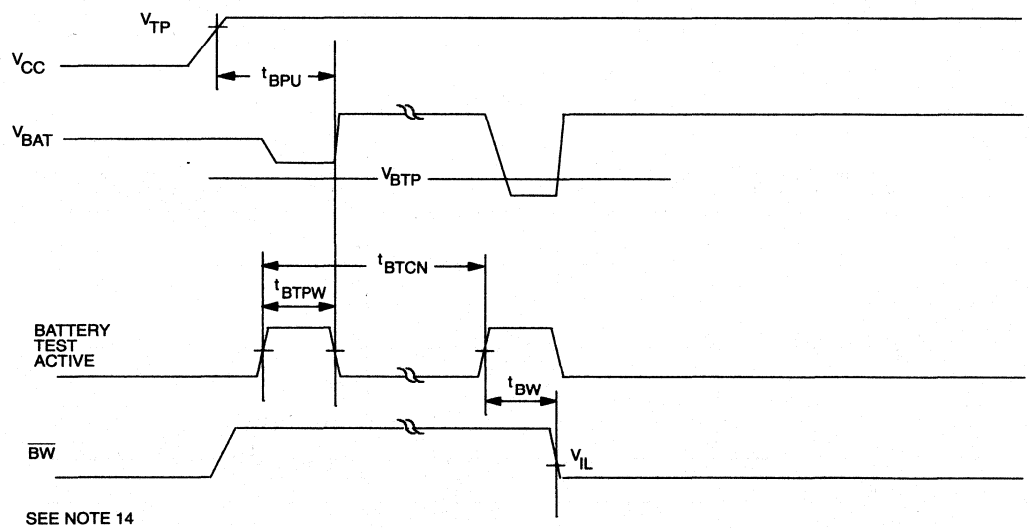


SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



BATTERY WARNING DETECTION



POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	150			µs	
V_{CC} Fail Detect to $\overline{RST}$ Active	t_{RPD}	7		25	µs	14
V_{CC} slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	150			µs	
$\overline{CE}$, at V_{IH} after Power-Up	t_{REC}	2		125	ms	
V_{CC} Valid to $\overline{RST}$ Inactive	t_{RPU}	150	200	350	ms	14
V_{CC} Valid to $\overline{BW}$ Valid	t_{BPU}			1	s	14

BATTERY WARNING TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Test Cycle	t_{BTC}		24		hr	
Battery Test Pulse Width	t_{BTPW}			1	s	
Battery Test to $\overline{BW}$ Active	t_{BW}			1	s	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.

9. Each DS1345 has a built–in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1} and t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2} and t_{DH2} are measured from $\overline{CE}$ going high.
14. $\overline{RST}$ and $\overline{BW}$ are open–drain outputs, as such, cannot source current. External pull–up resistors should be connected to these pins for proper operation. Both pins will sink 10 mA.

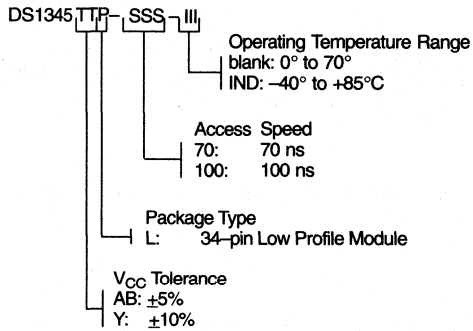
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

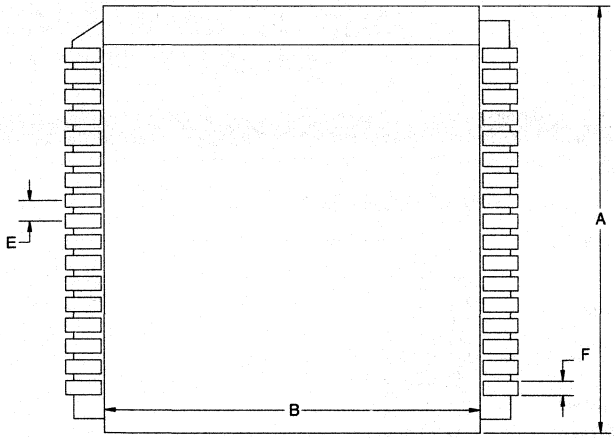
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

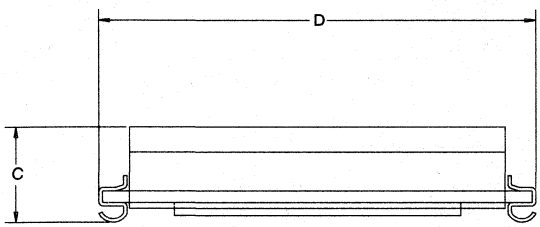
ORDERING INFORMATION



D1345Y/AB 34–PIN LOW PROFILE MODULE (LPM)



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.047	0.053
F	0.015	0.025



Suggested 68–pin PLCC surface mountable sockets with leads on two sides only are:

McKenzie	34P–SMT–3
Harwin	HIS–40001–04
Robin Nugent	PLCC–34–SMT
Dallas Semiconductor	DS34PIN–PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.

PRELIMINARY

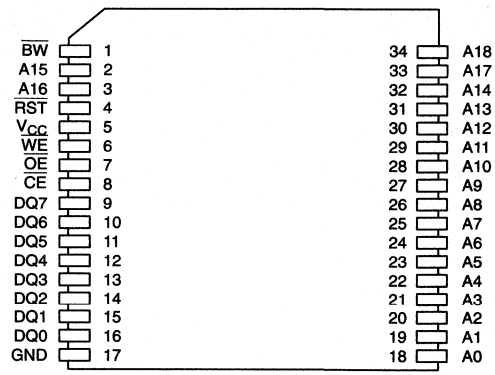
DALLAS SEMICONDUCTOR

DS1350Y/AB
4096K Nonvolatile SRAM with Battery Monitor

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Replaces 512K x 8 volatile static RAM or EEPROM
- Monitors system V_{CC}, resets processor when power failure occurs and holds processor in reset during system power–up
- Monitors internal lithium battery and provides advanced warning of impending battery failure
- Unlimited write cycles
- Low–power CMOS operation
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1350Y)
- Optional ±5% V_{CC} operating range (DS1350AB)
- Low Profile Module package fits into standard 68–pin PLCC surface mountable sockets
- Optional industrial temperature range of –40°C to +85°C, designated IND

PIN ASSIGNMENT



34–PIN LOW PROFILE MODULE (LPM)

PIN DESCRIPTION

A0–A18	–	Address Inputs
DQ0–DQ7	–	Data In/Data Out
$\overline{CE}$	–	Chip Enable
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
$\overline{RST}$	–	Reset Output
$\overline{BW}$	–	Battery Warning Output
V_{CC}	–	+5 Volts
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS1350 4096K Nonvolatile SRAMs are 4,194,304–bit, fully static, nonvolatile SRAMs organized as 524,288 words by 8 bits. Each NV SRAM has a self–contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out–of–tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. Additionally, the DS1350 devices have dedicated circuitry for monitoring the status of V_{CC} and the status of the internal lithium battery. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interfacing. The nonvolatile static RAMs can be used in place of 512K x 8 SRAM, EEPROM or Flash devices. DS1350 devices in the Low Profile Module package are specifically designed for surface mount applications.

READ MODE

The DS1350 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 19 address inputs (A_0 - A_{18}) defines which of the 524,288 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1350 devices excute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1350AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1350Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data.

During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for DS1350AB and 4.5 volts for the DS1350Y.

2

SYSTEM POWER MONITORING

DS1350 devices have the ability to monitor the external V_{CC} power supply. When an out–of–tolerance power supply condition is detected, the NV SRAMs warn a processor–based system of impending power failure by asserting $\overline{RST}$. On power up, $\overline{RST}$ is held active for 200 ms nominal to prevent system operation during power–on transients and to allow t_{REC} to expire. $\overline{RST}$ has an open–drain output driver.

BATTERY MONITORING

The DS1350 devices automatically perform periodic battery voltage monitoring on a 24 hour time interval. Such monitoring begins within t_{REC} after V_{CC} rises above V_{TP} and is suspended when power failure occurs.

After each 24 hour period has elapsed, the battery is connected to an internal 1MΩ test resistor for one second. During this one second, if battery voltage falls below the battery voltage trip point V_{BTP}, the battery warning output $\overline{BW}$ is asserted. Once asserted, $\overline{BW}$ remains active until the module is replaced. The battery is still retested after each V_{CC} power–up, however, even if $\overline{BW}$ is active. If the battery voltage is found to be higher than V_{BTP} during such testing, $\overline{BW}$ is de–asserted and regular 24–hour testing resumed. $\overline{BW}$ has an open–drain output driver.

FRESHNESS SEAL AND SHIPPING

Each DS1350 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C, -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C, -40°C to +85°C for IND parts
Soldering Temperature	260°C For 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1350AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1350Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1350AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1350Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	14
Output Current @ 0.4V	I_{OL}	2.0			mA	14
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		300	600	µA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		100	150	µA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1350AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1350Y)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

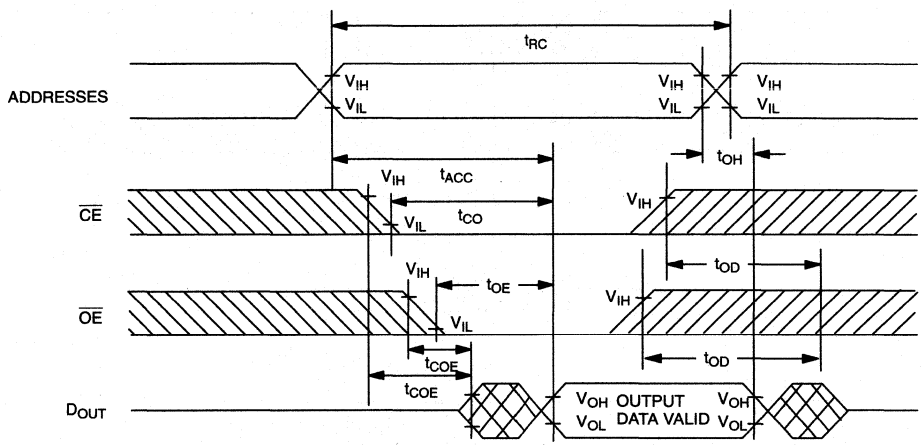
2

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1350AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1350Y)

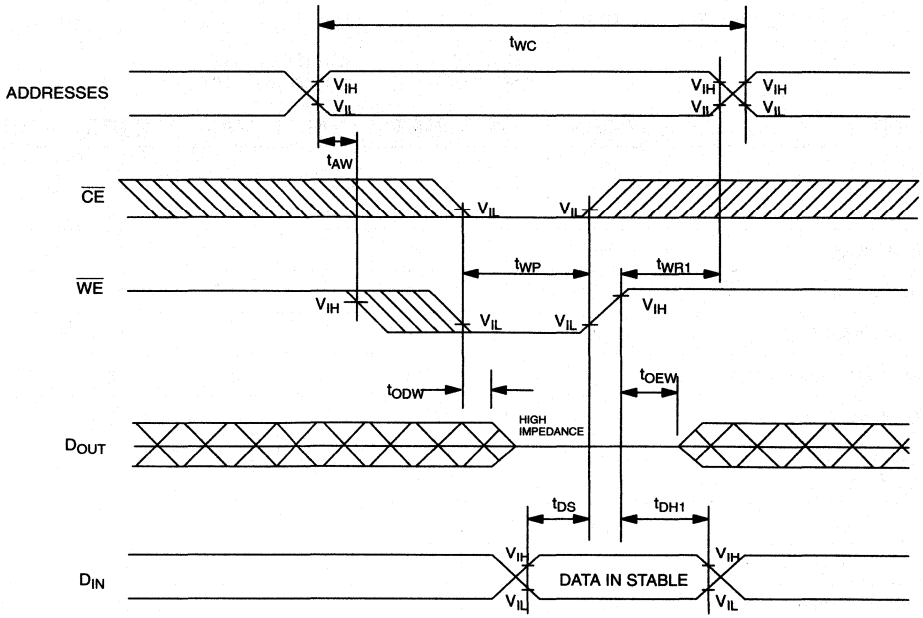
PARAMETER	SYMBOL	DS1350Y–70 DS1350AB–70		DS1350Y–100 DS1350AB–100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Access Time	t_{ACC}		70		100	ns	
OE to Output Valid	t_{OE}		35		50	ns	
CE to Output Valid	t_{CO}		70		100	ns	
OE or CE to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		100		ns	
Write Pulse Width	t_{WP}	55		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 10		5 10		ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 5		0 5		ns	12 13

READ CYCLE



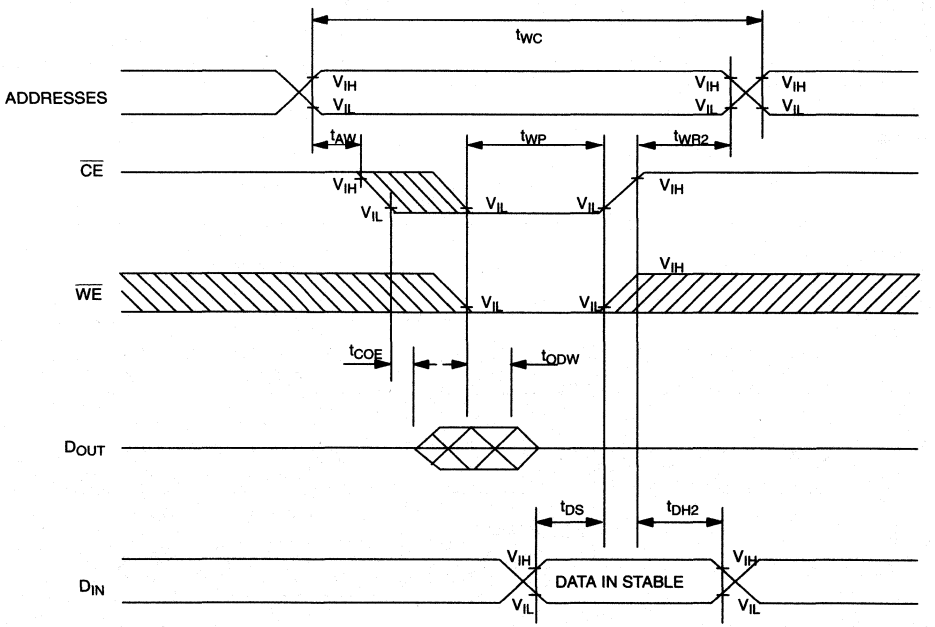
SEE NOTE 1

WRITE CYCLE 1



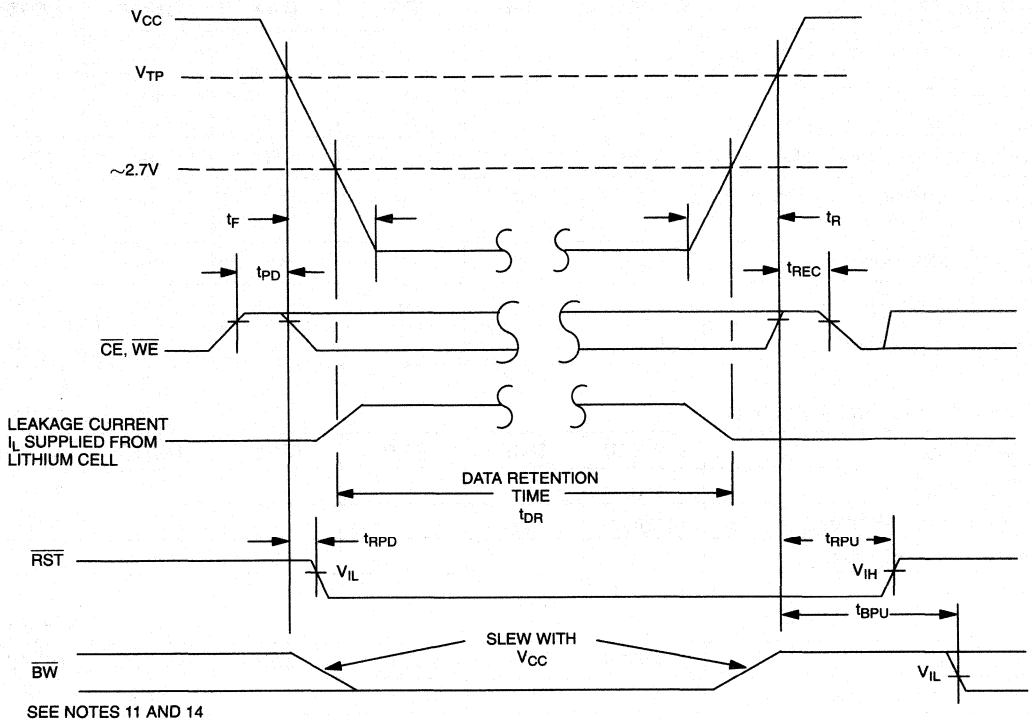
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



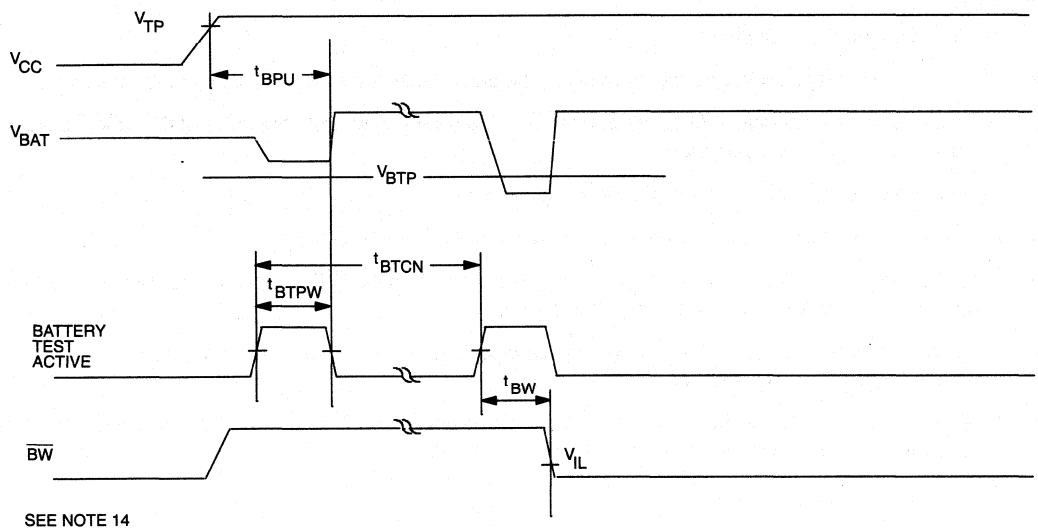
SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTES 11 AND 14

BATTERY WARNING DETECTION



SEE NOTE 14

POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	150			µs	
V_{CC} Fail Detect to $\overline{RST}$ Active	t_{RPD}	7		25	µs	14
V_{CC} slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	150			µs	
$\overline{CE}$, at V_{IH} after Power-Up	t_{REC}	2		125	ms	
V_{CC} Valid to $\overline{RST}$ Inactive	t_{RPU}	150	200	350	ms	14
V_{CC} Valid to $\overline{BW}$ Valid	t_{BPU}			1	s	14

BATTERY WARNING TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Test Cycle	t_{BTC}		24		hr	
Battery Test Pulse Width	t_{BTPW}			1	s	
Battery Test to $\overline{BW}$ Active	t_{BW}			1	s	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.

9. Each DS1350 has a built–in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1} and t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2} and t_{DH2} are measured from $\overline{CE}$ going high.
14. $\overline{RST}$ and $\overline{BW}$ are open–drain outputs, as such, cannot source current. External pull–up resistors should be connected to these pins for proper operation. Both pins will sink 10 mA.

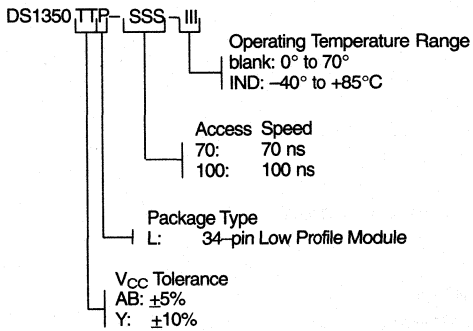
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

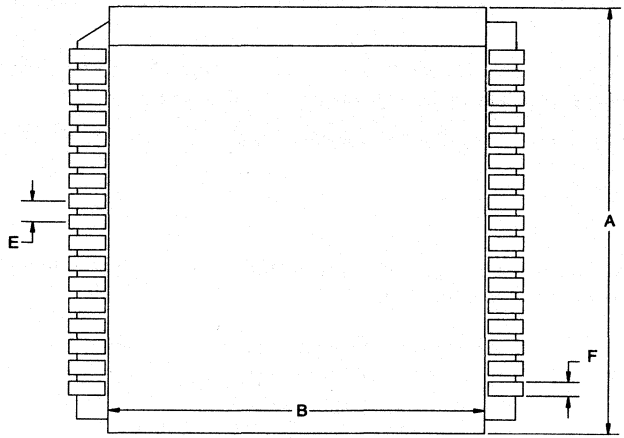
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

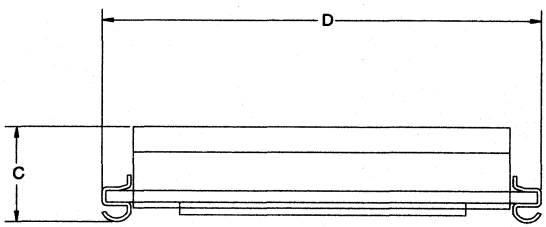
ORDERING INFORMATION



D1350Y/AB 34–PIN LOW PROFILE MODULE (LPM)



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.047	0.053
F	0.015	0.025



Suggested 68–pin PLCC surface mountable sockets with leads on two sides only are:

McKenzie	34P–SMT–3
Harwin	HIS–40001–04
Robin Nugent	PLCC–34–SMT
Dallas Semiconductor	DS34PIN–PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.

DALLAS SEMICONDUCTOR

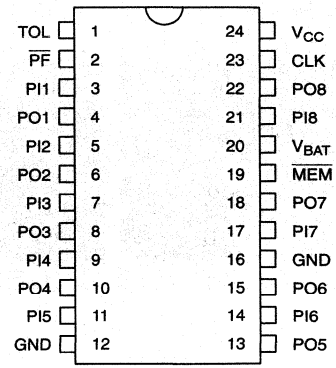
DS1380
RAMport

2

FEATURES

- 2K x 8 Static RAM
- 8-Bit Transparent I/O Port
- Battery connection provided for nonvolatility
- Multiplexed address/data bus reduces pin count
- 5% or 10% V_{CC} tolerance
- Power Fail output signal
- Low Power CMOS
- 24–pin DIP Package or optional 24–pin SOIC
- Ideally suited for microcontroller applications as add on memory

PIN ASSIGNMENT



24–PIN DIP (600 MIL)
24–PIN SOIC (300 MIL)

PIN DESCRIPTION

PI1 - PI8	–	Port Inputs (µP Ports)
PO1 - PO8	–	Port Outputs (External Ports)
$\overline{PF}$	–	Power Fail Output
CLK	–	Clock
$\overline{MEM}$	–	Memory Select
V_{BAT}	–	+ Battery Connection
V_{CC}	–	+5 Volts
GND	–	Ground

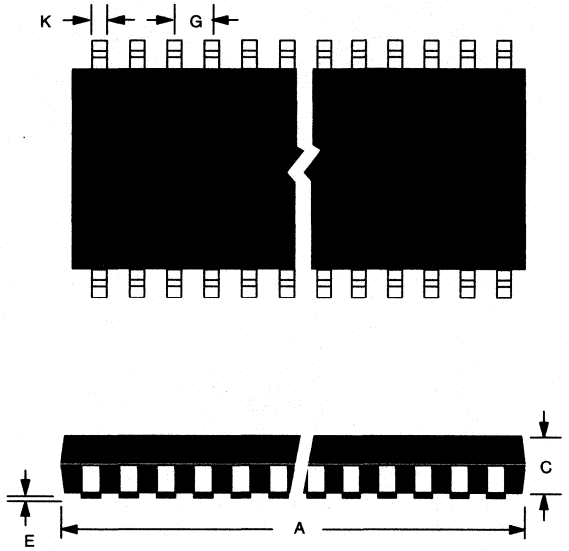
DESCRIPTION

The DS1380 is a 2K x 8 nonvolatile static RAM designed to connect directly to the port pins of a microcontroller. Eight of ten port pins required to interface with the microcontroller are reproduced by the DS1380 for general purpose use. The reproduced port pins can be both inputs and outputs and will appear exactly the same as the pins on the attached microcontroller. The static RAM is read or written with three successive cycles containing high order address, low order address and then data. Read, write and status information is passed to the DS1380 along with the high order address transfer. While transferring data to and from memory, the I/O status is locked and maintained. All data within the DS1380 can be made nonvolatile with direct connection of a 3 volt lithium battery. The DS1380 is controlled by only two signals: clock and memory select.

OPERATION

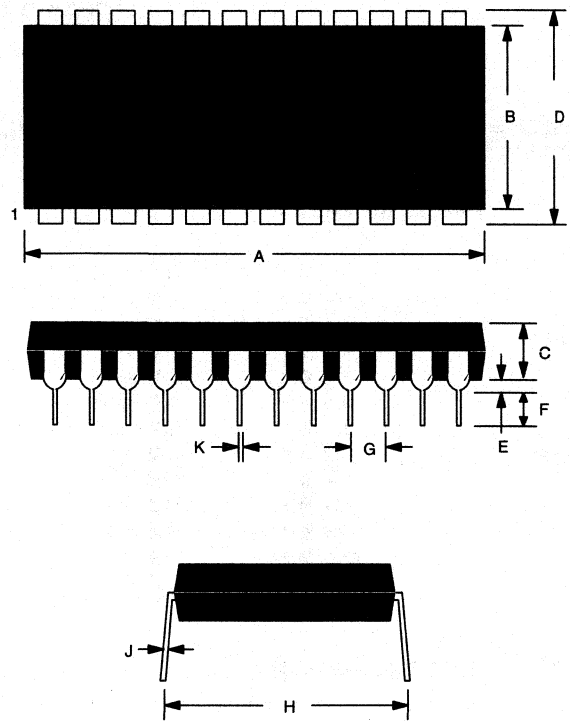
The DS1380 performs exactly to the specifications of the DS1381 with the exception of an external battery connection. The V_{BAT} pin is designed for a battery input voltage between 2.7 volts and 3.5 volts and requires a current of 100 nA at 25°C and 1 µA at 60°C. If battery backup operation is not required, the V_{BAT} input must be grounded. With the external battery connected, the DS1380 is nonvolatile and retains data in the absence of power. When the V_{BAT} input is grounded, the DS1380 is volatile and will not retain data without V_{CC}. For detailed operation and electrical specifications consult the DS1381 data sheet.

DS1380S RAMPORT



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.602 15.29	0.612 15.54
B IN. MM	0.290 7.37	0.300 7.62
C IN. MM	0.089 2.26	0.095 2.41
D IN. MM	0.325 8.26	0.330 8.38
E IN. MM	0.008 0.20	0.012 0.30
F IN. MM	0.097 2.46	0.105 2.68
G IN. MM	0.046 1.17	0.054 1.37
H IN. MM	0.400 10.16	0.410 10.41
J IN. MM	0.006 0.152	0.011 0.28
K IN. MM	0.013 0.33	0.019 0.48

DS1380 RAMPORT



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN.	1.245	1.270
MM	31.62	32.25
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.050
MM	0.380	1.27
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

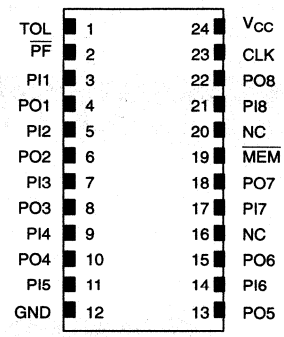
DALLAS SEMICONDUCTOR

DS1381
NV RAMport

FEATURES

- 2K x 8 Nonvolatile Static RAM
- 8-Bit Transparent I/O Port
- Greater than 10 years of data retention in absence of V_{CC}
- Multiplexed address/data bus reduces pin count
- Write protection for both RAM and port status at either 5% or 10%
- Power Fail output signal
- Low Power CMOS
- 24–pin DIP Package
- Ideally suited for microcontroller applications as add on memory

PIN ASSIGNMENT



24–PIN ENCAPSULATED PACKAGE

PIN DESCRIPTION

PI1 - PI8	–	Port Inputs (µP Ports)
PO1 - PO8	–	Port Outputs (External Ports)
$\overline{PF}$	–	Power Fail Output
CLK	–	Clock
$\overline{MEM}$	–	Memory Select
V_{CC}	–	+5 Volts
GND	–	Ground
NC	–	No Connection

Note: Pins 16 and 20 are missing by design.

DESCRIPTION

The DS1381 is a 2K x 8 nonvolatile static RAM designed to connect directly to the port pins of a microcontroller. Eight of ten port pins required to interface with the microcontroller are reproduced by the DS1381 for general purpose use. The reproduced port pins can be both inputs and outputs and will appear exactly the same as the pins on the attached microcontroller. The static RAM is read or written with three successive cycles containing high order address, low order address and then data. Read, write and status information is passed to the DS1381 along with the high order address transfer. While transferring data to and from memory, the I/O status is locked and maintained. All data within the DS1381 is nonvolatile and data retention time is over 10 years. The DS1381 is controlled by only two signals; clock and memory select.

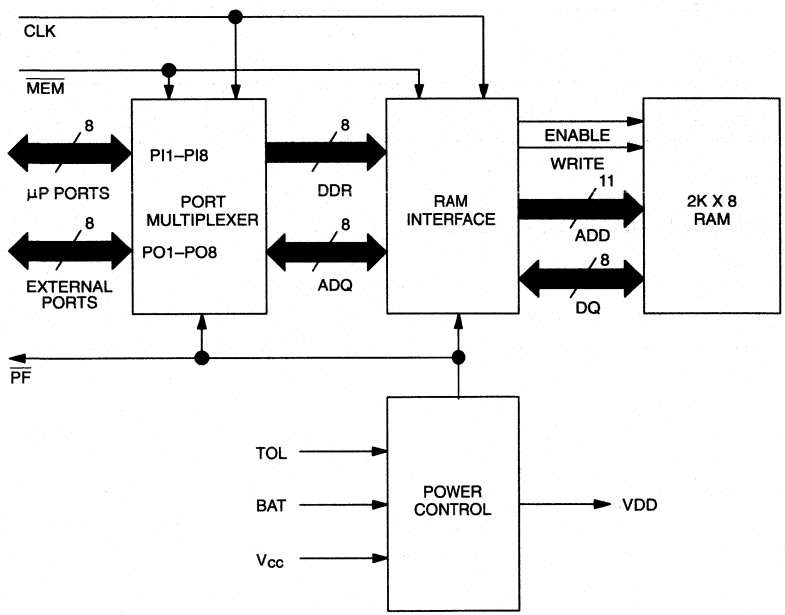
2

OPERATION–MEMORY AND PORT PINS

A block diagram of the DS1381 nonvolatile RAMport is shown in Figure 1. As shown, the DS1381 has four key elements; namely the port multiplexer, the RAM interface, a 2K x 8 static RAM, and a power control section. The port multiplexer is connected to eight microcontroller port pins from which address, data and port data are received. The 8 microcontroller port pins are reproduced through transmission gates at the multiplexer output when the $\overline{MEM}$ pin is high. When the $\overline{MEM}$ pin is low all reproduced output pins are latched in their high or low states and all reproduced inputs go to a high impedance state. With the $\overline{MEM}$ pin low the microcontroller port pins are then free to pass address and data to and from the nonvolatile static RAM. Each read or write cycle to memory is accomplished in three separate steps involving two address transfers and one data transfer. The clock signal (CLK) is used to strobe address and data information through the port multiplexer into the RAM interface circuitry. To accomplish RAM access the high order address (A8-A10) is placed on port input pins PI1 through PI3. PI4 through PI8 contain bits which dictate a read of RAM or a write to RAM. If these bits do not match exactly the bit patterns as shown in Figure 2, completion of the full cycle will be allowed but no action will be taken during the data transfer portion. With the proper bit patterns placed on the port pins, the CLK input is then transitioned high to low and then high again. The clock action allows the address and read/write information to propagate through the port multiplexer and latch the information into the RAM interface. Next the low order address (A0-A7) is placed on the port input pins (PI1 through PI8) and the second address transfer also propagates through the port multiplexer as CLK goes low and returns high. The RAM is now ready for data transfer. If a write cycle is to occur, the microcontroller port pins must deliver the correct data to be written. As the CLK transitions high to low, data propagates through the port multiplexer and the RAM interface and finally to the RAM where data is written into RAM. The write cycle is terminated when the CLK transitions low to high. Data can then be removed from the port input pins. If during the data transfer a read cycle is to occur, the port input pins must not be driven by the microcontroller. Then as CLK transitions high to low, the RAM becomes active and data is presented on the port input pins for the microcontroller to read. A read cycle is terminated when the CLK signal is transitioned low to high and the port input pins are returned to a high impedance state.

After completing the read or write cycle another read or write cycle can be performed without pulsing the $\overline{MEM}$ pin high between cycles. After all access to the RAM is complete, the $\overline{MEM}$ pin must be returned to a high state.

FUNCTIONAL BLOCK DIAGRAM Figure 1



OPERATION - WRITING THE DATA DIRECTION REGISTER

The data direction register is written with a logic one in each bit location which will have a corresponding high impedance output pin (PO1-PO8) during reading and writing of the memory of the DS1381 by the microcontroller (see Figure 3). This will avoid contention between PO1-PO8 and devices driving PO1-PO8 as inputs. To write data to the data direction register, the CLK input is driven low prior to $\overline{MEM}$ going low. With CLK low $\overline{MEM}$ is driven low which latches the port output pins and readies the DS1381 for data direction information. Data direction information is then placed on the port input pins by the microcontroller and is written into the data direction register as $\overline{MEM}$ transitions low to high. While the data direction register is being written, the output pins (PO1 through PO8) are latched to the PI1 through PI8 states with their high or low impedance condition determined by the old data direction contents. The new data direction contents will be effective the next time $\overline{MEM}$ is taken to a low state.

OPERATION - POWER FAIL AND DATA RETENTION MODE

The DS1381 has full functional capability when V_{CC} is within normal limits. However, when V_{CC} goes to an out of tolerance level, the nonvolatile RAMport assumes a write protected status such that the memory and data direction register cannot be accessed. In addition the port output signals go to a high impedance state, the port input pins become "don't care" and the transmission gates connecting the 8 microprocessor port pins to the external ports will go to a low impedance state. The power fail pin ($\overline{PF}$) goes to an active low level when power fail occurs and remains low until V_{CC} returns to nominal limits. The point at which write protection occurs depends on the level of the tolerance pin (TOL). When TOL is grounded, write protection will occur between 4.75 volts and 4.5 volts. When TOL is connected to V_{CC}, write protection occurs between 4.5 volts and 4.25 volts. After power fail detection has occurred and the V_{CC} level falls below the voltage level of the internal lithium cell the internal memory and register contents are maintained by this cell which is capable of maintaining data for over 10 years. The switch over from V_{CC} to the lithium cell occurs when V_{CC} is below approximately 3 volts.

READ AND WRITE BIT PATTERNS Figure 2

	LSB							MSB
READ	A8	A9	A10	1	0	1	0	1
WRITE	A8	A9	A10	0	1	0	1	0

DATA DIRECTION REGISTER BITS Figure 3

LSB							MSB
PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (TOL=GND)	V_{CC}	4.75	5.0	5.5	V	1
Supply Voltage (TOL=V_{CC})	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} within DC operating conditions)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Current t_{CYC}=200 ns	I_{CC1}		20	25	mA	2
Standby Current	I_{CC2}		3	7	mA	3
Logic 1 Out @ 1 mA	V_{OH}	2.4			V	1, 6
Logic 0 Out @ 2 mA	V_{OL}			0.4	V	1, 6
V_{CC} Write Protect (TOL=GND)	V_{TP}	4.50	4.62	4.75	V	1
V_{CC} Write Protect (TOL=VCC)	V_{TP}	4.25	4.37	4.50	V	1
Input Leakage	I_{IL}	-1.0		+1.0	µA	4
Output Leakage	I_{LO}	-1.0		+1.0	µA	5
Port Pins In to Out Impedance	P_Z		75	150	Ω	7

CAPACITANCE

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	t_A=25°C			10	pF	
Output Capacitance	C_{OUT}	t_A=25°C			10	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C TOL = V_{CC}; V_{CC}=4.50 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Low	t_{CL}	150			ns	
Clock High	t_{CH}	50			ns	
Address Setup	t_{AS}	20			ns	
Address Hold	t_{AH}	0			ns	
Data Setup	t_{DS}	20			ns	
Data Hold	t_{DH}	0			ns	
$\overline{MEM}$ to CLK Low	t_{MC}	40			ns	
$\overline{MEM}$ to Output Latch	t_{ML}	25			ns	
CLK to $\overline{MEM}$ High	t_{CMH}	10			ns	
CLK to Data Valid	t_{CD}			100	ns	
CLK to Data at High Z	t_{DZ}			20	ns	
CLK to $\overline{MEM}$ Active	t_{CM}	40			ns	
DDR Data Setup	t_{DSD}	100			ns	
V_{CC} Slew Rate	t_R, t_F	250			µs	

DATA RETENTION

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	

NOTES:

1. All voltages are reference to ground
2. Active current is defined as $\overline{MEM}$ low with CLK low and all outputs are open
3. Standby current is defined as $\overline{MEM}$ high with CLK high and all outputs are open
4. Input leakage applies to CLK and $\overline{MEM}$ only
5. Output leakage applies to $\overline{PF}$ only
6. Logic levels apply to $\overline{PF}$ and PO1-PO8 when these outputs are latched
7. Port input to output impedance is the on resistance of the transmission gate between port inputs and port outputs with $\overline{MEM}$ high and with less than 4 mA flowing through the transmission gate.

DC TEST CONDITIONS

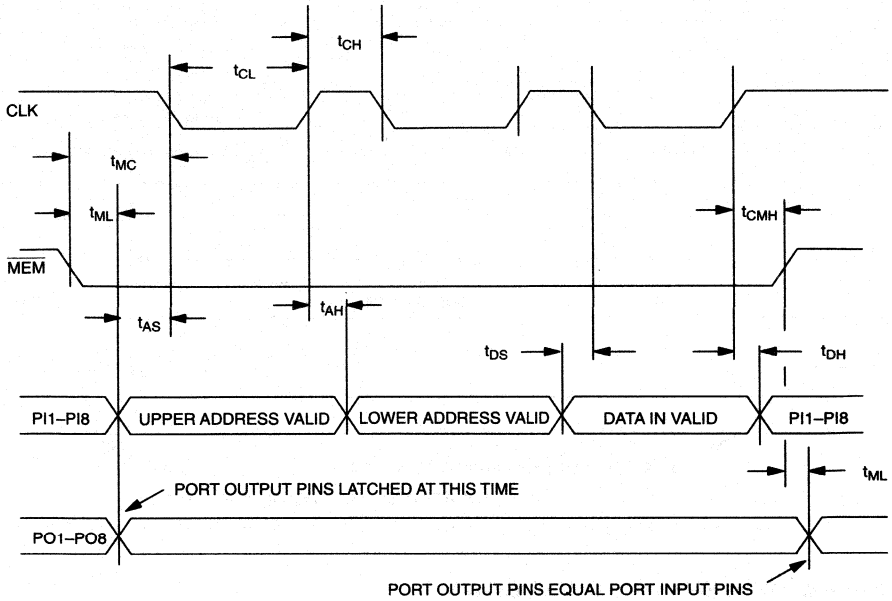
Outputs Open
All voltages are referenced to ground.

AC TEST CONDITIONS

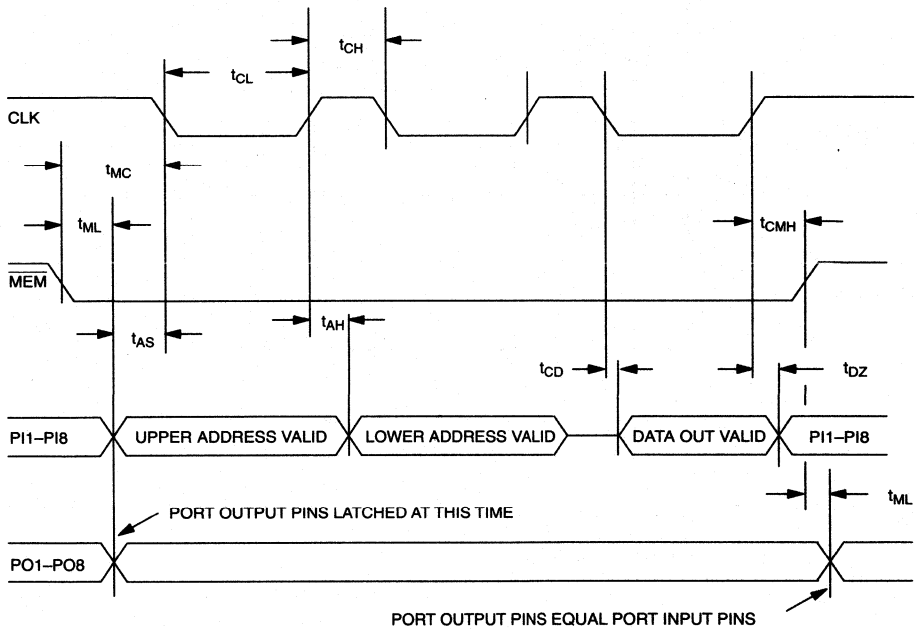
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0V - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

2

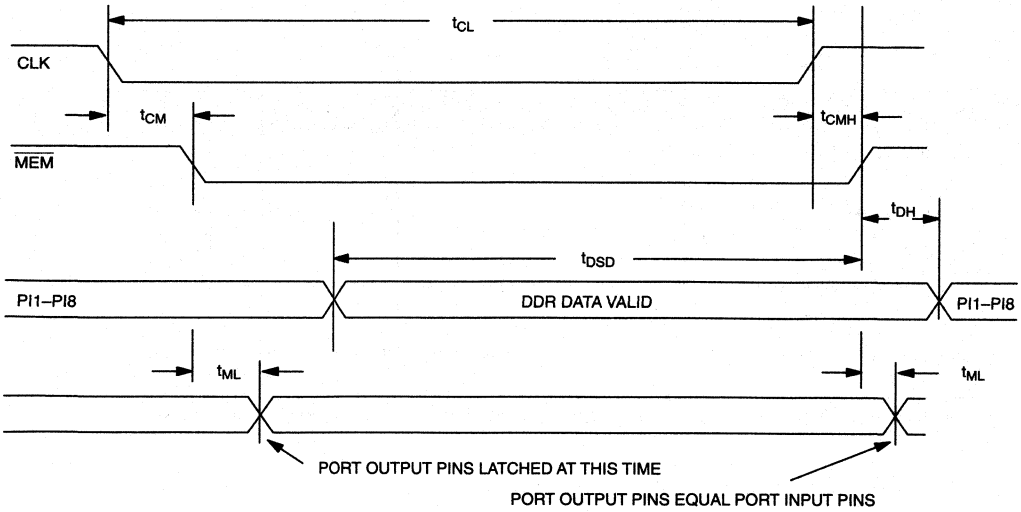
TIMING DIAGRAM: WRITE CYCLE TO MEMORY



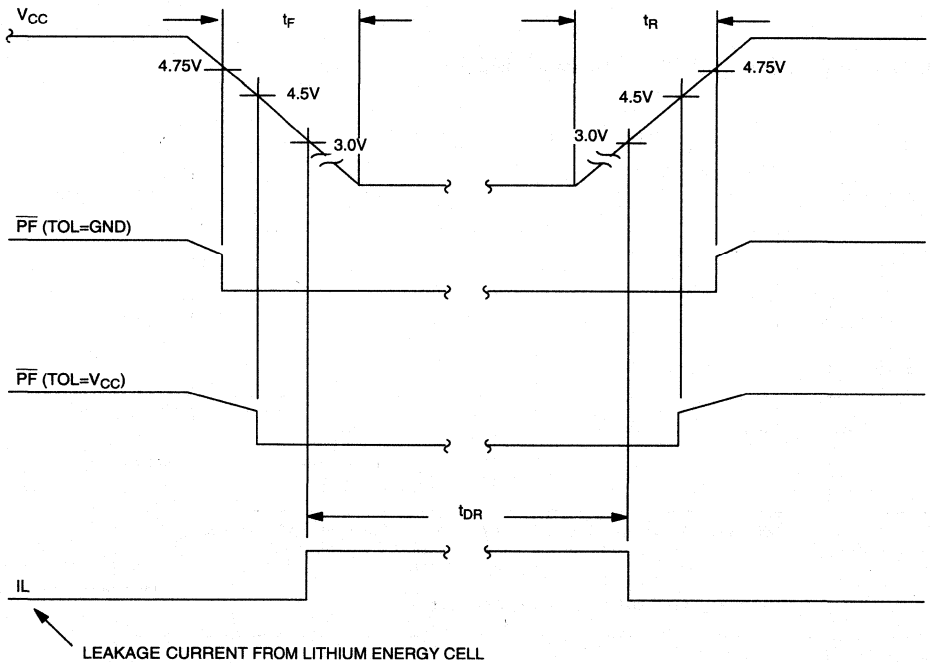
TIMING DIAGRAM: READ CYCLE FROM MEMORY



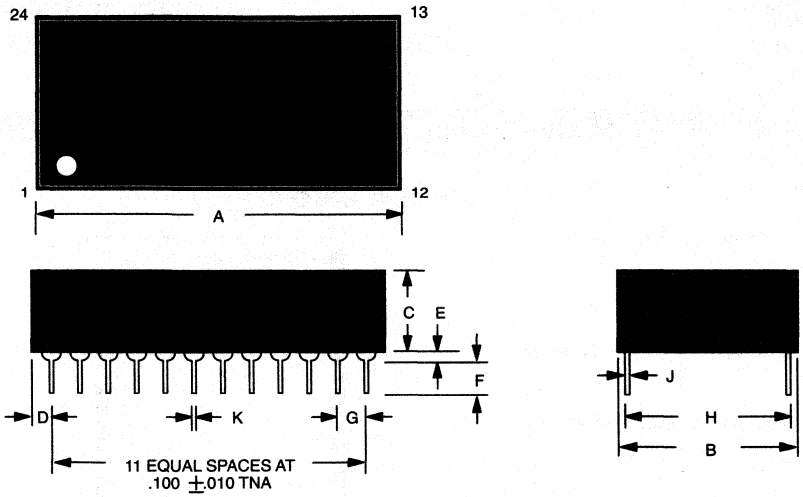
TIMING DIAGRAM: WRITE CYCLE TO DATA DIRECTION REGISTER



TIMING DIAGRAM: POWER UP - POWER DOWN



NONVOLATILE RAMPORT



DIM	MIN	MAX
A IN.	1.320	1.335
MM	33.53	33.91
B IN.	0.675	0.700
MM	17.14	17.78
C IN.	0.345	0.370
MM	8.76	9.40
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.035
MM	0.38	0.89
F IN.	0.110	0.140
MM	2.79	3.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 16 AND 20 ARE MISSING BY DESIGN

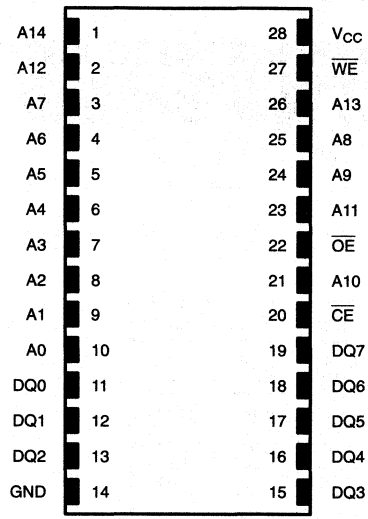
DALLAS SEMICONDUCTOR

DS1630Y/AB
Partitionable 256K NV SRAM

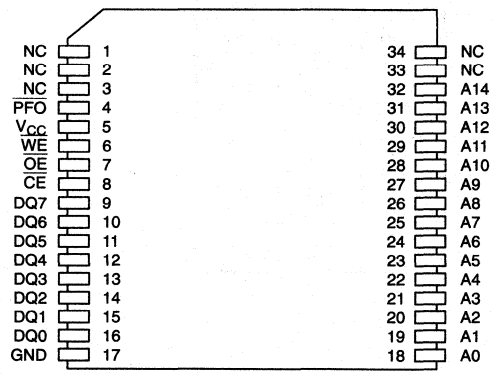
FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 32K x 8 volatile static RAM or EEPROM
- Write protects selected blocks of memory when programmed
- Unlimited write cycles
- Low-power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1630Y)
- Optional ±5% V_{CC} operating range (DS1630AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND
- JEDEC standard 28-pin DIP package
- Low Profile Module (LPM) package
  - Fits into standard 68–pin PLCC surface mountable socket
  - 255 mils package height
  - Power Fail Output ($\overline{PFO}$) warns system of impending V_{CC} power failure

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED



34–PIN LOW PROFILE MODULE (LPM)

PIN DESCRIPTION

A0 - A14	–	Address Inputs
DQ0 - DQ7	–	Data In/Data Out
$\overline{CE}$	–	Chip Enable
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
$\overline{PFO}$	–	Power Fail Output (LPM only)
V_{CC}	–	Power (+5V)
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS1630 256K Nonvolatile SRAMs are 262,144-bit, fully static, nonvolatile SRAMs organized as 32,768 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. In addition, the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt programs and important data. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing. DIP–package DS1630 devices can be used in place of existing 32K x 8 SRAMs directly conforming to the popular bytewide 28–pin DIP standard. The DIP devices also match the pinout of 28256 EEPROMs, allowing direct substitution while enhancing performance. DS1630 devices in the Low Profile Module package are specifically designed for surface mount applications. DS1630 LPM devices also have an additional pin, a Power Fail Output, that can be used to warn a system of impending V_{CC} power failure.

READ MODE

The DS1630 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 15 address inputs (A_0 - A_{14}) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1630 devices execute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1630AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1630Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvoltile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1630AB and 4.5 volts for the DS1630Y.

FRESHNESS SEAL

Each DS1630 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

PARTITION PROGRAMMING MODE

The register controlling the partitioning logic is selected by recognition of a specific binary pattern which is sent on address lines A11 - A14. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycles will load the partition register. Since there are 16 protectable partitions, the size of each partition is 32K/16 or 2K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycles as defined by A11 through A14 and shown in Table 2. A logical 1 in a bit location write protects the corresponding partition. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A12 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1630 devices to internally inhibit $\overline{WE}$ for all write accesses where A14 A13 A12 A11=0101. Note that while programming the partition register, data which is being accessed from the RAM should be ignored, since the purpose of the 24 read cycles is to program the partition register, not to access data from RAM.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A11	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A12	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A13	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A14	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST BITS ENTERED

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{14} A_{13} A_{12} A_{11})
A11	BIT 21	PARTITION 0	0000
A12	BIT 21	PARTITION 1	0001
A13	BIT 21	PARTITION 2	0010
A14	BIT 21	PARTITION 3	0011
A11	BIT 22	PARTITION 4	0100
A12	BIT 22	PARTITION 5	0101
A13	BIT 22	PARTITION 6	0110
A14	BIT 22	PARTITION 7	0111
A11	BIT 23	PARTITION 8	1000
A12	BIT 23	PARTITION 9	1001
A13	BIT 23	PARTITION 10	1010
A14	BIT 23	PARTITION 11	1011
A11	BIT 24	PARTITION 12	1100
A12	BIT 24	PARTITION 13	1101
A13	BIT 24	PARTITION 14	1110
A14	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C, –40°C to +85°C for IND parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1630 Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1630AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 10% for DS1630Y)
(t_A: See Note 10) (V_{CC}=5V ± 5% for DS1630AB)

PARAMETER	SYMBLE	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	14
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1630Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1630AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBLE	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

2

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1630AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1630Y)

PARAMETER	SYMBOL	DS1630Y-70 DS1630AB–70		DS1630Y-85 DS1630AB–85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		ns	
Access Time	t_{ACC}		70		85	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		45	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		85	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		85		ns	
Write Pulse Width	t_{WP}	55		65		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	10 10		10 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		30	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		35		ns	4
Data Hold Time	t_{DH1} t_{DH2}	5 5		5 5		ns ns	12 13

PARAMETER	SYMBOL	DS1630Y-100 DS1630AB–100		DS1630Y-120 DS1630AB–120		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	100		120		ns	
Access Time	t_{ACC}		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		120		ns	
Write Pulse Width	t_{WP}	75		90		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	10 10		10 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	40		50		ns	4
Data Hold Time	t_{DH1} t_{DH2}	5 5		5 5		ns ns	12 13

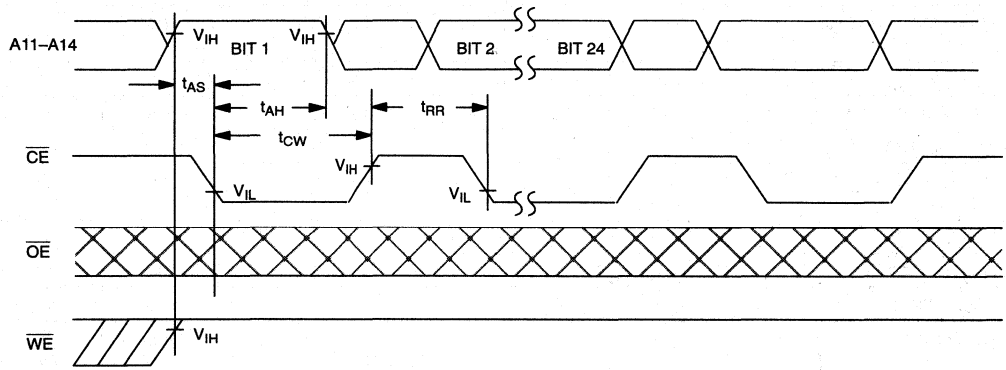
AC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CCI}=4.50V to 5.50V)*

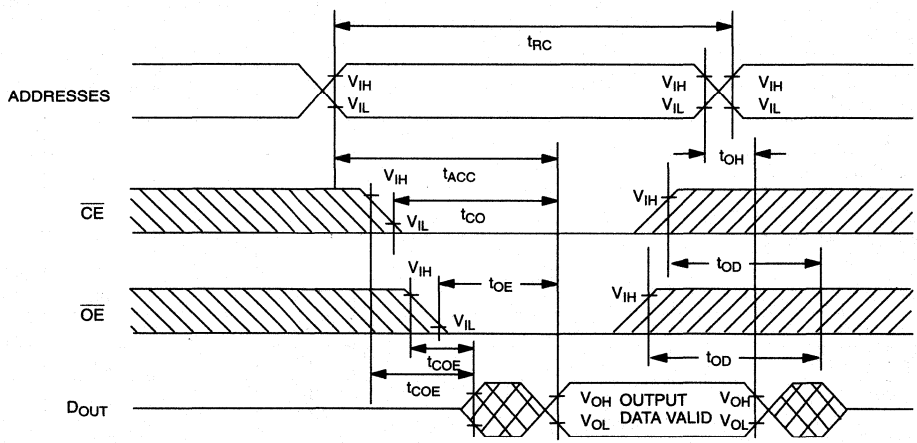
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	10			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

*For loading partition register

TIMING DIAGRAM: LOADING PARTITION REGISTER



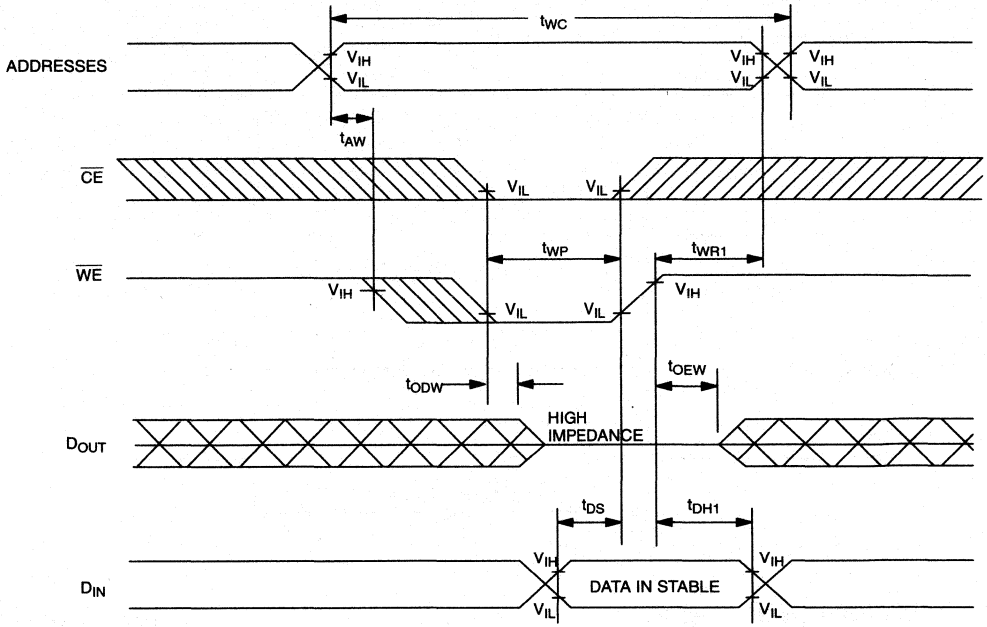
READ CYCLE



SEE NOTE 1

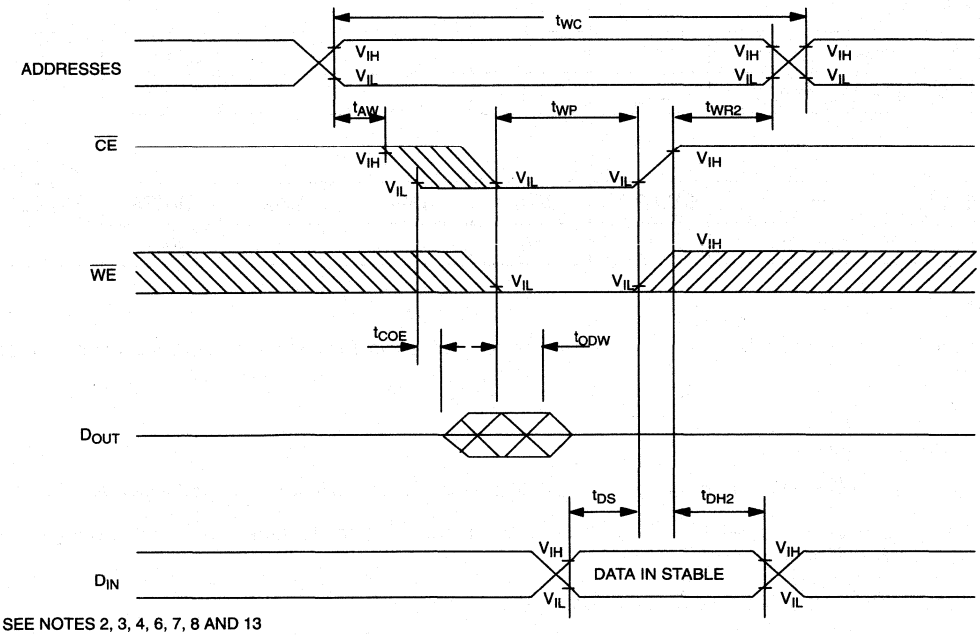
2

WRITE CYCLE 1



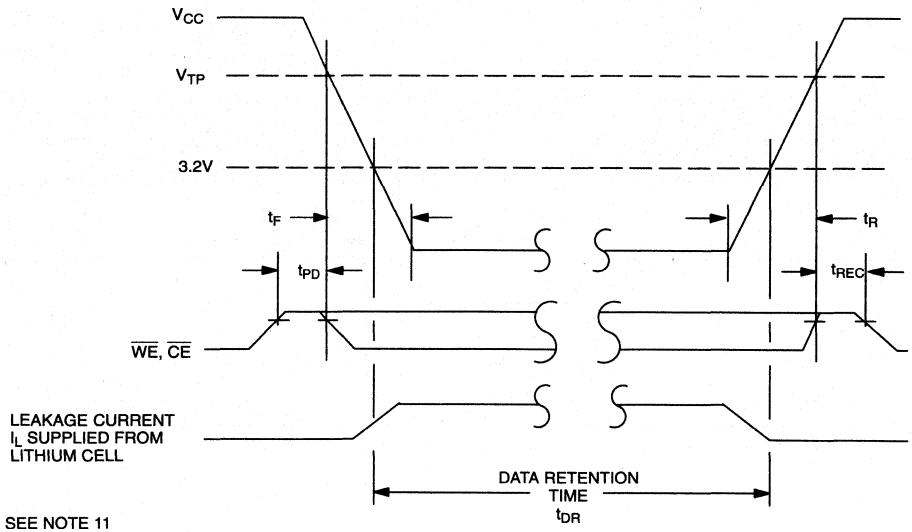
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power–Down	t_{PD}	0			µs	11
V_{CC} slew from V_{TP} to 0V	t_F	300			µs	
V_{CC} slew from 0V to V_{TP}	t_R	0			µs	
$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power–Up	t_{REC}	25			ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1630 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C for industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
14. The power fail output signal ($\overline{PFO}$) is driven active (V_{OL}=0.4V) when the V_{CC} trip point occurs. While active, the $\overline{PFO}$ pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of $\overline{PFO}$ is 2.4 volts minimum and will source a current of 1 mA. This signal is only present on the LPM package variations.
15. DS1630 modules are recognized by Underwriters Laboratory (U.L.®) under file E99151(R).

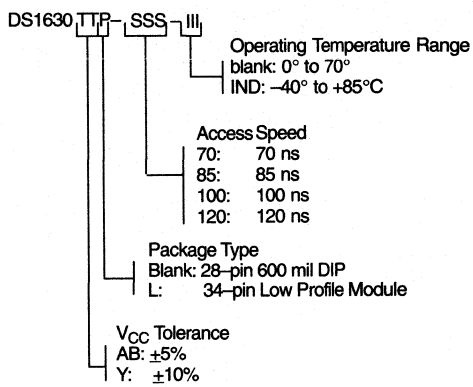
DC TEST CONDITIONS

Outputs Open
t Cycle = 200 ns
All voltages are referenced to ground

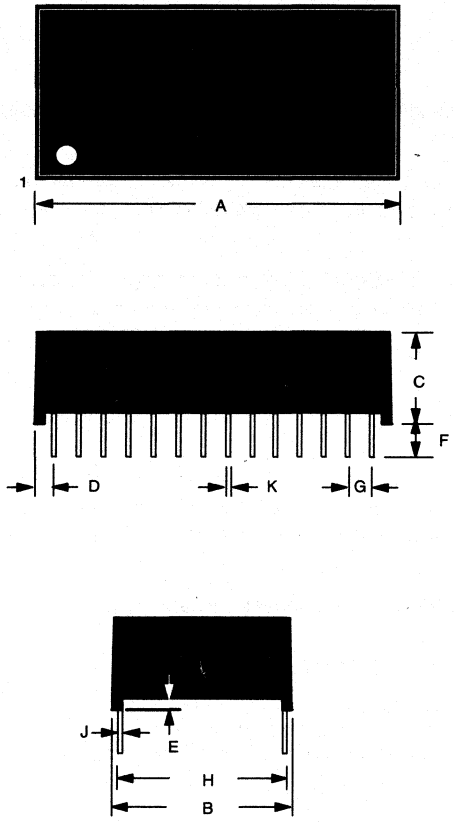
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION

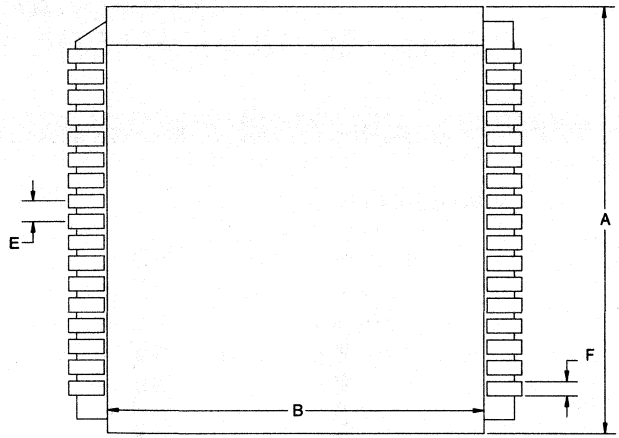


DS1630Y/AB NONVOLATILE SRAM, 28–PIN 740 MIL EXTENDED MODULE

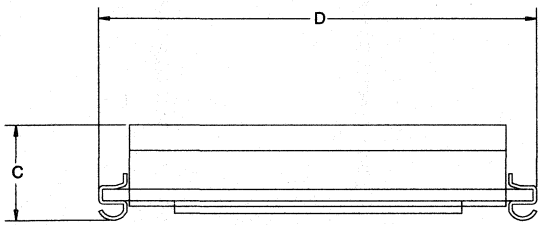


PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.480	1.500
MM	37.60	38.10
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.355	0.375
MM	9.02	9.52
D IN.	0.080	0.110
MM	2.03	2.79
E IN.	0.015	0.025
MM	0.38	0.63
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1630Y/AB 34–PIN LOW PROFILE MODULE (LPM)



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.047	0.053
F	0.015	0.025



Suggested 68–pin PLCC surface mountable sockets with leads on two sides only are:

McKenzie	34P–SMT–3
Harwin	HIS–40001–04
Robinson Nugent	PLCC–34–SMT
Dallas Semiconductor	DS34PIN–PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.

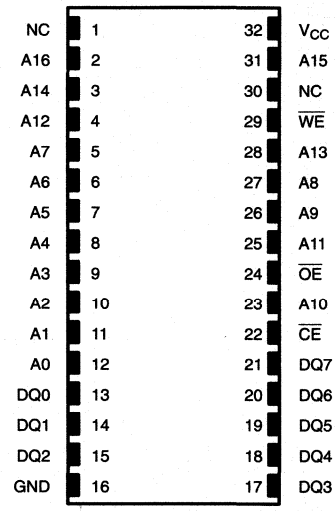
DALLAS SEMICONDUCTOR

DS1645Y/AB
Partitionable 1024K NV SRAM

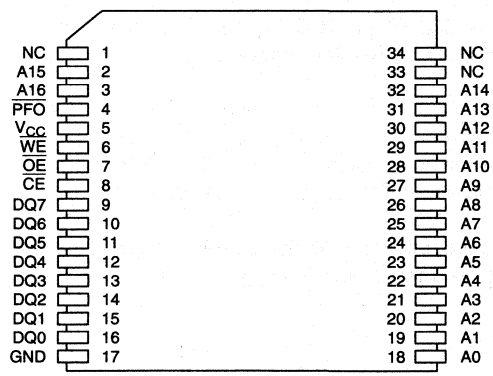
FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 128K x 8 volatile static RAM
- Write protects selected blocks of memory when programmed
- Unlimited write cycles
- Low-power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1645Y)
- Optional ±5% V_{CC} operating range (DS1645AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND
- JEDEC standard 32-pin DIP package
- Low Profile Module (LPM) package
  - Fits into standard 68–pin PLCC surface mountable socket
  - 250 mil package height
  - Power Fail Output ($\overline{PFO}$) warns system of impending V_{CC} power failure

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED



34–PIN LOW PROFILE MODULE (LPM)

PIN DESCRIPTION

A0 - A16	–	Address Inputs
DQ0 - DQ7	–	Data In/Data Out
$\overline{CE}$	–	Chip Enable
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
$\overline{PFO}$	–	Power Fail Output (LPM only)
V_{CC}	–	Power (+5V)
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS1645 1024K Nonvolatile SRAMs are 1,048,576-bit, fully static, nonvolatile SRAMs organized as 131,072 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. In addition, the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt programs and important data. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing. DIP–package DS1645 devices can be used in place of existing 128K x 8 SRAMs directly conforming to the popular bytewide 32–pin DIP standard. DS1645 devices in the Low Profile Module package are specifically designed for surface mount applications. DS1645 LPM devices also have an additional pin, a Power Fail Output, that can be used to warn a system of impending V_{CC} power failure.

READ MODE

The DS1645 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 17 address inputs (A_0 - A_{16}) defines which of the 131,072 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1645 devices execute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1645AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1645Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvoltile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1645AB and 4.5 volts for the DS1645Y.

FRESHNESS SEAL

Each DS1645 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

PARTITION PROGRAMMING MODE

The register controlling the partitioning logic is selected by recognition of a specific binary pattern which is sent on address lines A13 - A16. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycles will load the partition register. Since there are 16 protectable partitions, the size of each partition is 128K/16 or 8K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycles as defined by A13 through A16 and shown in Table 2. A logical 1 in a bit location write protects the corresponding partition. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A14 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1645 devices to internally inhibit $\overline{WE}$ for all write accesses where A16 A15 A14 A13=0101. Note that while programming the partition register, data which is being accessed from the RAM should be ignored, since the purpose of the 24 read cycles is to program the partition register, not to access data from RAM.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A13	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A14	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A15	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A16	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST BITS ENTERED

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{16} A_{15} A_{14} A_{13})
A13	BIT 21	PARTITION 0	0000
A14	BIT 21	PARTITION 1	0001
A15	BIT 21	PARTITION 2	0010
A16	BIT 21	PARTITION 3	0011
A13	BIT 22	PARTITION 4	0100
A14	BIT 22	PARTITION 5	0101
A15	BIT 22	PARTITION 6	0110
A16	BIT 22	PARTITION 7	0111
A13	BIT 23	PARTITION 8	1000
A14	BIT 23	PARTITION 9	1001
A15	BIT 23	PARTITION 10	1010
A16	BIT 23	PARTITION 11	1011
A13	BIT 24	PARTITION 12	1100
A14	BIT 24	PARTITION 13	1101
A15	BIT 24	PARTITION 14	1110
A16	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C, –40°C to +85°C for IND parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1645Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1645AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 10% for DS1645Y)
(t_A: See Note 10) (V_{CC}=5V ± 5% for DS1645AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	14
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1645Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1645AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1645AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1645Y)

PARAMETER	SYMBOL	DS1645Y-70 DS1645AB-70		DS1645Y-85 DS1645AB-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		ns	
Access Time	t_{ACC}		70		85	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		45	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		85	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		85		ns	
Write Pulse Width	t_{WP}	55		65		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	10 10		10 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		30	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		35		ns	4
Data Hold Time	t_{DH1} t_{DH2}	5 5		5 5		ns ns	12 13

PARAMETER	SYMBOL	DS1645Y-100 DS1645AB-100		DS1645Y-120 DS1645AB-120		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	100		120		ns	
Access Time	t_{ACC}		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		120		ns	
Write Pulse Width	t_{WP}	75		90		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	10 10		10 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	40		50		ns	4
Data Hold Time	t_{DH1} t_{DH2}	5 5		5 5		ns ns	12 13

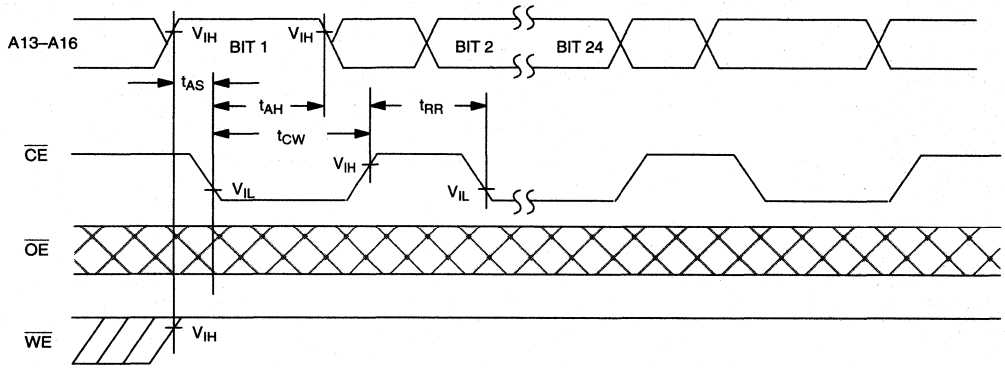
AC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CCI}=4.50V to 5.50V)*

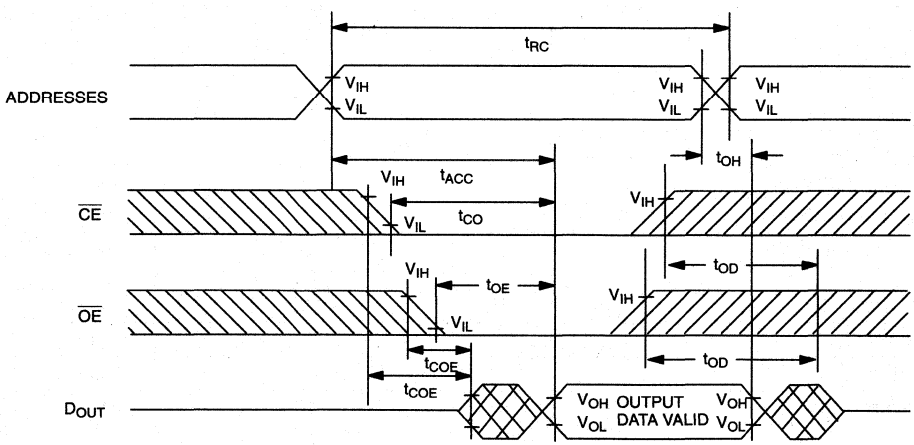
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	10			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

*For loading partition register

TIMING DIAGRAM: LOADING PARTITION REGISTER



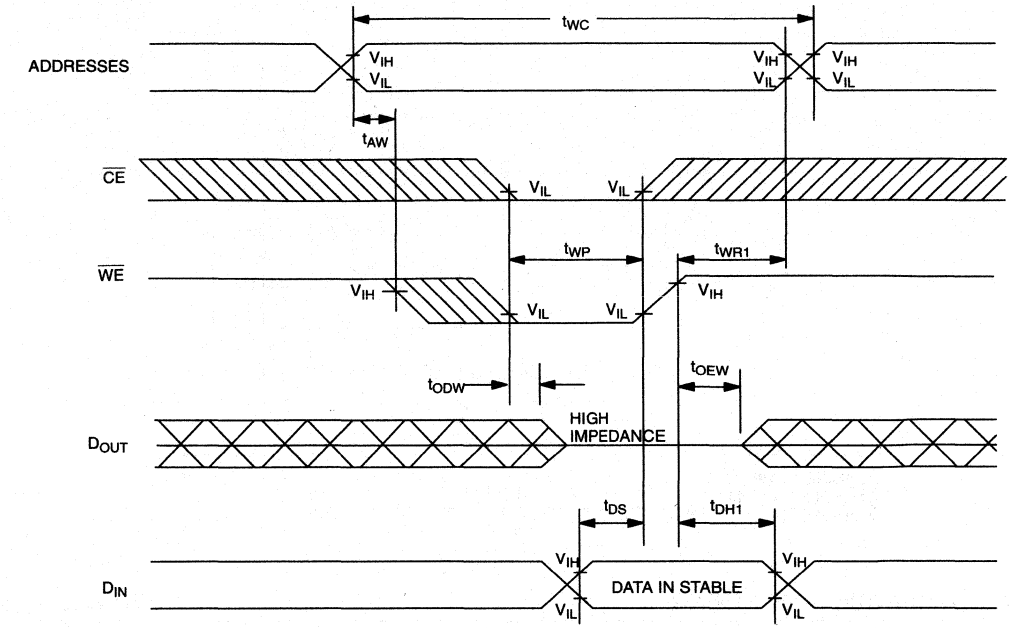
READ CYCLE



SEE NOTE 1

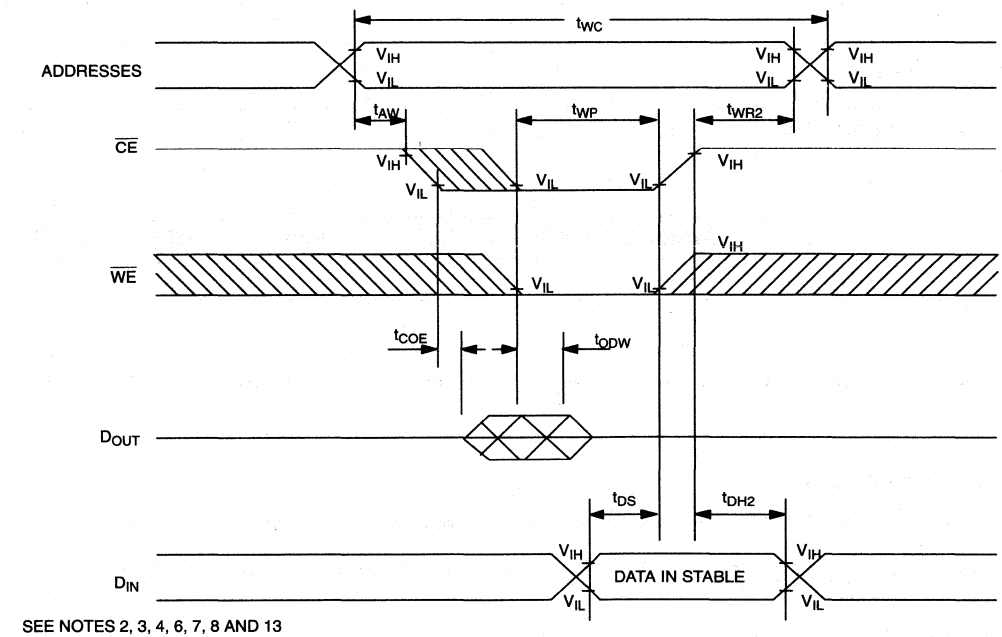
2

WRITE CYCLE 1



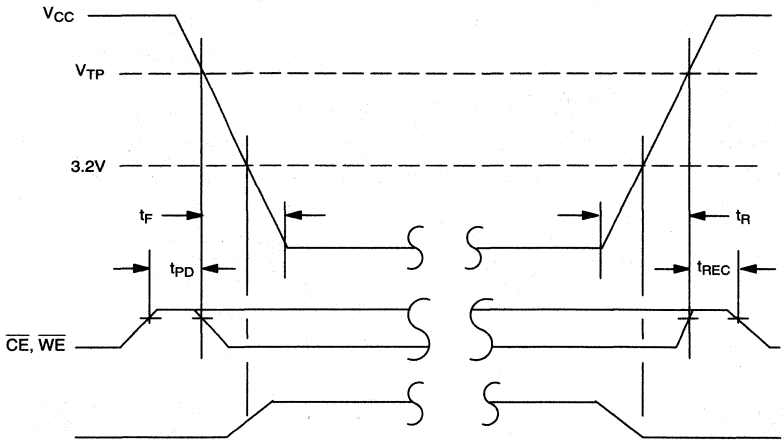
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to V_{tp} ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power-Up	t_{REC}	25		125	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1645 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C for industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
14. The power fail output signal ($\overline{PFO}$) is driven active (V_{OL}=0.4V) when the V_{CC} trip point occurs. While active, the $\overline{PFO}$ pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of $\overline{PFO}$ is 2.4 volts minimum and will source a current of 1 mA. This signal is only present on the LPM package variations.
15. DS1645 modules are recognized by Underwriters Laboratory (U.L.®) under file E99151(R).

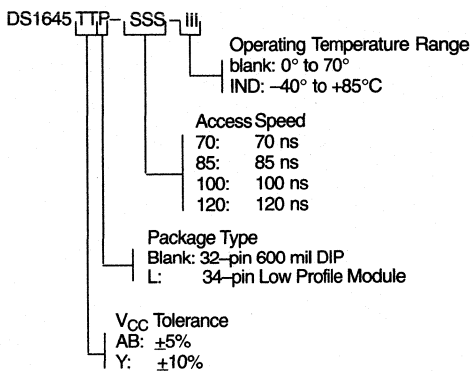
DC TEST CONDITIONS

Outputs Open
t Cycle = 200 ns
All voltages are referenced to ground

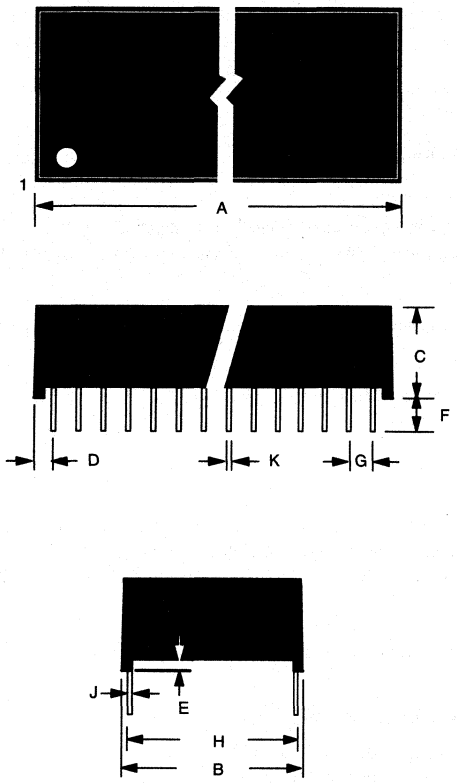
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION

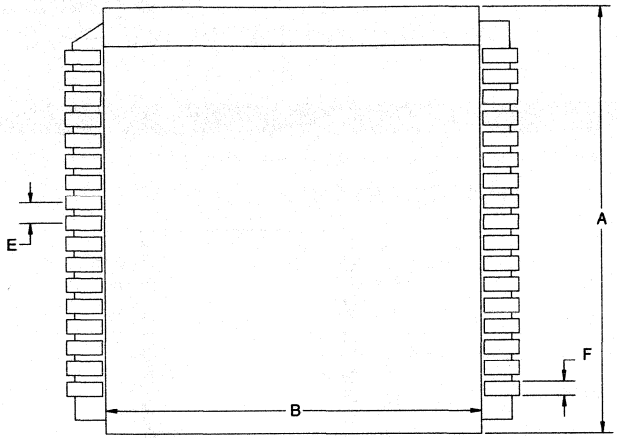


DS1645Y/AB NONVOLATILE SRAM, 32–PIN 740 MIL EXTENDED MODULE

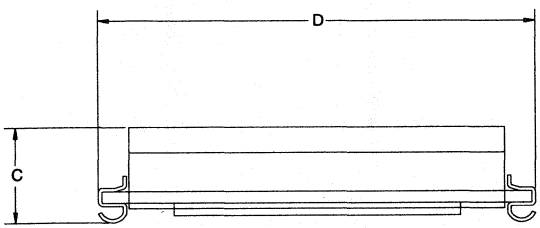


PKG	32-PIN	
DIM	MIN	MAX
A IN.	1.680	1.700
MM	42.67	43.18
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.355	0.375
MM	9.02	9.52
D IN.	0.080	0.110
MM	2.03	2.79
E IN.	0.015	0.025
MM	0.38	0.63
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1645Y/AB 34–PIN LOW PROFILE MODULE (LPM)



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.047	0.053
F	0.015	0.025



Suggested 68–pin PLCC surface mountable sockets with leads on two sides only are:

McKenzie	34P–SMT–3
Harwin	HIS–40001–04
Robinson Nugent	PLCC–34–SMT
Dallas Semiconductor	DS34PIN–PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.

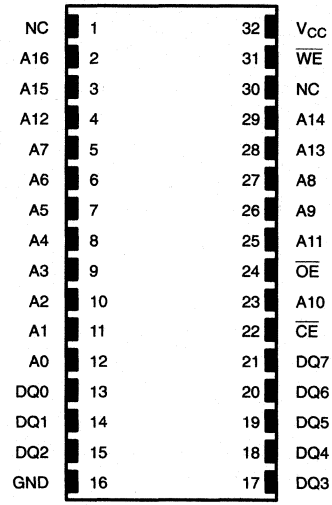
DALLAS SEMICONDUCTOR

DS1645EE
Partitioned 1024K NV SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 128K x 8 EPROM, EEPROM, or FLASH
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in either 70, 85, or 100 ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
(740 MIL EXTENDED)

PIN DESCRIPTION

A0 - A16	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ0 - DQ7	-	Data In/Data Out
V_{CC}	-	Power (+5V)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
NC	-	No Connect

DESCRIPTION

The DS1645EE 1024K Nonvolatile SRAM is a 1,048,576-bit, fully static, nonvolatile SRAM organized as 131,072 words by 8 bits. The DS1645EE has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The nonvolatile static RAM can be used in place of existing 128K x 8 EPROM, EEPROM or FLASH conforming to the popular bytewide 32 pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface. This part is functionally equivalent to the DS1645Y and differs only in pinout. See the DS1645Y/AB 1024K NV SRAM data sheet for technical details.

DALLAS SEMICONDUCTOR

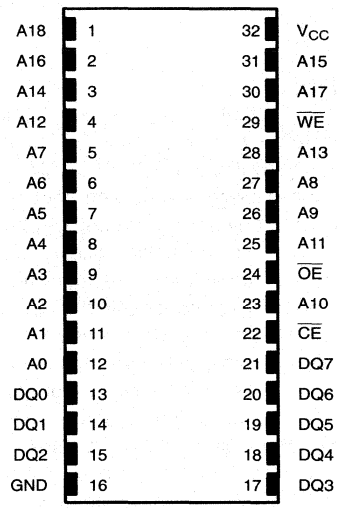
DS1650Y/AB
Partitionable 4096K NV SRAM

2

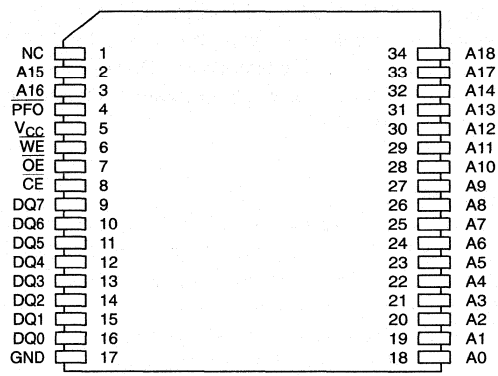
FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 512K x 8 volatile static RAM
- Write protects selected blocks of memory when programmed
- Unlimited write cycles
- Low-power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1650Y)
- Optional ±5% V_{CC} operating range (DS1650AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND
- JEDEC standard 32-pin DIP package
- Low Profile Module (LPM) package
  - Fits into standard 68–pin PLCC surface mountable socket
  - 255 mils package height
  - Power Fail Output ($\overline{PFO}$) warns system of impending V_{CC} power failure

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED



34–PIN LOW PROFILE MODULE (LPM)

PIN DESCRIPTION

A0 - A18	–	Address Inputs
DQ0 - DQ7	–	Data In/Data Out
$\overline{CE}$	–	Chip Enable
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
$\overline{PFO}$	–	Power Fail Output (LPM only)
V_{CC}	–	Power (+5V)
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS1650 4096K Nonvolatile SRAMs are 4,194,304-bit, fully static, nonvolatile SRAM organized as 524,288 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. In addition, the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt programs and important data. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing. DIP–package DS1650 devices can be used in place of existing 512K x 8 SRAMs directly conforming to the popular bytewide 32–pin DIP standard. DS1650 devices in the Low Profile Module package are specifically designed for surface mount applications. DS1650 LPM devices also have an additional pin, a Power Fail Outputs that can be used to warn a system of impending V_{CC} power failure.

READ MODE

The DS1650 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 19 address inputs (A_0 - A_{18}) defines which of the 524,288 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1650 devices execute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1650AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1650Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvoltile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1650AB and 4.5 volts for the DS1650Y.

FRESHNESS SEAL

Each DS1650 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

PARTITION PROGRAMMING MODE

The register controlling the partitioning logic is selected by recognition of a specific binary pattern which is sent on address lines A15 - A18. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycles will load the partition register. Since there are 16 protectable partitions, the size of each partition is 512K/16 or 32K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycles as defined by A15 through A18 and shown in Table 2. A logical 1 in a bit location write protects the corresponding partition. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A16 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1650 devices to internally inhibit $\overline{WE}$ for all write accesses where A18 A17 A16 A15=0101. Note that while programming the partition register, data which is being accessed from the RAM should be ignored, since the purpose of the 24 read cycles is to program the partition register, not to access data from RAM.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A15	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A16	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A17	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A18	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST BITS ENTERED

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{18} A_{17} A_{16} A_{15})
A15	BIT 21	PARTITION 0	0000
A16	BIT 21	PARTITION 1	0001
A17	BIT 21	PARTITION 2	0010
A18	BIT 21	PARTITION 3	0011
A15	BIT 22	PARTITION 4	0100
A16	BIT 22	PARTITION 5	0101
A17	BIT 22	PARTITION 6	0110
A18	BIT 22	PARTITION 7	0111
A15	BIT 23	PARTITION 8	1000
A16	BIT 23	PARTITION 9	1001
A17	BIT 23	PARTITION 10	1010
A18	BIT 23	PARTITION 11	1011
A15	BIT 24	PARTITION 12	1100
A16	BIT 24	PARTITION 13	1101
A17	BIT 24	PARTITION 14	1110
A18	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C, –40°C to +85°C for IND parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1650Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1650AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 10% for DS1650Y)
(t_A: See Note 10) (V_{CC}=5V ± 5% for DS1650AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	14
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1650Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1650AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1650AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1650Y)

PARAMETER	SYMBOL	DS1650Y-70 DS1650AB–70		DS1650Y–85 DS1650AB–85		DS1650Y-100 DS1650AB–100		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		100		ns	
Access Time	t_{ACC}		70		85		100	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		45		50	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		85		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	70		85		100		ns	
Write Pulse Width	t_{WP}	55		65		75		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	10 10		10 10		10 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		30		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	30		35		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	5 5		5 5		5 5		ns ns	12 13

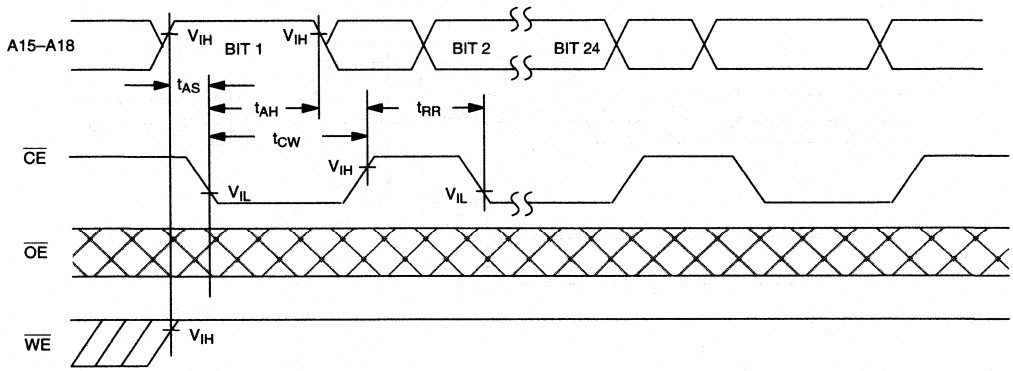
AC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CCI}=4.50V to 5.50V)*

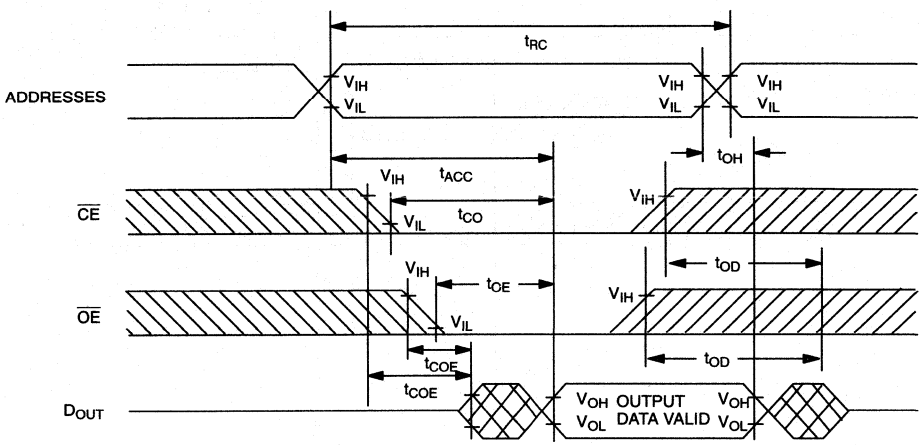
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	10			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

*For loading partition register

TIMING DIAGRAM: LOADING PARTITION REGISTER

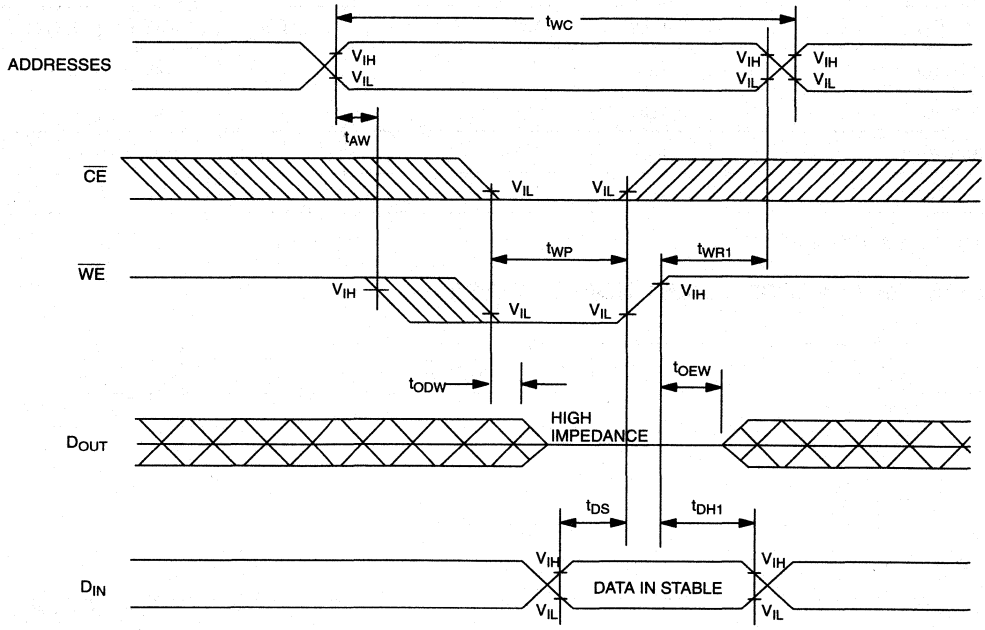


READ CYCLE



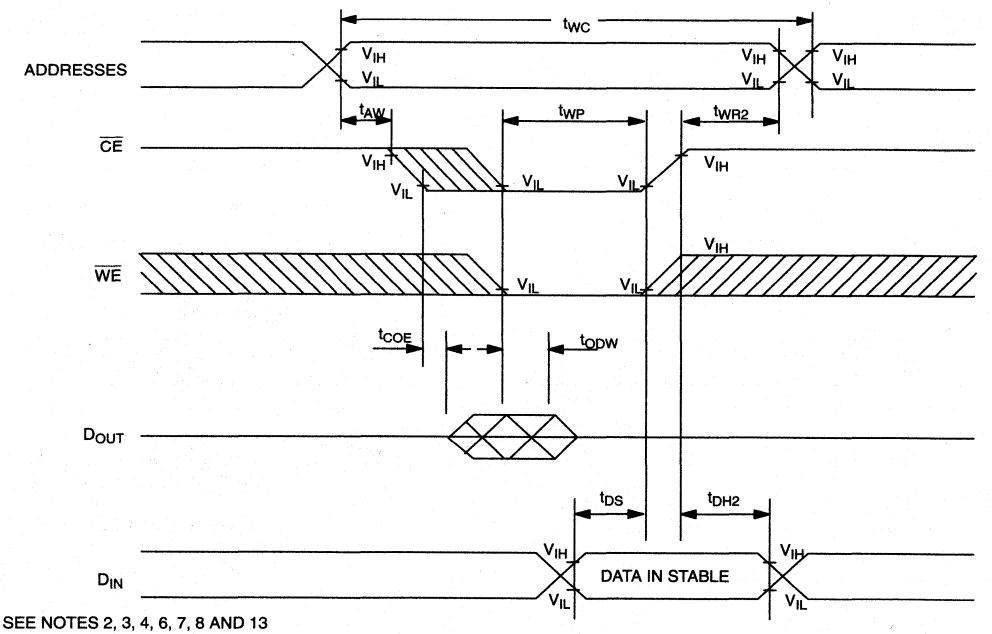
SEE NOTE 1

WRITE CYCLE 1



SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

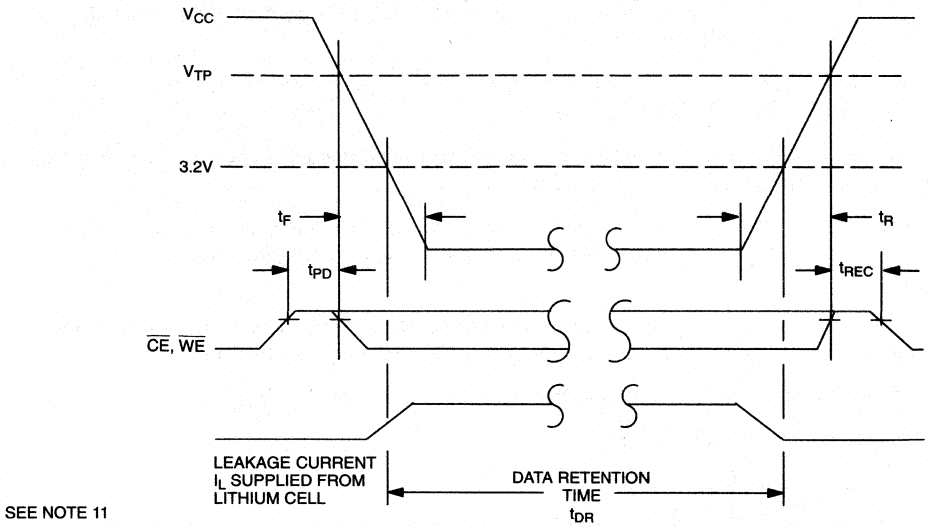
WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

2

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power-Up	t_{REC}	25		125	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1650 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
14. The power fail output signal ($\overline{PFO}$) is driven active (V_{OL}=0.4V) when the V_{CC} trip point occurs. While active, the $\overline{PFO}$ pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of $\overline{PFO}$ is 2.4 volts minimum and will source a current of 1 mA. This signal is only present on the LPM package variations.
15. DS1650 modules are recognized by Underwriters Laboratory (U.L.®) under file E99151(R).

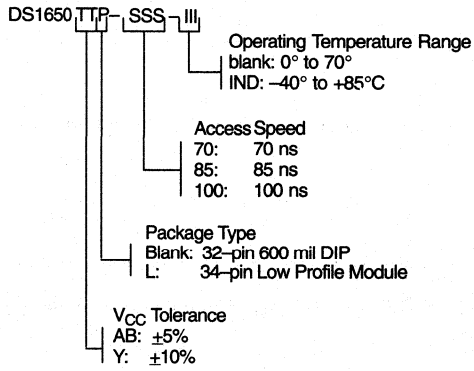
DC TEST CONDITIONS

Outputs Open
t Cycle = 200 ns
All voltages are referenced to ground

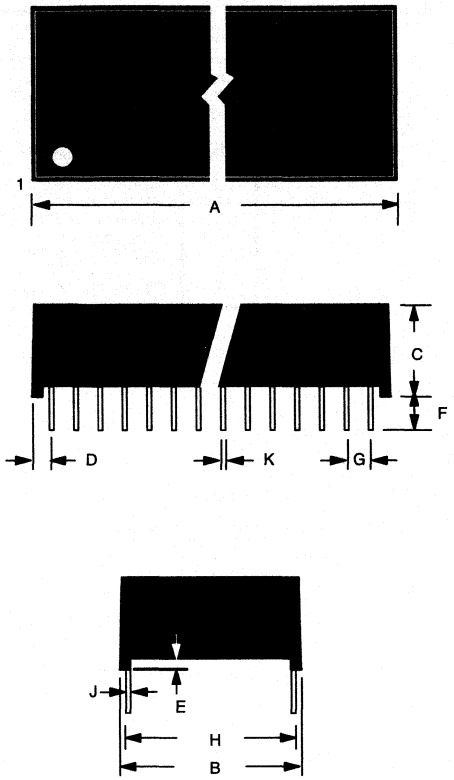
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION

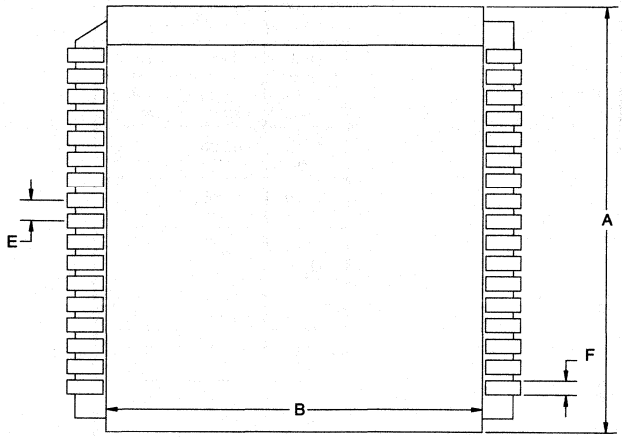


DS1650Y/AB NONVOLATILE SRAM, 32–PIN 740 MIL EXTENDED MODULE

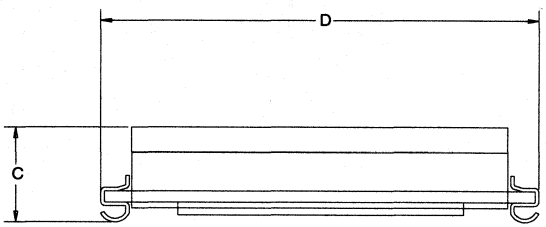


PKG	32-PIN	
DIM	MIN	MAX
A IN.	1.680	1.700
MM	42.67	43.18
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.355	0.375
MM	9.02	9.52
D IN.	0.080	0.110
MM	2.03	2.79
E IN.	0.015	0.025
MM	0.38	0.63
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1650Y/AB 34–PIN LOW PROFILE MODULE (LPM)



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.047	0.053
F	0.015	0.025



Suggested 68–pin PLCC surface mountable sockets with leads on two sides only are:

McKenzie	34P–SMT–3
Harwin	HIS–40001–04
Robinson Nugent	PLCC–34–SMT
Dallas Semiconductor	DS34PIN–PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.

DALLAS SEMICONDUCTOR

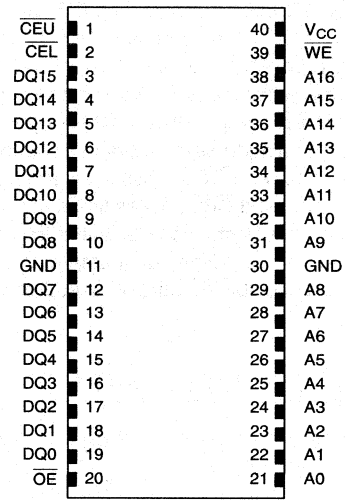
DS1658Y/AB
Partitionable 128K x 16 NV SRAM

2

FEATURES

- 10 year minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Write protects selected blocks of memory when programmed
- Separate upper byte and lower byte chip selection inputs
- Unlimited write cycles
- Low–power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1658Y)
- Optional ±5% V_{CC} operating range (DS1658AB)
- Optional industrial temperature range of –40°C to 85°C (designated IND)

PIN ASSIGNMENT



40–PIN EXCAPSULATED PACKAGE
740 MIL EXTENDED

PIN DESCRIPTION

A0–A16	–	Address Inputs
DQ0–DQ15	–	Data In/Data Out
$\overline{CEU}$	–	Chip Enable Upper Byte
$\overline{CEL}$	–	Chip Enable Lower Byte
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
V_{CC}	–	Power Supply (+5V)
GND	–	Ground

DESCRIPTION

The DS1658 128K x 16 NV SRAMs are 2,097,152 bit fully static, nonvolatile SRAMs, organized as 131,072 words by 16 bits. Each NV SRAM has a self contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out–of–tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. In addition, the DS1658 has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt programs and important data. DS1658 devices can be used in place of solutions which build nonvolatile 128K x 16 memory by utilizing a variety of discrete components. There is no limit on the number of write cycles that can be executed, and no additional support circuitry is required for microprocessor interfacing.

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READ MODE

The DS1658 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high), either/both of $\overline{CEU}$ or $\overline{CEL}$ (Chip Enables) are active (low) and $\overline{OE}$ (Output Enable) is active low. The unique address specified by the 17 address inputs (A0–A16) defines which of the 131,072 words of data is to be accessed. The status of $\overline{CEU}$ and $\overline{CEL}$ determines whether all or part of the addressed word is accessed. If $\overline{CEU}$ is active with $\overline{CEL}$ inactive, then only the upper byte of the addressed word is accessed. If $\overline{CEU}$ is inactive with $\overline{CEL}$ active, then only the lower byte of the addressed word is accessed. If both the $\overline{CEU}$ and $\overline{CEL}$ inputs are active (low), then the entire 16 bit word is accessed. Valid data will be available to the 16 data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CEU}$, $\overline{CEL}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$, $\overline{CEU}$, and $\overline{CEL}$ access times are not satisfied, then data access must be measured from the later occuring signal, and the limiting parameter is either t_{CO} for $\overline{CEU}$, $\overline{CEL}$, or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1658 devices execute a write cycle whenever $\overline{WE}$ and either/both of $\overline{CEU}$ or $\overline{CEL}$ are active (low) after address inputs are stable. The unique address specified by the 17 address inputs (A0–A16) defines which of the 131,072 words of data is accessed. The status of $\overline{CEU}$ and $\overline{CEL}$ determines whether all or part of the addressed word is accessed. If $\overline{CEU}$ is active with $\overline{CEL}$ inactive, then only the upper byte of the addressed word is accessed. If $\overline{CEU}$ is inactive with $\overline{CEL}$ active, then only the lower byte of the addressed word is accessed. If both the $\overline{CEU}$ and $\overline{CEL}$ inputs are active (low), then the entire 16–bit word is accessed. The write cycle is terminated by the earlier rising edge of $\overline{CEU}$ and/or $\overline{CEL}$, or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CEU}$ and/or $\overline{CEL}$, and $\overline{OE}$ active) then $\overline{WE}$ will disable outputs in t_{ODW} from its falling edge.

READ/WRITE FUNCTION Table 1

$\overline{OE}$	$\overline{WE}$	$\overline{CEL}$	$\overline{CEU}$	V_{CC} CURRENT	DQ0–DQ7	DQ8–DQ15	CYCLE PERFORMED
H	H	X	X	I_{CCO}	High–Z	High–Z	Output Disabled
L	H	L	L	I_{CCO}	Output	Output	Read Cycle
L	H	L	H		Output	High–Z	
L	H	H	L		High–Z	Output	
X	L	L	L	I_{CCO}	Input	Input	Write Cycle
X	L	L	H		Input	High–Z	
X	L	H	L		High–Z	Input	
X	X	H	H	I_{CCS}	High–Z	High–Z	Output Disabled

DATA RETENTION MODE

The DS1658AB provides full functional capability for V_{CC} greater than 4.75 volts, and write protects by 4.5 volts. The DS1658Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1658AB and 4.5 volts for the DS1658Y.

FRESHNESS SEAL

Each DS1658 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied and remains at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

PARTITION PROGRAMMING MODE

The register controlling the partitioning logic is selected by recognition of a specific binary pattern which is sent on address lines A13–A16. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles, using both $\overline{CEU}$ and $\overline{CEL}$, with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycles will load the partition register. Since there are 16 protectable partitions, the size of each partition is 128K/16 or 8K x 16. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycles as defined by A13 through A16 and shown in Table 2. A logical 1 in a bit location write protects the corresponding partition. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A14 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1658 devices to internally inhibit $\overline{WE}$ for all write acesses where A16 A15 A14 A13=0101. Note that while programming the partition register, data which is being accessed from the RAM should be ignored, since the purpose of the 24 read cycles is to program the partition register, not to read data from RAM.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 2

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A13	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A14	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A15	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A16	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST BITS ENTERED

PARTITION REGISTER MAPPING Table 3

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{16} A_{15} A_{14} A_{13})
A13	BIT 21	PARTITION 0	0000
A14	BIT 21	PARTITION 1	0001
A15	BIT 21	PARTITION 2	0010
A16	BIT 21	PARTITION 3	0011
A13	BIT 22	PARTITION 4	0100
A14	BIT 22	PARTITION 5	0101
A15	BIT 22	PARTITION 6	0110
A16	BIT 22	PARTITION 7	0111
A13	BIT 23	PARTITION 8	1000
A14	BIT 23	PARTITION 9	1001
A15	BIT 23	PARTITION 10	1010
A16	BIT 23	PARTITION 11	1011
A13	BIT 24	PARTITION 12	1100
A14	BIT 24	PARTITION 13	1101
A15	BIT 24	PARTITION 14	1110
A16	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to 7.0V
Operating Temperature	0°C to +70°C, –40°C to +85°C for IND parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1658Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1658AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1658AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1658Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-2.0		+2.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CEU}$, $\overline{CEL}$=2.2V	I_{CCS1}		10	20	mA	
Standby Current $\overline{CEU}$, $\overline{CEL}$=V_{CC} - 0.5V	I_{CCS2}		6	10	mA	
Operating Current	I_{CCO1}			170	mA	
Write Protection Voltage (DS1658Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (ds1658AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		20	25	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1658AB)
(t_A: See Note 10) (V_{CC}=5V ± 10% for DS1658Y)

PARAMETER	SYMBOL	DS1658Y–70 DS1658AB–70		DS1658Y–100 DS1658AB–100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Access Time	t_{ACC}		70		100	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		50	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		100		ns	
Write Pulse Width	t_{WP}	55		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	10 10		10 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	5 5		5 5		ns ns	12 13

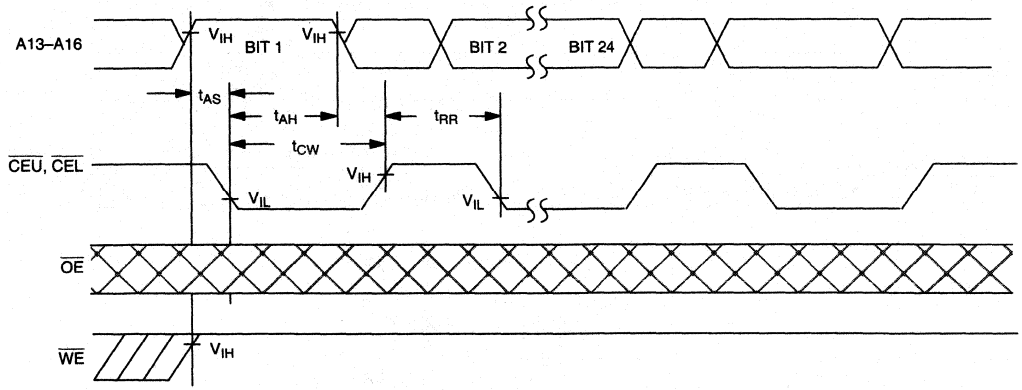
AC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CC}=4.5V to 5.5V)*

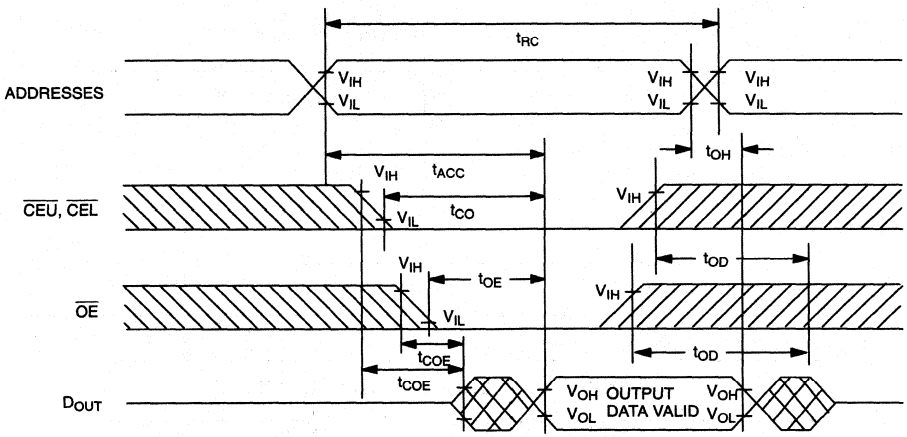
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	20			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

*For loading partition register

TIMING DIAGRAM: LOADING PARTITION REGISTER

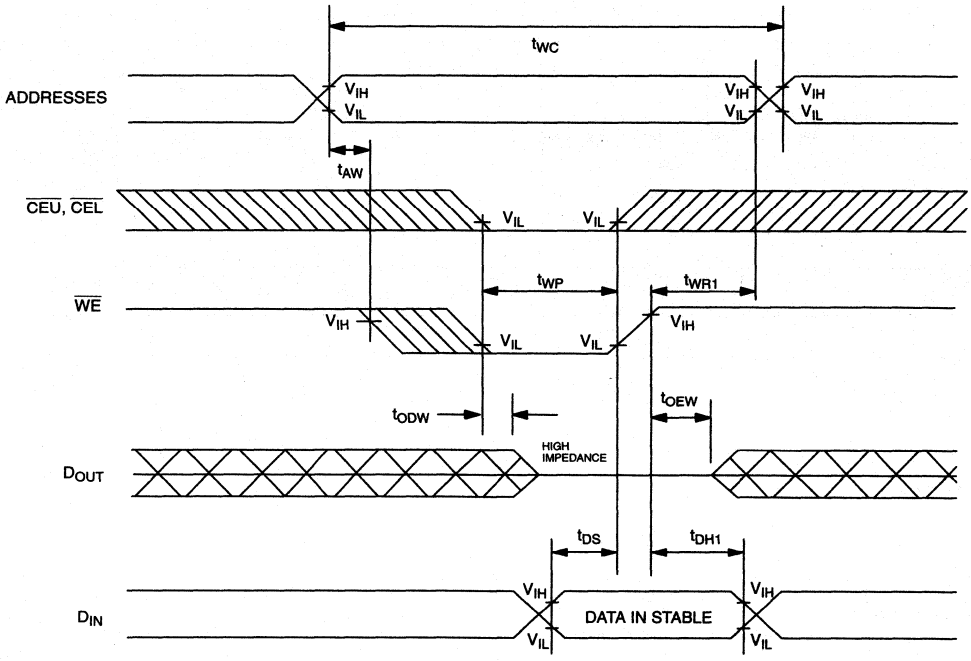


READ CYCLE



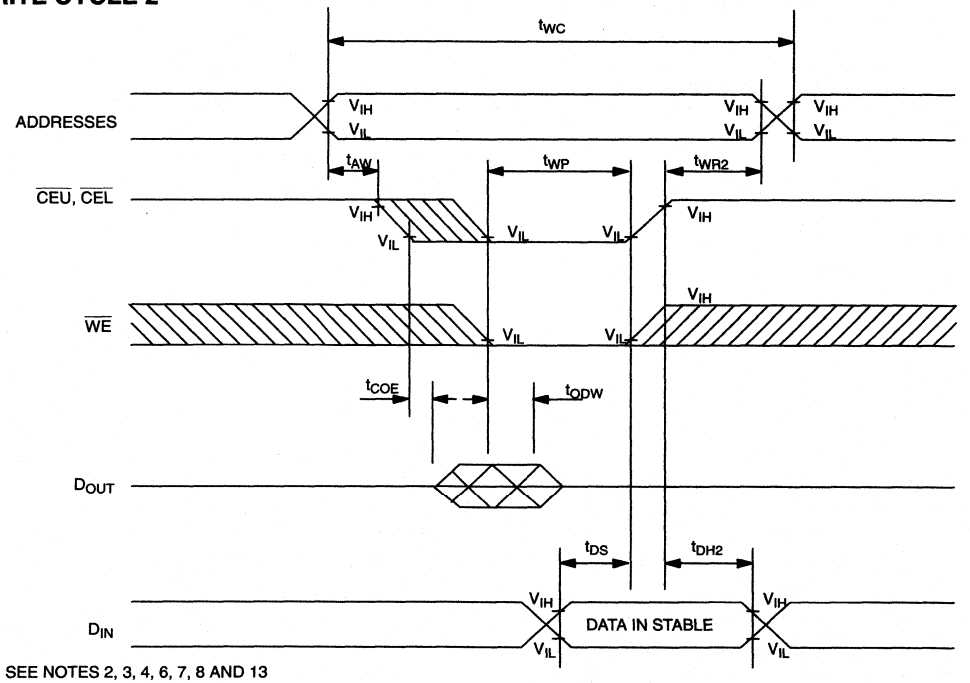
SEE NOTE 1

WRITE CYCLE 1



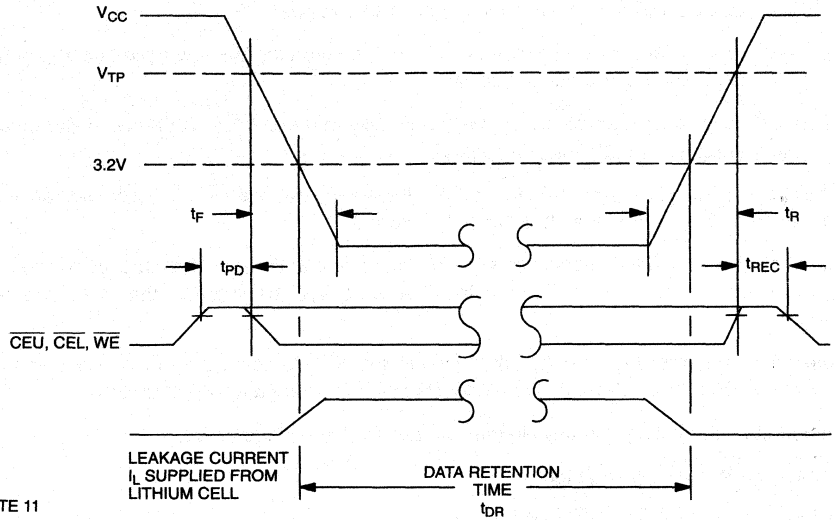
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEU}$, $\overline{CEL}$, $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} Slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CEU}$, $\overline{CEL}$, $\overline{WE}$ at V_{IH} after Power-Up	t_{REC}	25		125	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CEU}$ or $\overline{CEL}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CEU}$, $\overline{CEL}$ or $\overline{WE}$ going low to the earlier of $\overline{CEU}$, $\overline{CEL}$ or $\overline{WE}$ going high.

4. t_{DS} is measured from the earlier of $\overline{CEU}$ or $\overline{CEL}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CEU}$ or $\overline{CEL}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CEU}$ or $\overline{CEL}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CEU}$ or $\overline{CEL}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1658 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CEU}$ OR $\overline{CEL}$ going high.

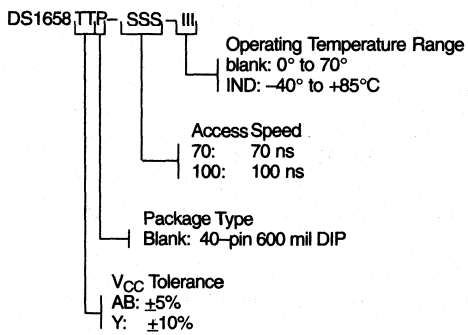
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All voltages are referenced to ground

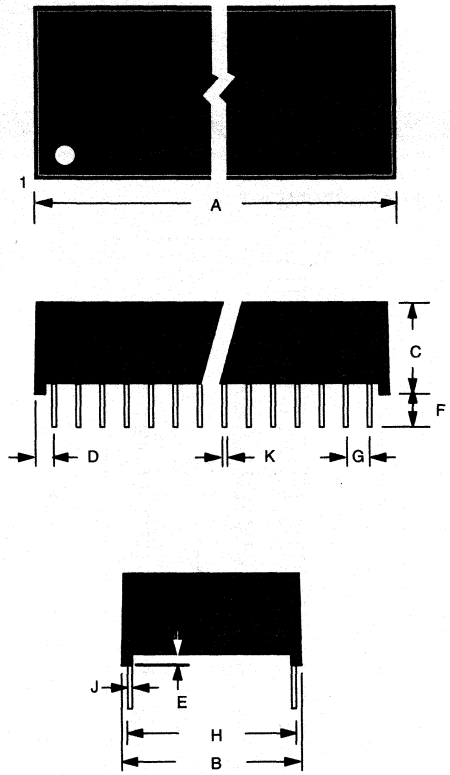
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels:
  0.0 to 3.0 volts
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION



DS1658Y/AB NONVOLATILE SRAM, 40–PIN 740 MIL EXTENDED MODULE



PKG	40-PIN	
DIM	MIN	MAX
A IN. MM	2.080 52.83	2.100 53.34
B IN. MM	0.715 18.16	0.740 18.80
C IN. MM	0.345 8.76	0.365 9.27
D IN. MM	0.085 2.16	0.115 2.92
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.120 3.05	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.43	0.025 0.58

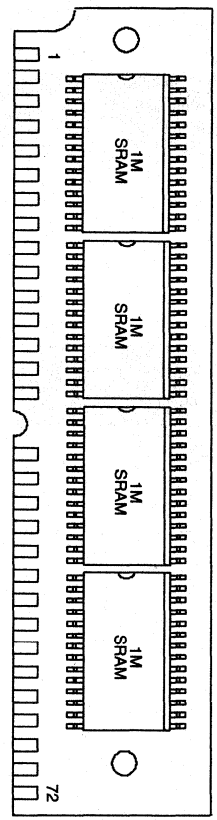
DALLAS SEMICONDUCTOR

DS2227
Flexible NV SRAM Stik

FEATURES

- Flexibly organized as 128K x 32, 256K x 16, or 512K x 8 bits
- Data retention >10 years in the absence of V_{CC}
- Nonvolatile circuitry transparent to and independent from host system
- Automatic write protection circuitry safeguards against data loss
- Separate chip enables allow access by byte, word, or long word
- Fast access times: 70ns, 100ns, or 120ns
- Unlimited write cycles
- Read cycle time equals write cycle time
- Employs popular JEDEC standard 72-position SIMM connection scheme
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time

PIN ASSIGNMENT



72-PIN SIP STIK

DESCRIPTION

The DS2227 Flexible NV SRAM Stik is a self-contained 4,194,304-bit nonvolatile static RAM which can be flexibly organized as 128K x 32 bits, 256K x 16 bits, or 512K x 8 bits. The nonvolatile memory contains all necessary control circuitry and lithium energy sources to maintain data integrity in the absence of power for more than 10 years. The DS2227 employs the popular JEDEC standard 72-position SIMM connection scheme requiring no additional circuitry.

OPERATION

The DS2227 Flexible NV SRAM Stik is used like any standard static RAM. All nonvolatile circuitry is transparent to the user. The flexibility of the part is achieved by providing separate read, write, and chip select pins for each of the four banks of onboard memories (see Figure 1). For operation as a 512K x 8 NV SRAM Stik, tie all data lines from each bank together (i.e., all D0s together, all D1s together, etc.). Read enables and write enables are also tied together. For operation as a 256K x 16 NV SRAM Stik, tie the data lines from two banks together. Chip enables, read enables, and write enables from these banks are also tied together. Connection to the DS2227 is made by using an industry-standard, 72-position SIMM socket DS9072-72V (AMP part number 821824-8). These SIMM sockets are also available in perpendicular, inclined, or parallel mount, depending on the height available. See the DS907x SipStik™ connectors available from Dallas Semiconductor.

READ MODE

The DS2227 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 17 address inputs (A_0 - A_{16}) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS2227 is in the write mode whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs to t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS2227 provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS2227 constantly monitors V_{CC}. Should the supply voltage decay, the NV SRAM automatically write-protects itself, all inputs become "don't care" and all outputs become high impedence. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS2227 checks lithium status to warn of potential data loss. Each time that V_{CC} power is restored to the DS2227, the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory access to the device is inhibited. Battery status can, therefore, be determined by a three–step process. First, a read cycle is performed to any location in memory, in order to save the contents of that location. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, then the battery voltage is less than 2.0V and data is in danger of being corrupted.

The DS2227 also provides battery redundancy. In many applications data integrity is paramount. The DS2227 provides two batteries for each SRAM and an internal isolation switch to select between them. During battery backup, the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user.

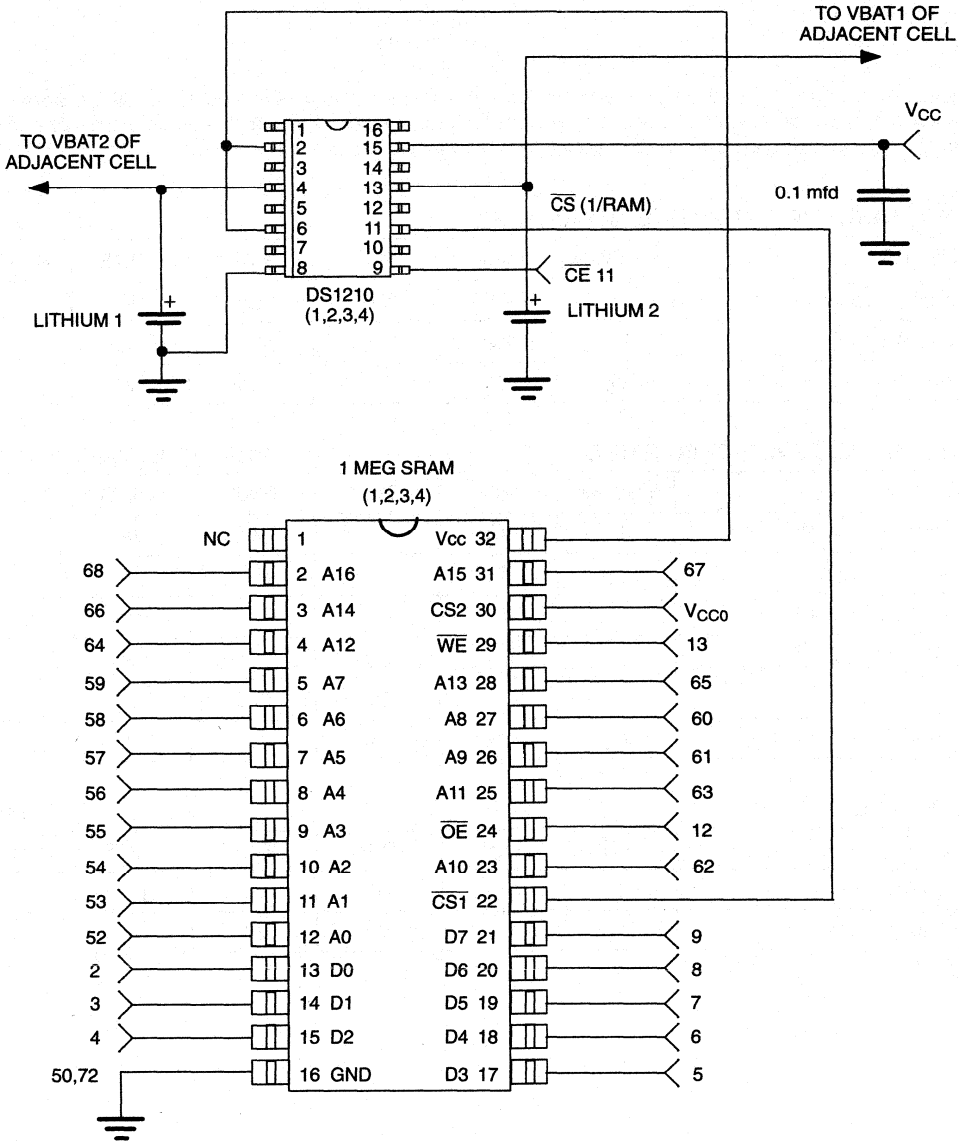
PIN DESCRIPTION Table 1

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	V_{CC}	38	4-D0
2	1-D0	39	4-D1
3	1-D1	40	4-D2
4	1-D2	41	4-D3
5	1-D3	42	4-D4
6	1-D4	43	4-D5
7	1-D5	44	4-D6
8	1-D6	45	4-D7
9	1-D7	46	NC
10	NC	47	4-$\overline{CE}$
11	1-$\overline{CE}$	48	4-$\overline{OE}$
12	1-$\overline{OE}$	49	4-$\overline{WE}$
13	1-$\overline{WE}$	50	GND
14	2-D0	51	V_{CC}
15	2-D1	52	A0
16	2-D2	53	A1
17	2-D3	54	A2
18	2-D4	55	A3
19	2-D5	56	A4
20	2-D6	57	A5
21	2-D7	58	A6
22	NC	59	A7
23	2-$\overline{CE}$	60	A8
24	2-$\overline{OE}$	61	A9
25	2-$\overline{WE}$	62	A10
26	3-D0	63	A11
27	3-D1	64	A12
28	3-D2	65	A13
29	3-D3	66	A14
30	3-D4	67	A15
31	3-D5	68	A16
32	3-D6	69	NC
33	3-D7	70	NC
34	NC	71	NC
35	3-$\overline{CE}$	72	GND
36	3-$\overline{OE}$		
37	3-$\overline{WE}$		

NOTE: Leave all pins marked as NC unconnected.

2

SCHEMATIC (1 CELL) Figure 1



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40° to +85°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LO}	-5.0		+5.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA	
Operating Current	I_{CC}		60	280	mA	
Write Protection Voltage	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

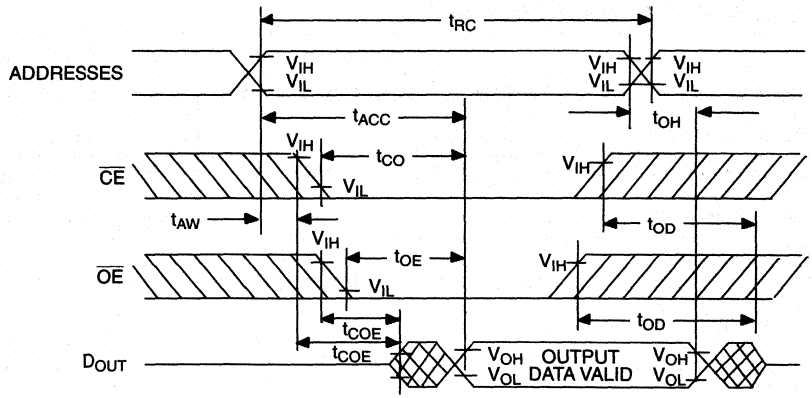
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		20	40	pF	
Output Capacitance	C_{OUT}		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

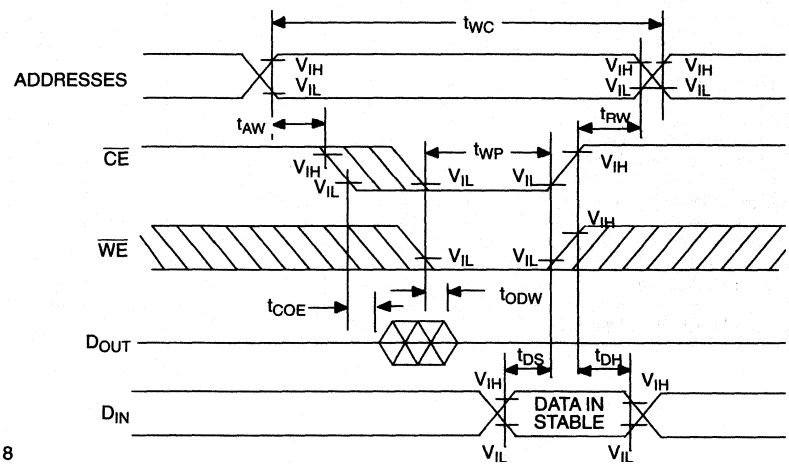
PARAMETER	SYMBOL	DS2227-70		DS2227-100		DS2227-120		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		120		ns	10
Access Time	t_{ACC}		70		100		120	ns	10
$\overline{OE}$ to Output Valid	t_{OE}		35		50		60	ns	10
$\overline{CE}$ to Output Valid	t_{CO}		70		100		120	ns	10
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	10
Output High Z from Deselection	t_{OD}		25		35		40	ns	10
Output Hold from Address Change	t_{OH}	5		5		5		ns	10
Write Cycle Time	t_{WC}	70		100		120		ns	10
Write Pulse Width	t_{WP}	55		75		90		ns	3,10
Address Setup Time	t_{AW}	0		0		0		ns	10
Write Recovery Time	t_{WR}	20		20		20		ns	10
Output High Z from WE	t_{ODW}		25		35		40	ns	10
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	8,10
Data Setup Time	t_{DS}	30		40		50		ns	4,10
Data Hold Time from $\overline{WE}$	t_{DH}	20		20		20		ns	4,5,10

READ CYCLE



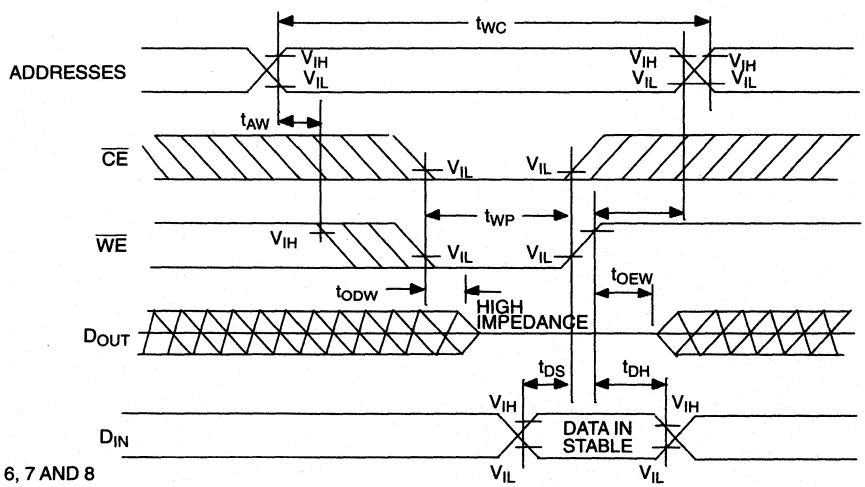
SEE NOTE 1

WRITE CYCLE 1



SEE NOTES 2, 3, 4, 5, 6, 7 AND 8

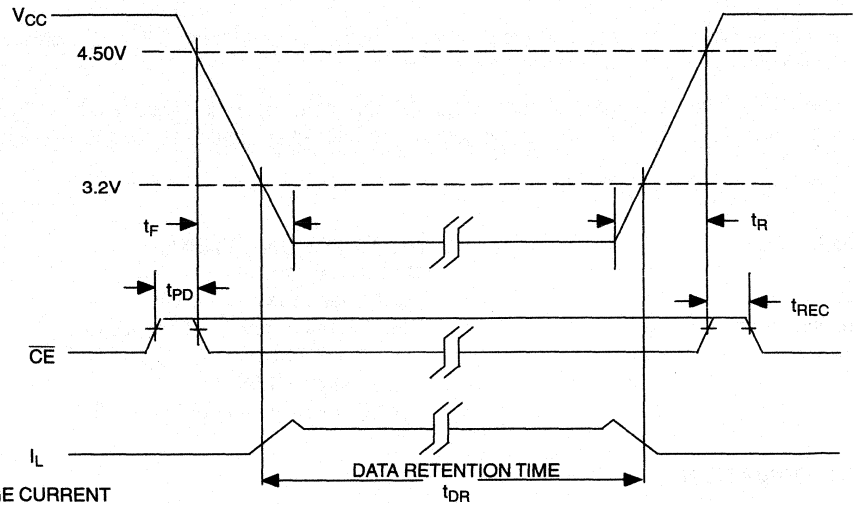
WRITE CYCLE 2



SEE NOTES 2, 3, 4, 5, 6, 7 AND 8

2

POWER-UP/POWER-DOWN CONDITION



POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} Before Power-down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 4.25V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-up	t_{REC}	2	80	125	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then t_{DH} = 20 ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.

7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.
8. If the $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state in this period.
9. Each DS2227 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The minimum expected t_{DR} is defined as starting at the date of manufacture.
10. Timings are valid only when $\overline{CE}$ is tied low.

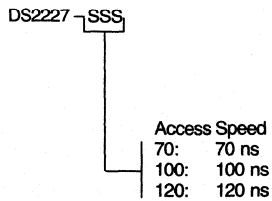
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All Voltages are Referenced to Ground

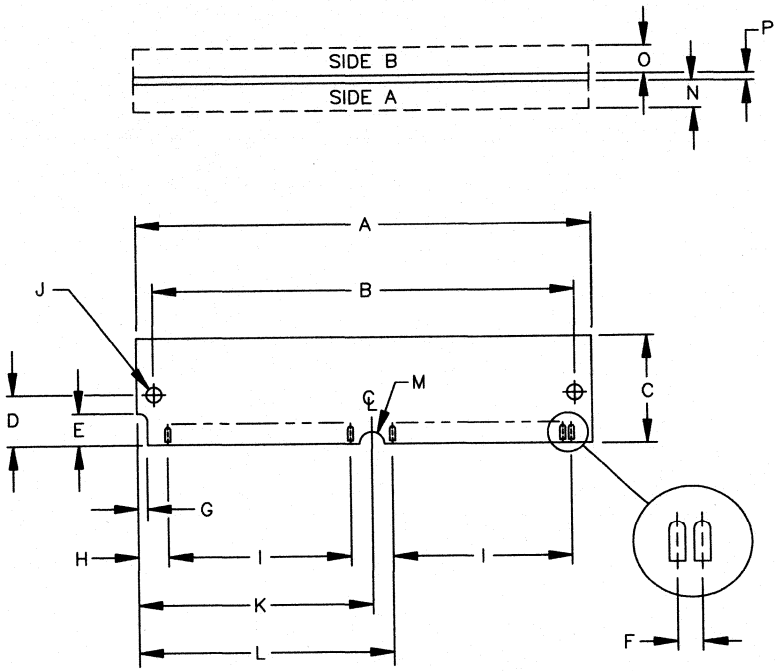
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL gate
Input Pulse Levels: 0 – 3.0 V
Timing Measurements Reference Levels:
Input - 1.5V
Output - 1.5V
Input Pulse Rise and Fall Times: 5ns

ORDERING INFORMATION



DS2227 72–PIN SIP STIK



DIM	72–PIN	
	MIN	MAX
A	4.245	4.255
B	3.979	3.989
C	0.845	0.855
D	0.395	0.405
E	0.245	0.255
F	0.050 BASIC	
G	0.075	0.085
H	0.245	0.255
I	1.750 BASIC	
J	0.120	0.130
K	2.120	2.130
L	2.245	2.255
M	0.057	0.067
N	–	0.140
O	–	0.140
P	–	0.054

NOTE: DIMENSIONS ARE SHOWN INCHES.

TIMEKEEPING

3

DALLAS SEMICONDUCTOR

DS1202, DS1202S
Serial Timekeeping Chip

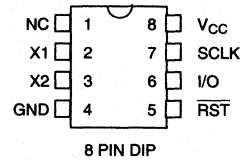
FEATURES

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation
- 24 x 8 RAM for scratchpad data storage
- Serial I/O for minimum pin count
- 2.0-5.5 volt full operation
- Uses less than 300 nA at 2 volts
- Single-byte or multiple-byte (burst mode) data transfer for read or write of clock or RAM data
- 8-pin DIP or optional 16-pin SOIC for surface mount
- Simple 3-wire interface
- TTL-compatible (V_{CC} = 5V)
- Optional industrial temperature range -40°C to +85°C

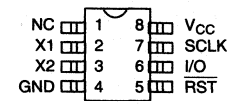
ORDERING INFORMATION

DS1202	8–pin DIP
DS1202S	16–pin SOIC
DS1202S8	8–pin SOIC

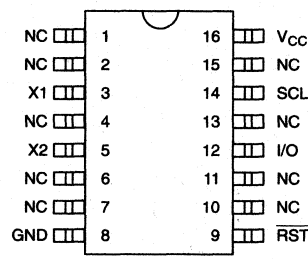
PIN ASSIGNMENT



8 PIN DIP



8–PIN SOIC
(208 mil)



16–PIN SOIC

PIN DESCRIPTION

NC	–	No Connection
X1, X2	–	32.768 KHz Crystal Input
GND	–	Ground
$\overline{RST}$	–	Reset
I/O	–	Data Input/Output
SCLK	–	Serial Clock
V_{CC}	–	Power Supply Pin

DESCRIPTION

The DS1202 Serial Timekeeping Chip contains a real time clock/calendar and 24 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Interfacing the DS1202 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: (1) $\overline{RST}$ (Reset), (2) I/O (Data line), and (3) SCLK (Serial clock). Data can be transferred to and from the clock/

RAM one byte at a time or in a burst of up to 24 bytes. The DS1202 is designed to operate on very low power and retain data and clock information on less than 1 microwatt.

OPERATION

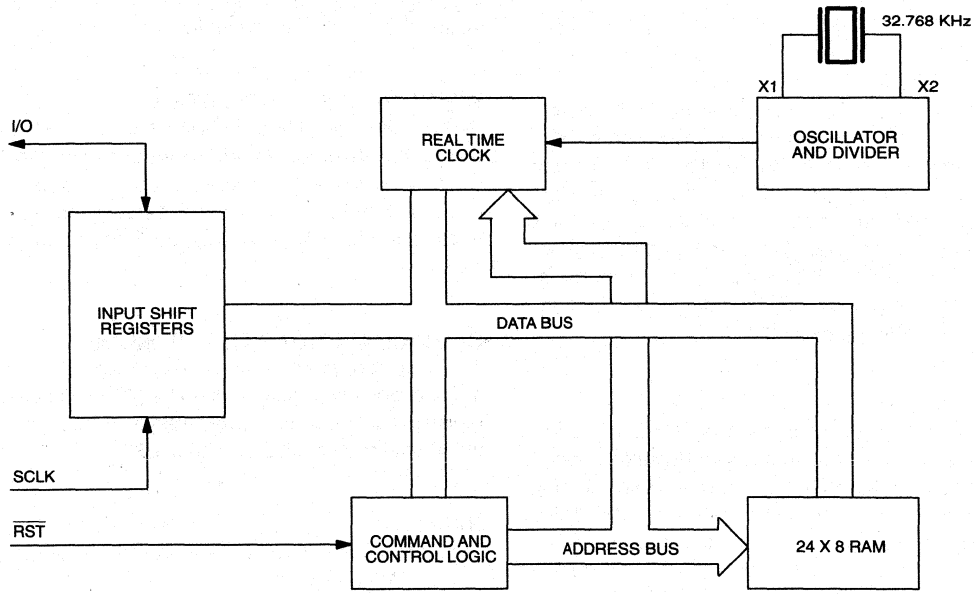
The main elements of the Serial Timekeeper are shown in Figure 1: shift register, control logic, oscillator, real time clock, and RAM. To initiate any transfer of data, $\overline{RST}$ is taken high and eight bits are loaded into the shift register providing both address and command information. Data is serially input on the rising edge of the SCLK. The first eight bits specify which of 32 bytes will be accessed, whether a read or write cycle will take place, and whether a byte or burst mode transfer is to occur. After the first eight clock cycles have occurred which load the command word into the shift register, additional clocks will output data for a read or input data for a write. The number of clock pulses equals eight plus eight for byte mode or eight plus up to 192 for burst mode.

COMMAND BYTE

The command byte is shown in Figure 2. Each data transfer is initiated by a command byte. The MSB (Bit 7) must be a logic 1. If it is zero, further action will be terminated. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits one through five specify the designated registers to be input or output, and the LSB (Bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

3

DS1202 BLOCK DIAGRAM Figure 1



ADDRESS/COMMAND BYTE Figure 2

7	6	5	4	3	2	1	0
1	RAM / $\overline{CK}$	A4	A3	A2	A1	A0	RD / $\overline{W}$

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves two functions. First, $\overline{RST}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{RST}$ signal provides a method of terminating either single byte or multiple byte data transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on t he falling edge of clock. All data transfer terminates if the $\overline{RST}$ input is low and the I/O pin goes to a high impedance state. Data transfer is illustrated in Figure 3.

DATA INPUT

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as $\overline{RST}$ remains high. This operation permits continuous burst mode read capability. Data is output starting with bit 0.

BURST MODE

Burst mode may be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits one through five = logical one). As before, bit six specified clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 8 through 31 in the Clock/Calendar Registers or locations 24 through 31 in the RAM registers. When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred.

However, when writing to RAM in burst mode it is not necessary to write all 24 bytes for the data to transfer. Each byte that is written to will be transferred to RAM regardless of whether all 24 bytes are written or not.

CLOCK/CALENDAR

The clock/calendar is contained in eight write/read registers as shown in Figure 4. Data contained in the clock/calendar registers is in binary coded decimal format (BCD).

CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock oscillator is stopped and the DS1202 is placed into a low-power standby mode with a current drain of not more than 100 nanoamps. When this bit is written to logic 0, the clock will start.

AM-PM/12-24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10 hour bit (20-23 hours).

WRITE PROTECT REGISTER

Bit 7 of write protect register is the write protect bit. The first seven bits (bits 0-6) are forced to zero and will always read a zero when read. Before any write operation to the clock or RAM, bit 7 must be zero. When high, the write protect bit prevents a write operation to any other register.

CLOCK/CALENDAR BURST MODE

The clock/calendar command byte specifies burst mode operation. In this mode the eight clock/calendar registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

RAM

The static RAM is 24 x 8 bytes addressed consecutively in the RAM address space.

RAM BURST MODE

The RAM command byte specifies burst mode operation. In this mode, the 24 RAM registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

REGISTER SUMMARY

A register data format summary is shown in Figure 4.

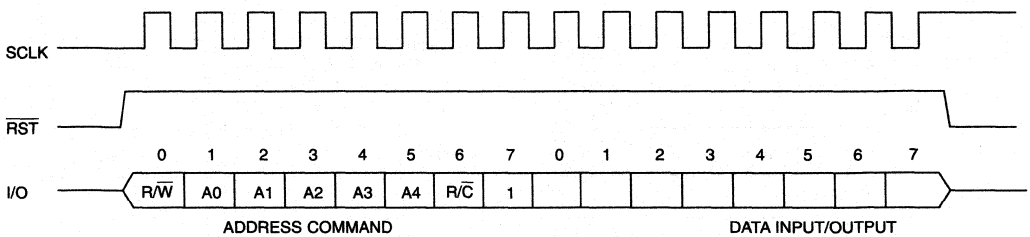
CRYSTAL SELECTION

A 32.768 KHz crystal, Daiwa Part No. DT26S, Seiko Part No. DS-VT-200 or equivalent, can be directly connected to the DS1202 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (CL) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks".

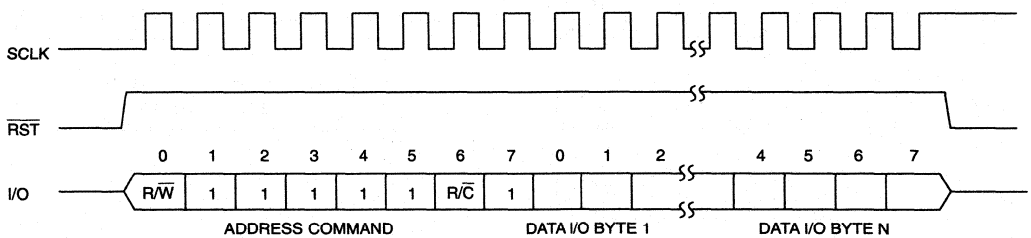
3

DATA TRANSFER SUMMARY Figure 3

SINGLE BYTE TRANSFER



BURST MODE TRANSFER



FUNCTION	BYTE N	SCLK n
CLOCK	8	72
RAM	24	200

REGISTER ADDRESS/DEFINITION Figure 4

REGISTER ADDRESS
A. CLOCK

	7	6	5	4	3	2	1	0
SEC	1	0	0	0	0	0	0	RD/$\overline{W}$
MIN	1	0	0	0	0	0	1	RD/$\overline{W}$
HR	1	0	0	0	0	1	0	RD/$\overline{W}$
DATE	1	0	0	0	0	1	1	RD/$\overline{W}$
MONTH	1	0	0	0	1	0	0	RD/$\overline{W}$
DAY	1	0	0	0	1	0	1	RD/$\overline{W}$
YEAR	1	0	0	0	1	1	0	RD/$\overline{W}$
CONTROL	1	0	0	0	1	1	1	RD/$\overline{W}$
CLOCK BURST	1	0	1	1	1	1	1	RD/$\overline{W}$

REGISTER DEFINITION

00–59	CH	10 SEC				SEC
00–59	0	10 MIN				MIN
01–12 00–23	12/24	0	10 A/P	HR		HR
01–28/29 01–30 01–31	0	0	10 DATE			DATE
01–12	0	0	0	10 M		MONTH
01–07	0	0	0	0	0	DAY
0–99	10 YEAR					YEAR
	WP	FORCED TO ZERO				

B. RAM

RAM 0	1	1	0	0	0	0	0	RD/$\overline{W}$
RAM 23	1	1	1	0	1	1	1	RD/$\overline{W}$
RAM BURST	1	1	1	1	1	1	1	RD/$\overline{W}$

RAM DATA 0								
RAM DATA 23								

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		2.0		5.5	V	1
Logic 1 Input	V_{IH}		2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	V_{CC}=2.0V	–0.3		+0.3	V	1
		V_{CC}=5V	–0.3		+0.8		

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 2.0 to 5.5V*)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}				+500	µA	6
I/O Leakage	I_{LO}				+500	µA	6
Logic 1 Output	V_{OH}	V_{CC}=2V	1.6			V	2
		V_{CC}=5V	2.4				
Logic 0 Output	V_{OL}	V_{CC}=2V			0.4	V	3
		V_{CC}=5V			0.4		
Active Supply Current	I_{CC}	V_{CC}=2V			.4	mA	5
		V_{CC}=5V			1.2		
Timekeeping Current	I_{CC1}	V_{CC}=2V			0.3	µA	4
		V_{CC}=5V			1		
Leakage Current	I_{CC2}	V_{CC}=2V			100	nA	10
		V_{CC}=5V			100		

*Unless otherwise noted.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Capacitance	C_X		6		pF	

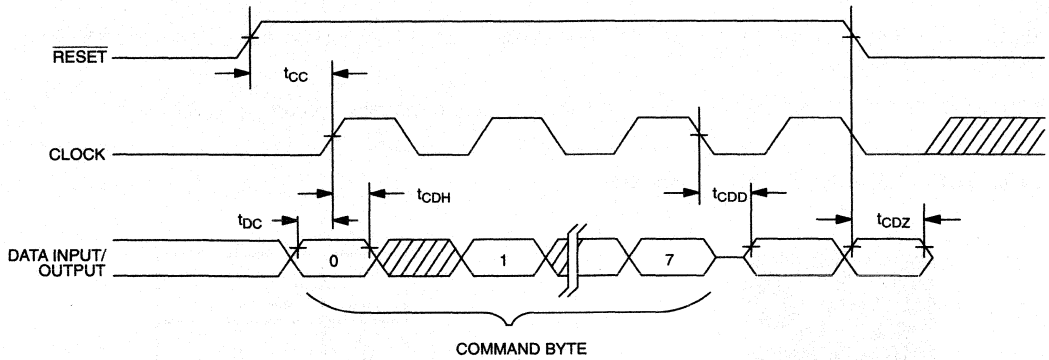
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 2.0 to 5.5V*)

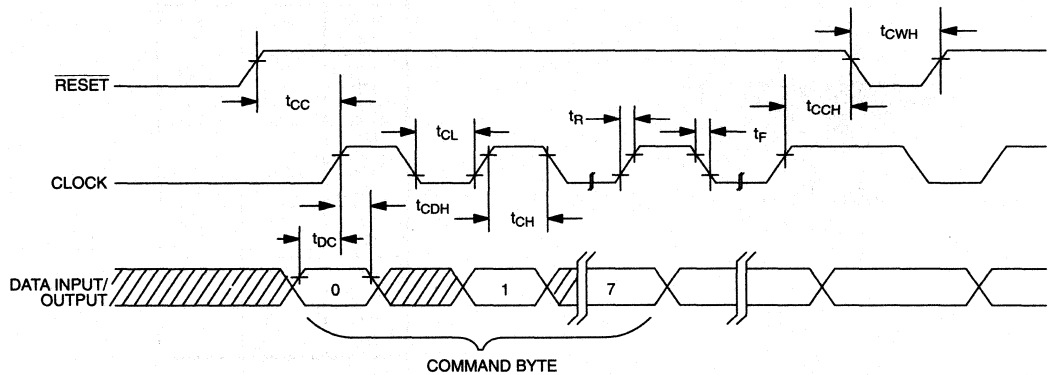
PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	V_{CC}=2V	200			ns	7
		V_{CC}=5V	50				
CLK to Data Hold	t_{CDH}	V_{CC}=2V	280			ns	7
		V_{CC}=5V	70				
CLK to Data Delay	t_{CDD}	V_{CC}=2V			800	ns	7, 8, 9
		V_{CC}=5V			200		
CLK Low Time	t_{CL}	V_{CC}=2V	1000			ns	7
		V_{CC}=5V	250				
CLK High Time	t_{CH}	V_{CC}=2V	1000			ns	7, 12
		V_{CC}=5V	250				
CLK Frequency	f_{CLK}	V_{CC}=2V			0.5	MHz	7, 12
		V_{CC}=5V	DC		2.0		
CLK Rise and Fall	t_R, t_F	V_{CC}=2V			2000	ns	
		V_{CC}=5V			500		
RST to CLK Setup	t_{CC}	V_{CC}=2V	4			µs	7
		V_{CC}=5V	1				
CLK to RST Hold	t_{CCH}	V_{CC}=2V	1000			ns	7
		V_{CC}=5V	250				
RST Inactive Time	t_{CWH}	V_{CC}=2V	4			µs	7
		V_{CC}=5V	1				
RST to I/O High Z	t_{CDZ}	V_{CC}=2V			280	ns	7
		V_{CC}=5V			70		

*Unless otherwise noted.

TIMING DIAGRAM: READ DATA TRANSFER Figure 5



TIMING DIAGRAM: WRITE DATA TRANSFER Figure 6



NOTES:

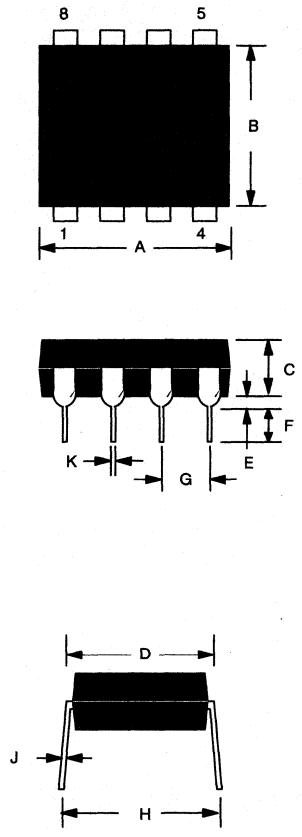
1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 mA at V_{CC}=5V and .4 mA at V_{CC}=2V, V_{OH}=V_{CC} for capacitive loads.
3. Logic zero voltages are specified at a sink current of 4 mA at V_{CC}=5V and 1.5 mA at V_{CC}=2V.
4. I_{CC1} is specified with I/O open, $\overline{RST}$ set to a logic 0, and clock halt flag=0 (oscillator enabled).
5. I_{CC} is specified with the I/O pin open, $\overline{RST}$ high, SCLK=2 MHz at V_{CC}=5V; SCLK=500 KHz, V_{CC}=2V and clock halt flag=0 (oscillator enabled).
6. $\overline{RST}$, SCLK, and I/O all have 40KΩ pulldown resistors to ground.
7. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10 ms maximum rise and fall time.
8. Measured at V_{OH}=2.4V or V_{OL}=0.4V.
9. Load capacitance = 50 pF.

10. I_{CC2} is specified with $\overline{RST}$, I/O, and SCLK open. The clock halt flag must be set to logic one (oscillator disabled).

11. At power–up, $\overline{RST}$ must be at a logic 0 until $V_{CC} \geqq 2$ volts. Also, SCLK must be at a logic 0 when $\overline{RST}$ is driven to a logic one state.

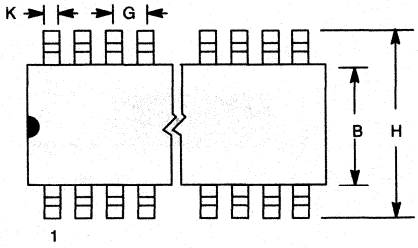
12. If t_{CH} exceeds 100 ms with $\overline{RST}$ in a logic one state, then I_{CC} may briefly exceed I_{CC} specification.

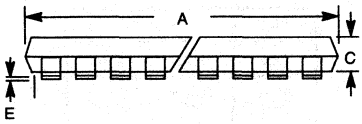
DS1202 SERIAL TIMEKEEPER 8–PIN DIP

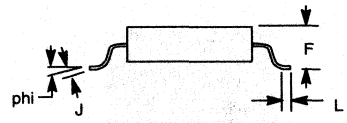


PKG	8–PIN	
DIM	MIN	MAX
A IN. MM	.360	.400
B IN. MM	.240	.260
C IN. MM	.120	.140
D IN. MM	.300	.325
E IN. MM	.015	.040
F IN. MM	.110	.140
G IN. MM	.090	.110
H IN. MM	.320	.370
J IN. MM	.008	.012
K IN. MM	.015	.021

DS1202S SERIAL TIMEKEEPER 16–PIN SOIC



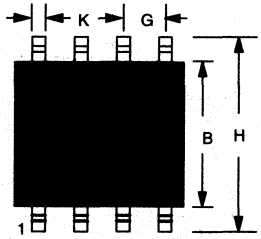


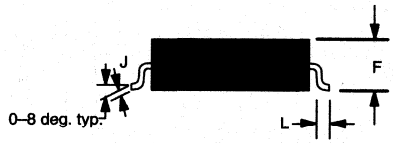


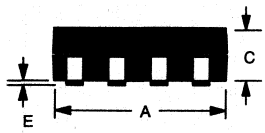
PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.500 12.70	0.511 12.99
B IN. MM	0.290 .7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN MM	0.016 0.406	0.040 1.20
phi	0°	8°

3

DS1202S8 8–PIN SOIC 200 MIL







PKG	8-PIN	
DIM	MIN	MAX
A IN. MM	0.203 5.16	0.213 5.41
B IN. MM	0.203 5.16	0.213 5.41
C IN. MM	0.070 1.78	0.074 1.88
E IN. MM	0.004 0.102	0.010 0.390
F IN. MM	0.074 1.88	0.84 2.13
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.302 7.67	0.318 8.07
J IN. MM	0.006 0.152	0.010 0.254
K IN. MM	0.013 0.33	0.020 0.508
L IN. MM	0.19 4.83	0.030 0.762

DALLAS SEMICONDUCTOR

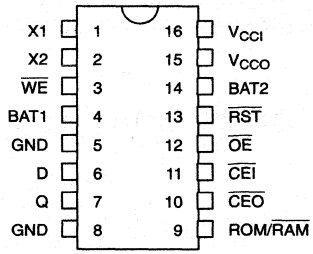
DS1215
Phantom Time Chip

3

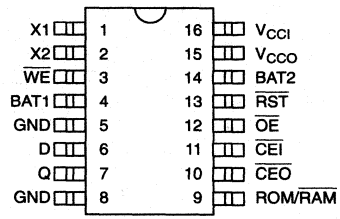
FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adjusts for months with fewer than 31 days
- Leap year automatically corrected
- No address space required
- Provides nonvolatile controller functions for battery backup of RAM
- Supports redundant batteries for high-reliability applications
- Uses a 32.768 KHz watch crystal
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Space-saving, 16-pin DIP package and SOIC

PIN ASSIGNMENT



16–PIN DIP (300 MIL)



16–PIN SOIC (300 MIL)

DESCRIPTION

The DS1215 Phantom Time Chip is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch keeps track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including correction for leap year every four years. The watch operates in one of two formats: a 12-hour mode with an AM/PM indicator or a 24-hour mode. The nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can be interfaced with either RAM or ROM without leaving gaps in memory.

PIN DESCRIPTION

X1, X2	–	32.768 KHz Crystal Connections
$\overline{WE}$	–	Write Enable
BAT1	–	Battery 1 Input
GND	–	Ground
D	–	Data In
Q	–	Data Out
ROM/$\overline{RAM}$	–	ROM/RAM Select
$\overline{CEO}$	–	Chip Enable Out
$\overline{CEI}$	–	Chip Enable Input
$\overline{OE}$	–	Output Enable
$\overline{RST}$	–	Reset
BAT2	–	Battery 2 Input
V_{CCO}	–	Switched Supply Output
V_{CCI}	–	+5 VDC Input

NOTE: Both pins 5 and 8 must be grounded.

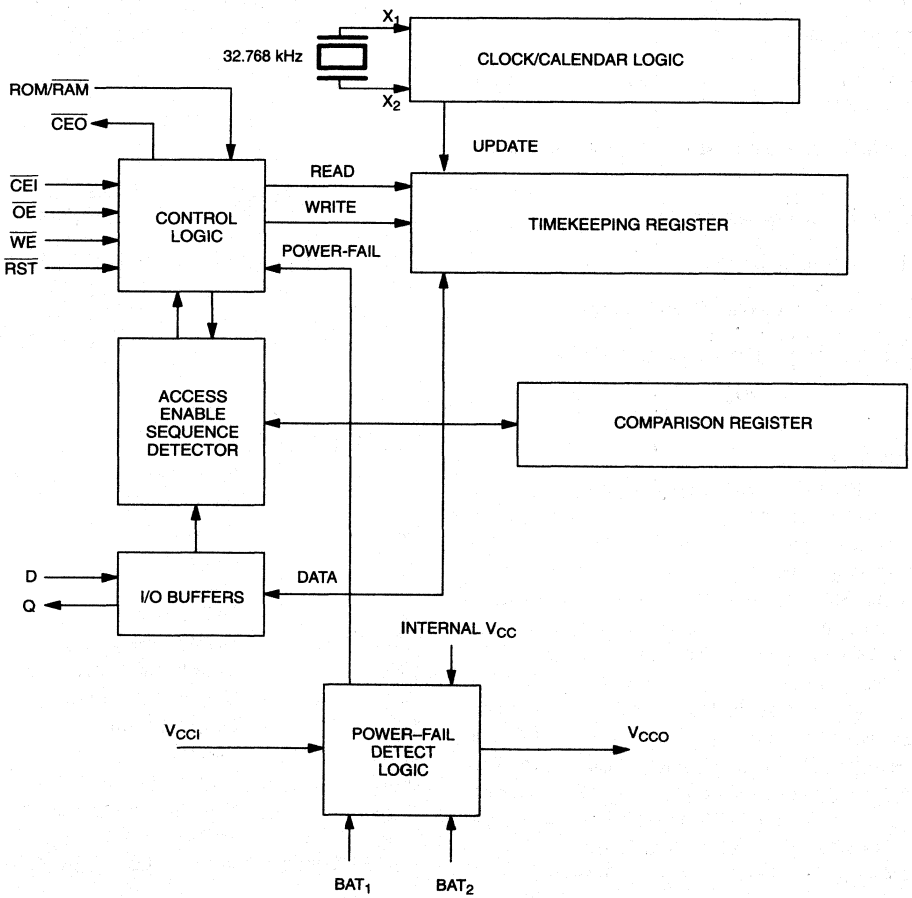
OPERATION

The block diagram of Figure 1 illustrates the main elements of the Time Chip. Communication with the Time Chip is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on data in (D). All accesses which occur prior to recognition of the 64-bit pattern are directed to memory via the chip enable output pin ($\overline{CEO}$).

After recognition is established, the next 64 read or write cycles either extract or update data in the Time Chip and $\overline{CEO}$ remains high during this time, disabling the connected memory.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable input ($\overline{CEI}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle using the $\overline{CEI}$ and $\overline{OE}$ control of the Time Chip starts the pattern recognition sequence by moving a pointer to the first bit of the 64 bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CEI}$ and $\overline{WE}$ control of the Time Chip. These 64 write cycles are used only to gain access to the Time Chip.

TIMING BLOCK DIAGRAM Figure 1



When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched. (This bit pattern is shown in Figure 2.) With a correct match for 64 bits, the Time Chip is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the Time Chip to either receive data on D, or transmit data on Q, depending on the level of $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Time Chip.

A 32,768 Hz quartz crystal, Seiko part no. DS-VT-200 or equivalent, can be directly connected to the DS1215 via pins 1 and 2 (X1, X2). The crystal selected for use should have a specified load capacitance (C_L) of 6 pF. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks".

TIME CHIP COMPARISON REGISTER DEFINITION Figure 2

	7	6	5	4	3	2	1	0	HEX VALUE
BYTE 0	1	1	0	0	0	1	0	1	C5
BYTE 1	0	0	1	1	1	0	1	0	3A
BYTE 2	1	0	1	0	0	0	1	1	A3
BYTE 3	0	1	0	1	1	1	0	0	5C
BYTE 4	1	1	0	0	0	1	0	1	C5
BYTE 5	0	0	1	1	1	0	1	0	3A
BYTE 6	1	0	1	0	0	0	1	1	A3
BYTE 7	0	1	0	1	1	1	0	0	5C

NOTE:
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Time Chip are less than 1 in 10^{19}.

NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the Time Chip is determined by the level of the ROM/$\overline{\text{RAM}}$ select pin. When ROM/$\overline{\text{RAM}}$ is connected to ground, the controller is set in the RAM mode and performs the circuit functions required to make static CMOS RAM and the timekeeping function nonvolatile. A switch is provided to direct power from the battery inputs or V_{CCI} to V_{CCO} with a maximum voltage drop of 0.3 volts. The V_{CCO} output pin is used to supply uninterrupted power to CMOS SRAM. The DS1215 also performs redundant battery control for high reliability. On power-fail, the battery with the highest voltage is automatically switched to V_{CCO}. If only one battery is used in the system, the unused battery input should be connected to ground.

The DS1215 safeguards the Time Chip and RAM data by power-fail detection and write protection. Power-fail detection occurs when V_{CCI} falls below VTP, which is equal to 1.26 x V_{BAT}. The DS1215 constantly monitors the V_{CCI} supply pin. When V_{CCI} is less than VTP, a comparator outputs a power-fail signal to the control logic. The power-fail signal forces the chip enable output ($\overline{\text{CEO}}$) to V_{CCI} or V_{BAT}-0.2 volts for external RAM write protection. During nominal supply conditions, $\overline{\text{CEO}}$ will track $\overline{\text{CEI}}$ with a maximum propagation delay of 20ns. Internally, the DS1215 aborts any data transfer in progress without changing any of the Time Chip registers and prevents future access until V_{CCI} exceeds VTP. A typical RAM/Time Chip interface is illustrated in Figure 3.

When the ROM/$\overline{\text{RAM}}$ pin is connected to V_{CCO}, the controller is set in the ROM mode. Since ROM is a read-only device that retains data in the absence of power, battery backup and write protection is not required. As a result, the chip enable logic will force $\overline{\text{CEO}}$ low when power fails. However, the Time Chip does retain the same internal nonvolatility and write protection as described in the RAM mode. In addition, the chip enable output is set at a low level on power-fail as V_{CCI} falls below the level of V_{BAT}. A typical ROM/Time Chip interface is illustrated in Figure 4.

TIME CHIP REGISTER INFORMATION

Time Chip information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Time Chip registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 5.

Data contained in the Time Chip registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping though all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 -23 hours).

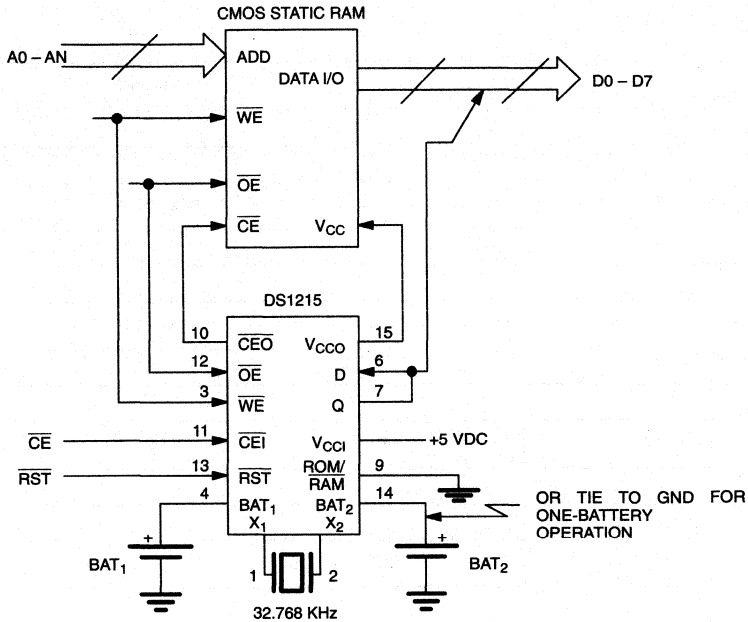
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin (Pin 13). When the reset bit is set to logic 1, the reset input pin is ignored. When the reset bit is set to logic 0, a low input on the reset pin will cause the Time Chip to abort data transfer without changing data in the timekeeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to logic 0, the oscillator turns on and the watch becomes operational.

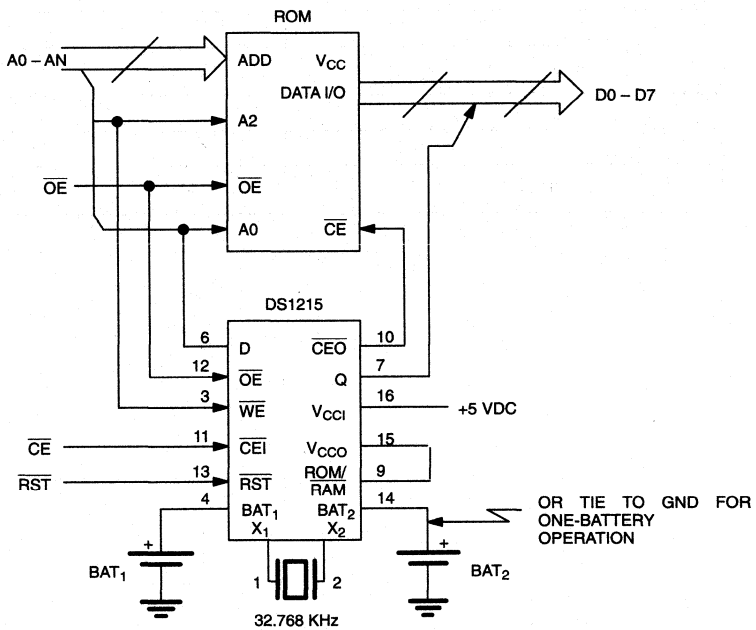
ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits that will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

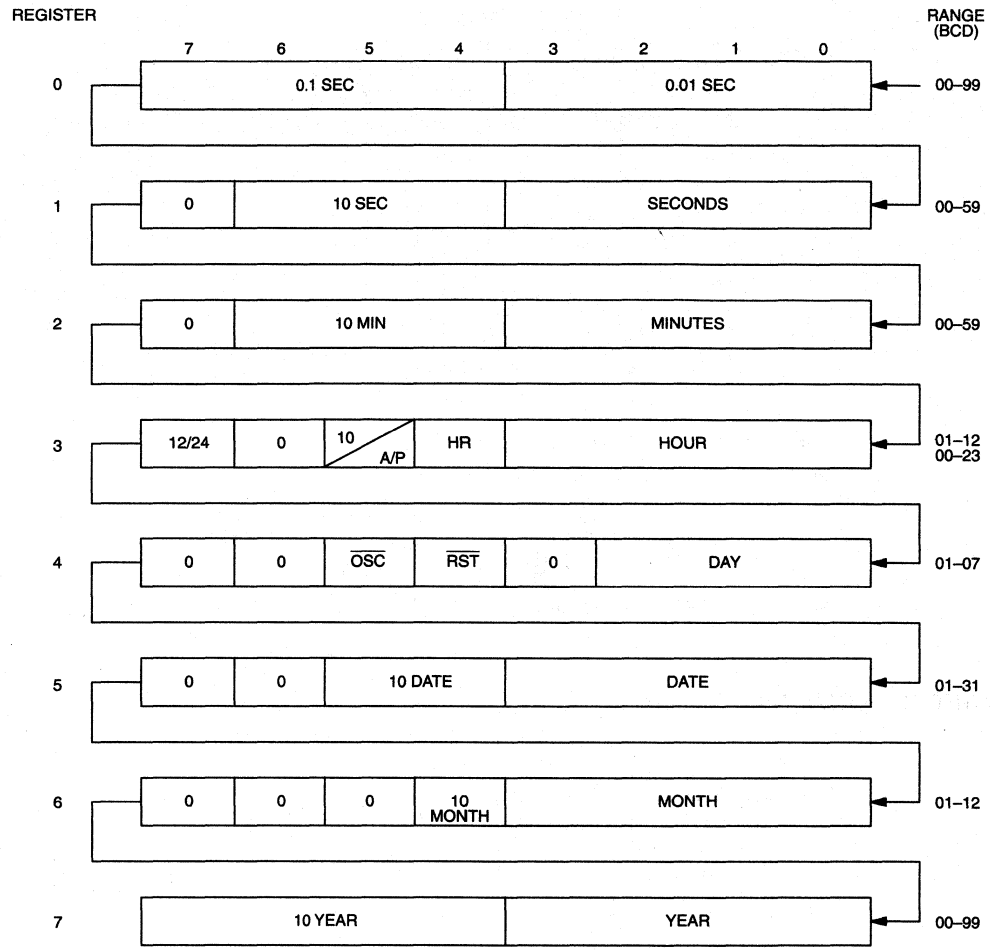
RAM/TIME CHIP INTERFACE Figure 3



ROM/TIME CHIP INTERFACE Figure 4



TIME CHIP REGISTER DEFINITION Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3		1
Logic 0	V_{IL}	-0.3		+0.8	V	1
V_{BAT1} or V_{BAT2} Battery Voltage	V_{BAT}	2.5		3.7	V	7

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	6
Supply Current $V_{CCO} = V_{CCI}$-0.3	I_{CCO1}			80	mA	8
Input Leakage	I_{IL}	-1.0		+1.0	µA	11
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Output @ 2.4V	I_{OH}	-1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} < 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEO}$ Output	V_{OH1}	V_{CCI} or V_{BAT}-0.2			V	9
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			1	µA	6
Battery Backup Current @ $V_{CCO} = V_{BAT}$-0.2V	I_{CCO2}			10	µA	10

AC ELECTRICAL CHARACTERISTICS ROM/$\overline{\text{RAM}}$ = GND

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{\text{CE1}}$ Access Time	t_{CO}			100	ns	
$\overline{\text{OE}}$ Access Time	t_{OE}			100	ns	
$\overline{\text{CE1}}$ to Output Low Z	t_{COE}	10			ns	
$\overline{\text{OE}}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{\text{CE1}}$ to Output High Z	t_{OD}			40	ns	
$\overline{\text{OE}}$ to Output High Z	t_{ODO}			40	ns	
Read Recovery	t_{RR}	20			ns	
Write Cycle	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	
Write Recovery	t_{WR}	20			ns	4
Data Setup	t_{DS}	40			ns	5
Data Hold Time	t_{DH}	10			ns	5
$\overline{\text{CE1}}$ Pulse Width	t_{CW}	100			ns	
$\overline{\text{RST}}$ Pulse Width	t_{RST}	200			ns	
$\overline{\text{CE1}}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 3
$\overline{\text{CE1}}$ High to Power-Fail	t_{PF}			0	ns	

AC ELECTRICAL CHARACTERISTICS ROM/$\overline{\text{RAM}}$ = GND

(0°C to 70°C; V_{CC} > 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3.0V	t_F	0			ms	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Output Capacitance	C_{OUT}		5	10	pF	

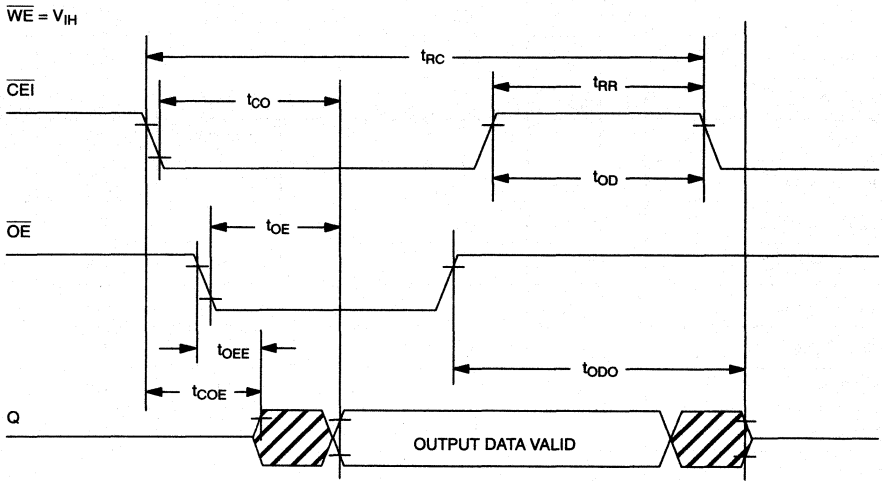
AC ELECTRICAL CHARACTERISTICS ROM/$\overline{RAM}$ = V_{CCO} (0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output in Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output in Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output in High Z	t_{OD}			40	ns	
$\overline{OE}$ to Output in High Z	t_{ODO}			40	ns	
Address Setup Time	t_{AS}	20			ns	
Address Hold Time	t_{AH}			10	ns	
Read Recovery	t_{RR}	20			ns	
Write Cycle Time	t_{WC}	120			ns	
$\overline{CE}$ Pulse Width	t_{CW}	100			ns	
$\overline{OE}$ Pulse Width	t_{OW}	100			ns	
Write Recovery	t_{WR}	20			ns	4
Data Setup Time	t_{DS}	40			ns	5
Data Hold Time	t_{DH}	10			ns	5
$\overline{RST}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 3
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

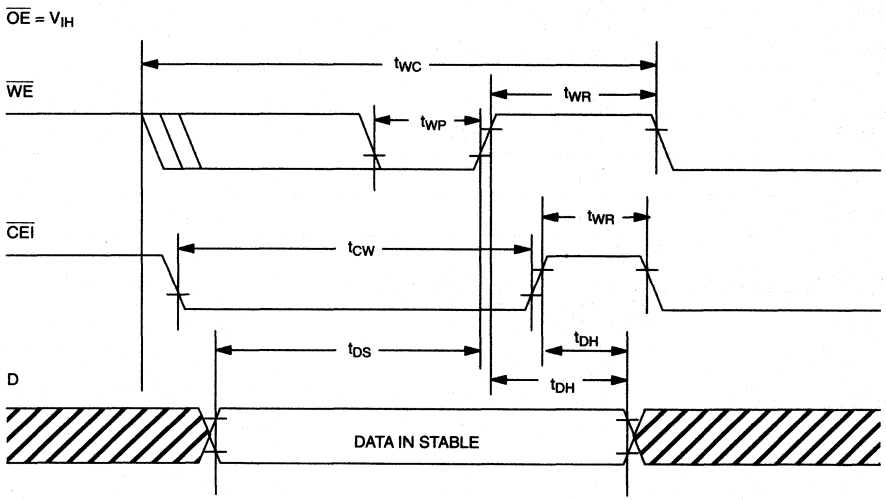
AC ELECTRICAL CHARACTERISTICS ROM/$\overline{RAM}$ = V_{CCO} (0°C to 70°C; V_{CC} < 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3.0V	t_F	0			ms	

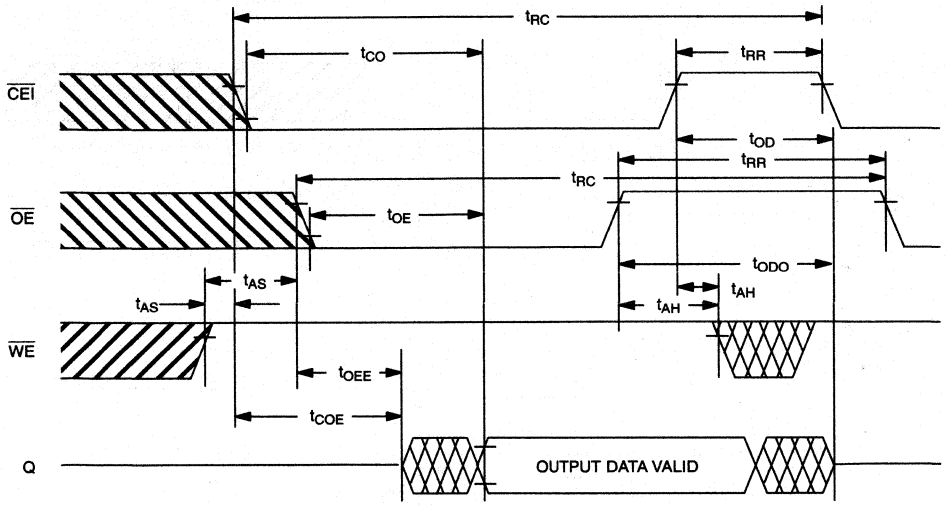
TIMING DIAGRAM: READ CYCLE TO TIME CHIP ROM/$\overline{\text{RAM}}$ = GND



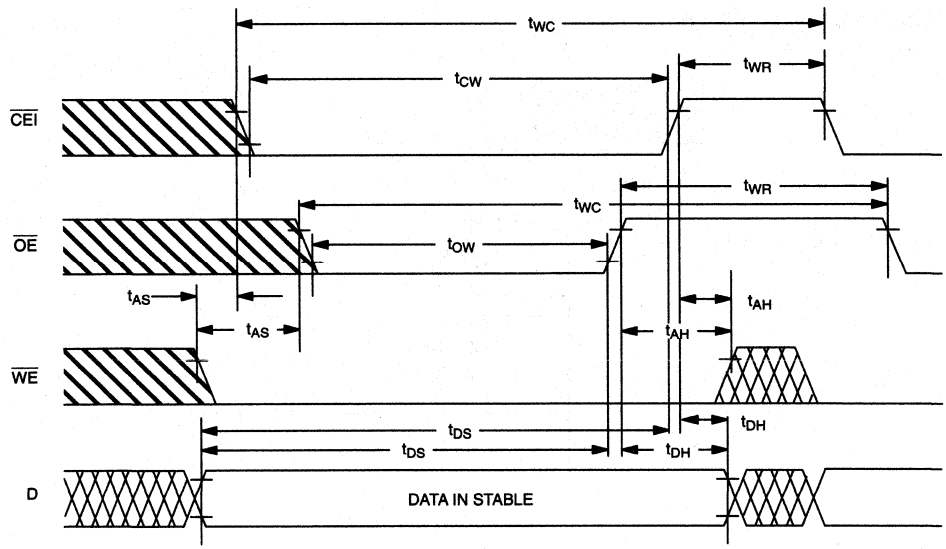
TIMING DIAGRAM: WRITE CYCLE TO TIME CHIP ROM/$\overline{\text{RAM}}$ = GND



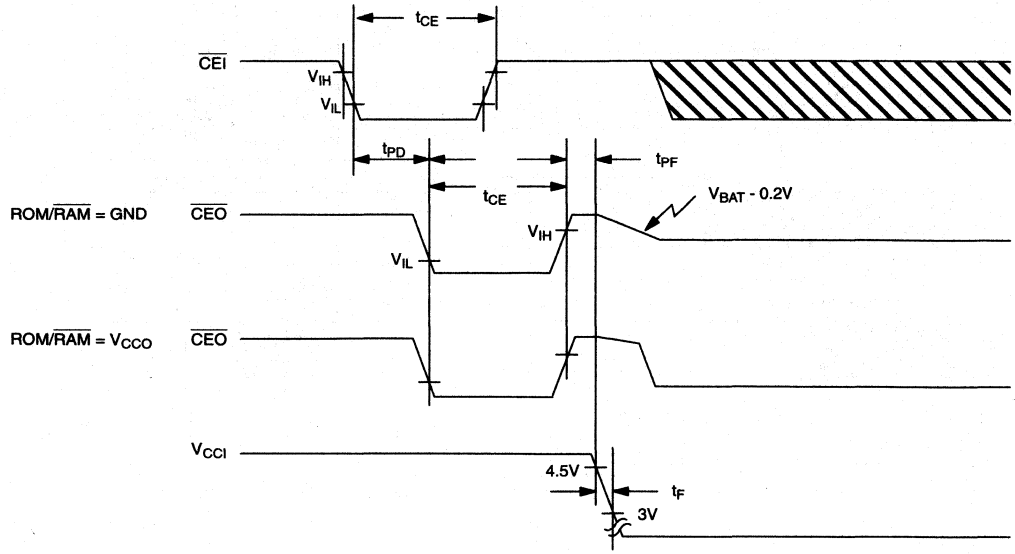
TIMING DIAGRAM: READ CYCLE ROM/$\overline{\text{RAM}}$ = V_{CCO}



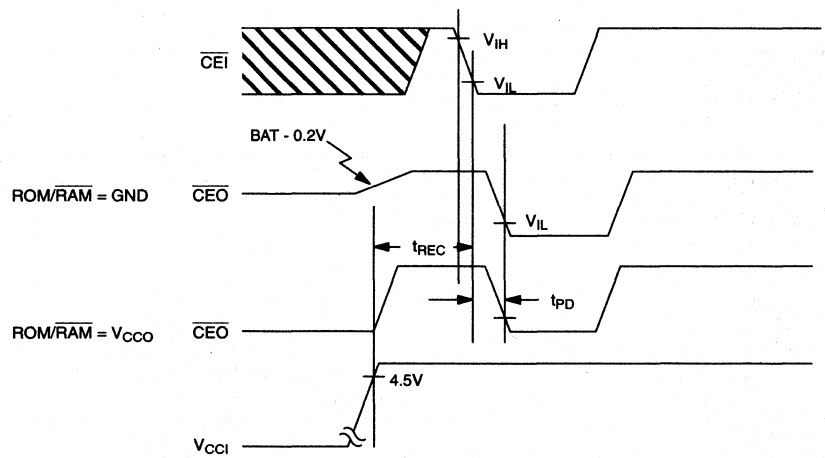
TIMING DIAGRAM: WRITE CYCLE ROM/$\overline{\text{RAM}}$ = V_{CCO}



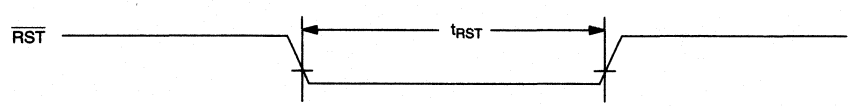
TIMING DIAGRAM: POWER DOWN



TIMING DIAGRAM: POWER UP



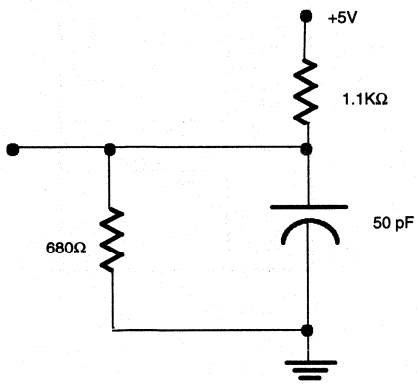
TIMING DIAGRAM: RESET FOR TIME CHIP



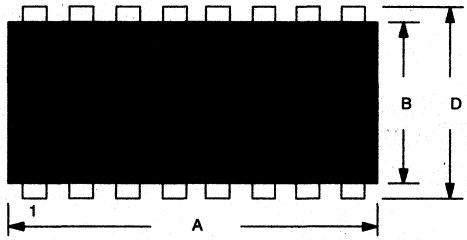
NOTES:

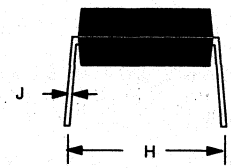
1. All voltages are referenced to ground.
2. Measured with load shown in Figure 6.
3. Input pulse rise and fall times equal 10ns.
4. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode, or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
5. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode, or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
6. Measured without RAM connected.
7. Trip point voltage for power-fail detect. $V_{TP} = 1.26 \times V_{BAT}$. For 10% V_{CC}= 5V + 10% operation V_{BAT} = 3.5V max.; for 5% operation V_{BAT} = 3.7V max.
8. I_{CC01} is the maximum average load current the DS1215 can supply to memory.
9. Applies to $\overline{CEO}$ with the ROM/$\overline{RAM}$ pin grounded. When the ROM/$\overline{RAM}$ pin is connected to V_{CCO}, $\overline{CEO}$ will go to a low level as V_{CCI} falls below V_{BAT}.
10. I_{CC02} is the maximum average load current that the DS1215 can supply to memory in the battery backup mode.
11. Applies to all input pins except $\overline{RST}$. $\overline{RST}$ is pulled internally to V_{CCI}.

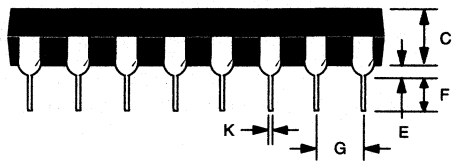
OUTPUT LOAD Figure 6



DS1215 TIME CHIP

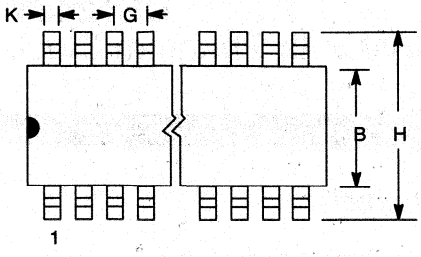


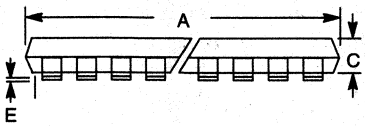


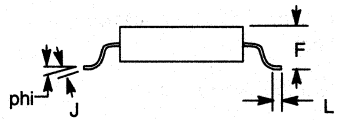


PKG	16-PIN	
DIM	**MIN**	**MAX**
A IN. MM	.740	.780
B IN. MM	.240	.260
C IN. MM	.120	.140
D IN. MM	.300	.325
E IN. MM	.015	.040
F IN. MM	.110	.140
G IN. MM	.090	.110
H IN. MM	.300	.370
J IN. MM	.008	.012
K IN. MM	.015	.021

DS1215S SERIAL TIMEKEEPER 16–PIN SOIC







PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	.050 BSC 1.27 BSC	
H IN MM	0.398 10.11	0.416 10.57
J IN MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN MM	.016 .40	.040 1.02
PHI	0°	8°

DALLAS SEMICONDUCTOR

DS1243Y
64K NV SRAM with Phantom Clock

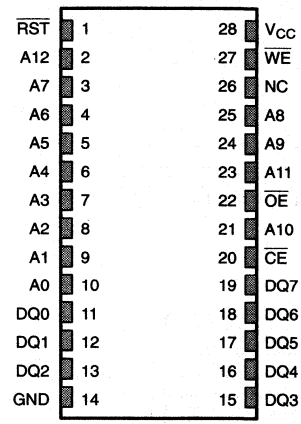
FEATURES

- Real time clock keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- 8K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C
- Over 10 years of data retention in the absence of power
- Available in 120, 150 and 200 ns access time

ORDERING INFORMATION

DS1243Y–XXX		
	–120	120 ns access
	–150	150 ns access
DS1243Y		200 ns access

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
720 MIL EXTENDED

PIN DESCRIPTION

A_0-A_{12}	–	Address Inputs
$\overline{CE}$	–	Chip Enable
GND	–	Ground
DQ_0-DQ_7	–	Data In/Data Out
V_{CC}	–	Power (+5V)
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
NC	–	No Connect
$\overline{RST}$	–	Reset

DESCRIPTION

The DS1243Y 64K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 8192 words by 8 bits) with a built-in real time clock. The DS1243Y has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent corrupted data in both the memory and real time clock.

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Phantom Clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

RAM READ MODE

The DS1243Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A0-A12) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

RAM WRITE MODE

The DS1243Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1243Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by approximately 4.0 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

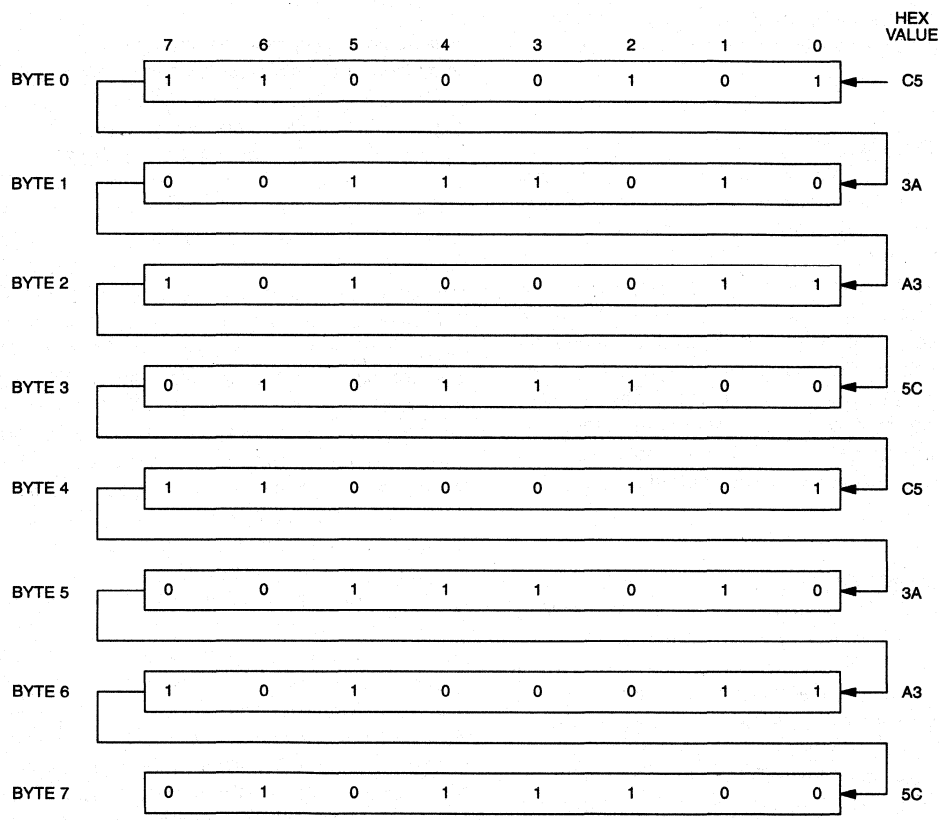
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the Phantom Clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

PHANTOM CLOCK REGISTER INFORMATION

The Phantom Clock information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the Phantom Clock register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

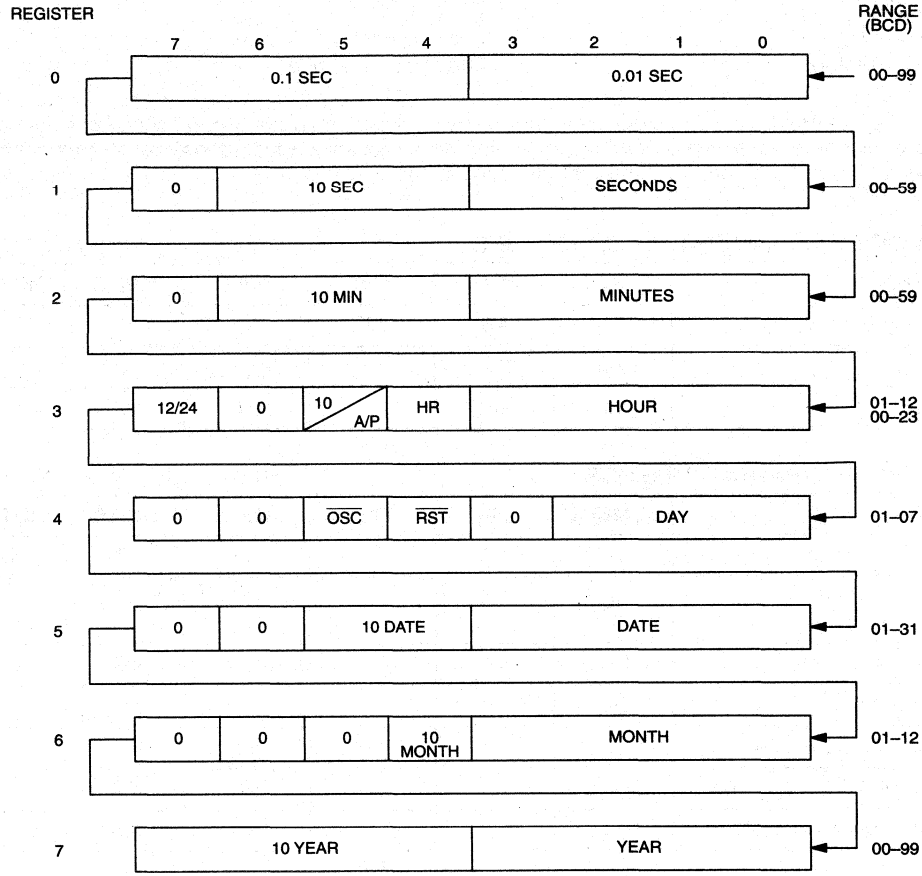
PHANTOM CLOCK REGISTER DEFINITION Figure 1



NOTE:

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Clock is less than 1 in 10^{19}. This pattern is sent to the Phantom Clock LSB to MSB.

PHANTOM CLOCK REGISTER DEFINITION Figure 2



AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logic 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logic 0, a low input on the $\overline{\text{RESET}}$ pin will cause the Phantom Clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	
Input Logic 0	V_{IL}	–0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	12
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 200 ns	I_{CC01}			85	mA	

DC TEST CONDITIONS

Outputs are open; all voltages are referenced to ground.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

MEMORY AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	DS1243Y-120		DS1243Y-150		DS1243Y		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		60		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		40		70		100	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		150		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		ns	
Output High Z from $\overline{WE}$	t_{ODW}		40		70		80	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	50		60		80		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20		20		20		ns	4

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0-3V

Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output High Z	t_{OD}			40	ns	5
$\overline{OE}$ to Output High Z	t_{ODO}			40	ns	5
Read Recovery	t_{RR}	20			ns	
Write Cycle Time	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	
Write Recovery	t_{WR}	20			ns	10
Data Setup Time	t_{DS}	40			ns	11
Data Hold Time	t_{DH}	10			ns	11
$\overline{CE}$ Pulse Width	t_{CW}	100			ns	
$\overline{RESET}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	

POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}			2	ms	

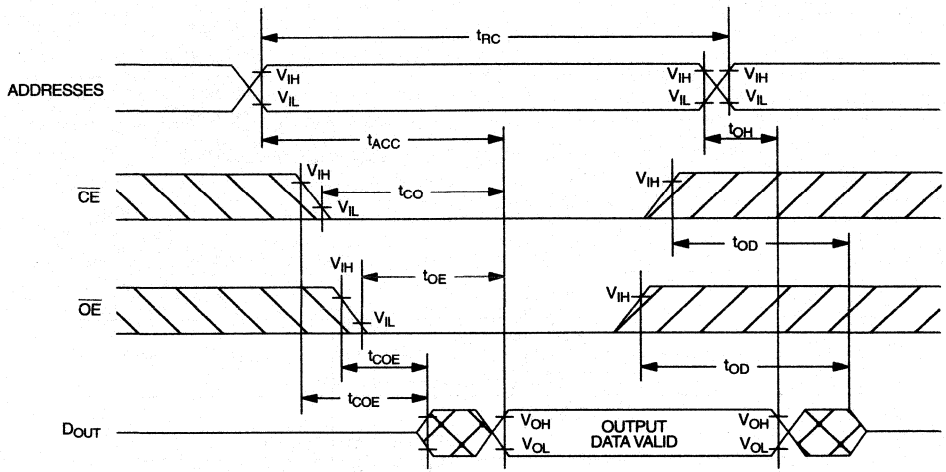
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

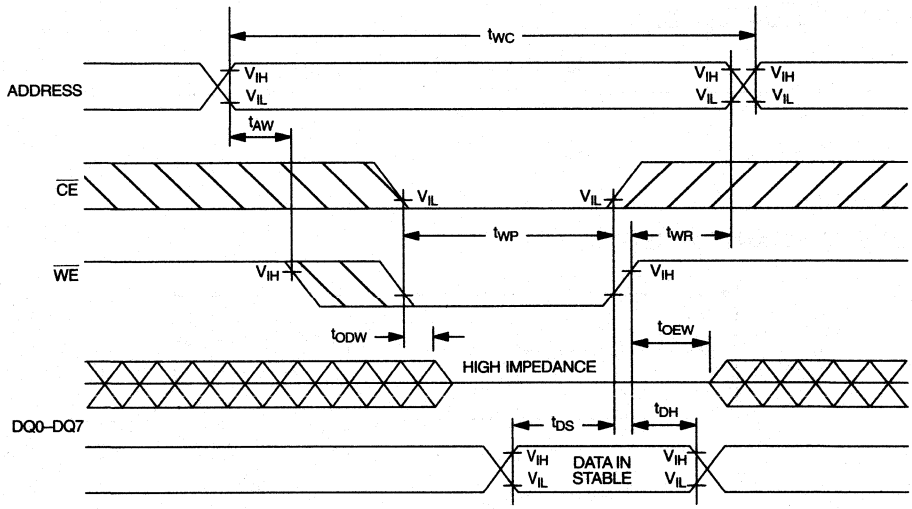
WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

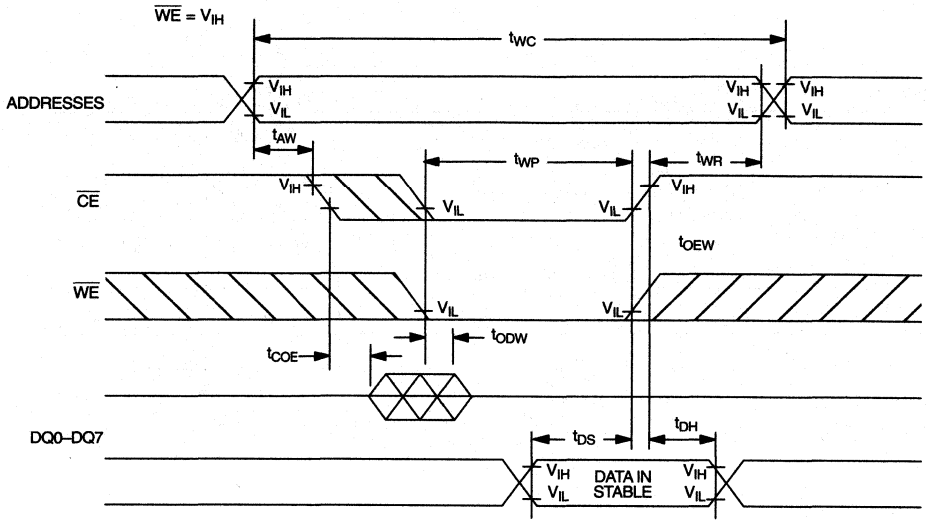
MEMORY READ CYCLE (NOTE 1)



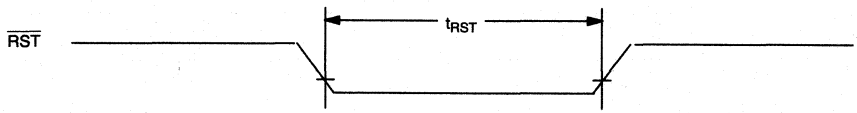
MEMORY WRITE CYCLE 1 (NOTES 2, 6, AND 7)



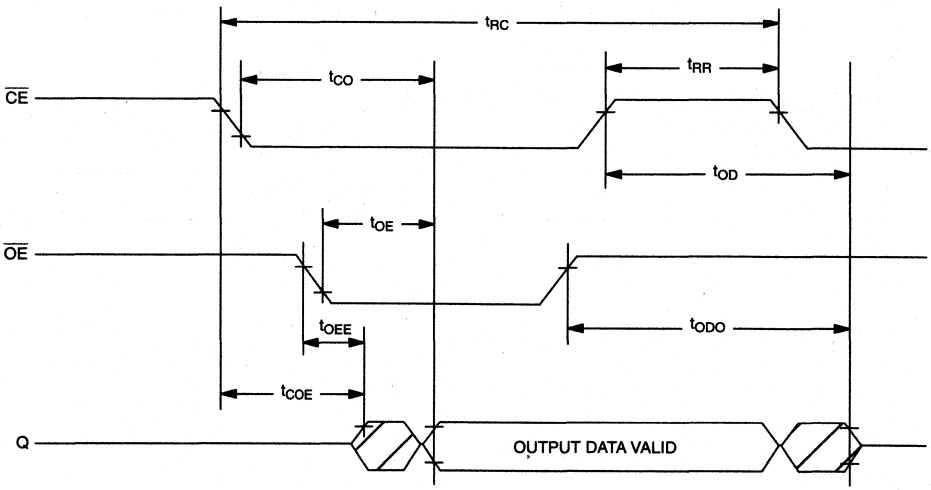
MEMORY WRITE CYCLE 2 (NOTES 2 AND 8)



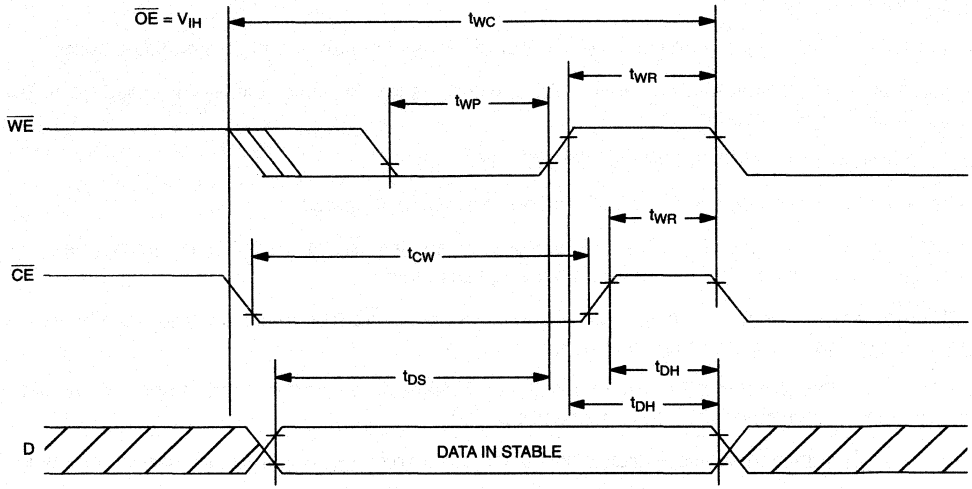
RESET FOR PHANTOM CLOCK



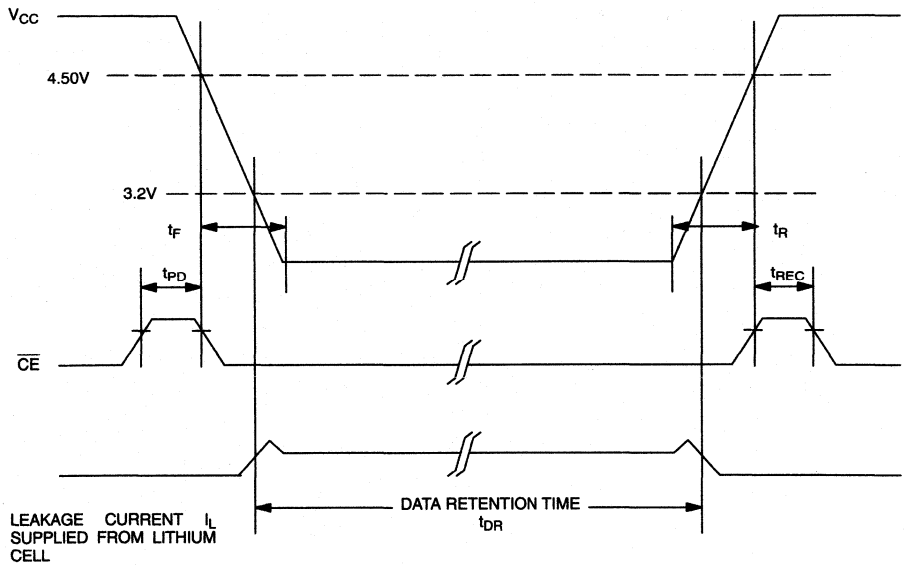
READ CYCLE TO PHANTOM CLOCK



WRITE CYCLE TO PHANTOM CLOCK



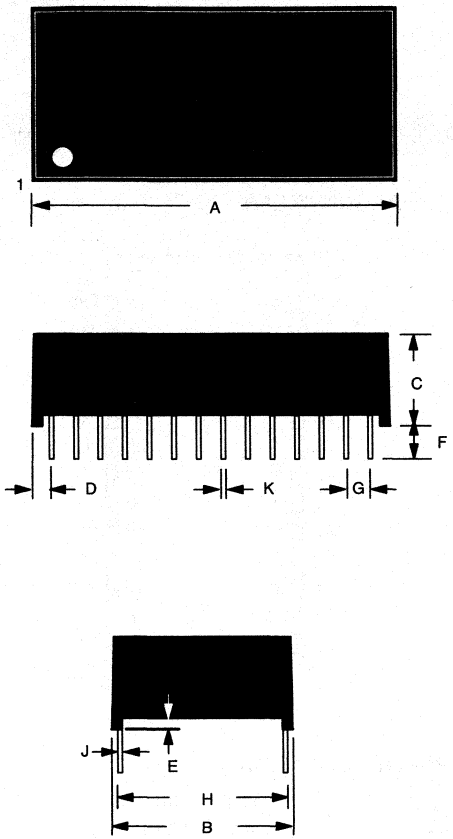
POWER-DOWN/POWER-UP CONDITION



NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 50 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} with the clock oscillator running.
10. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
11. t_{DH} and t_{DS} are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
12. $\overline{RST}$ (Pin1) has an internal pull-up resistor.

DS1243Y 28–PIN EXTENDED BOTTOM 720 MIL BODY WIDTH (DIMENSION B)



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

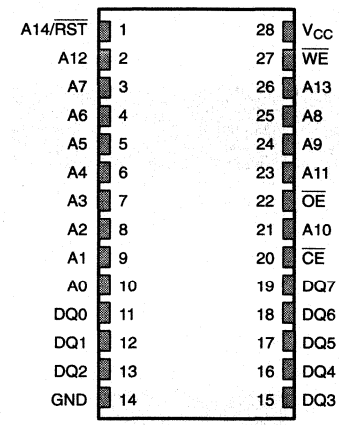
DALLAS SEMICONDUCTOR

DS1244Y
256K NV SRAM with Phantom Clock

FEATURES

- Real time clock keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years
- 32K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C
- Over 10 years of data retention in the absence of power
- Available in 120, 150 and 200 ns access time

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED

PIN DESCRIPTION

A_0-A_{14}	–	Address Inputs
$\overline{CE}$	–	Chip Enable
GND	–	Ground
DQ_0-DQ_7	–	Data In/Data Out
V_{CC}	–	Power (+5V)
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
NC	–	No Connect
$\overline{RST}$	–	Reset

DESCRIPTION

The DS1244Y 256K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 32,768 words by 8 bits) with a built-in real time clock. The DS1244Y has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock.

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Phantom Clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

RAM READ MODE

The DS1244Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

RAM WRITE MODE

The DS1244Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1244Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by approximately 4.0 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

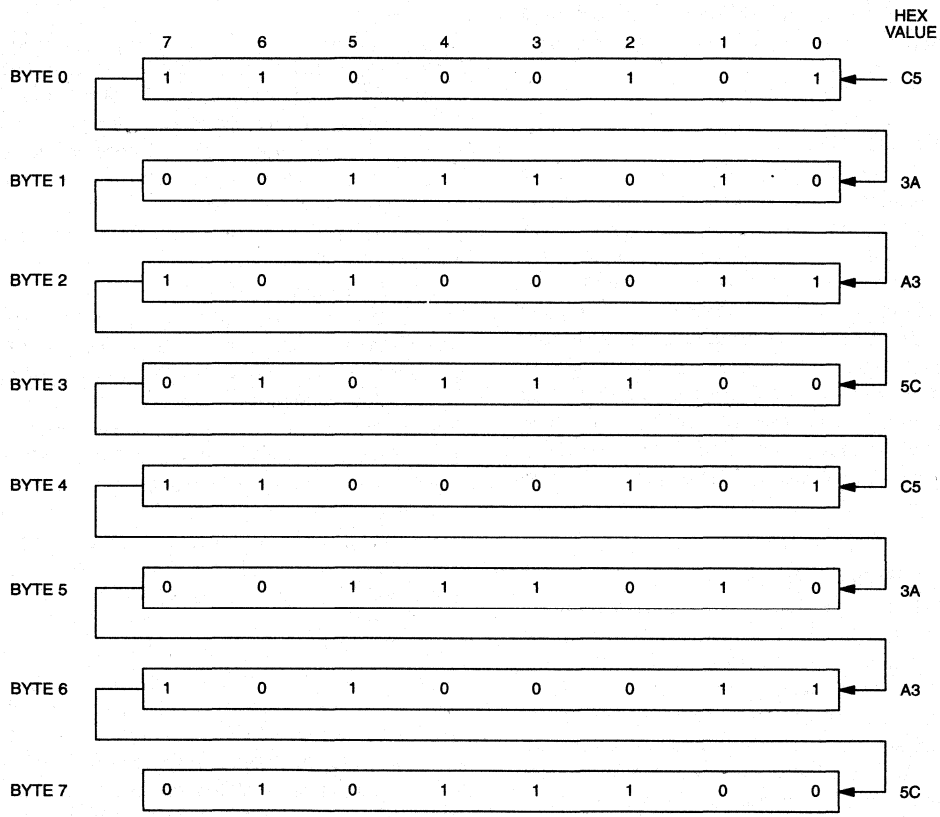
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the Phantom Clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

PHANTOM CLOCK REGISTER INFORMATION

The Phantom Clock information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the Phantom Clock register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

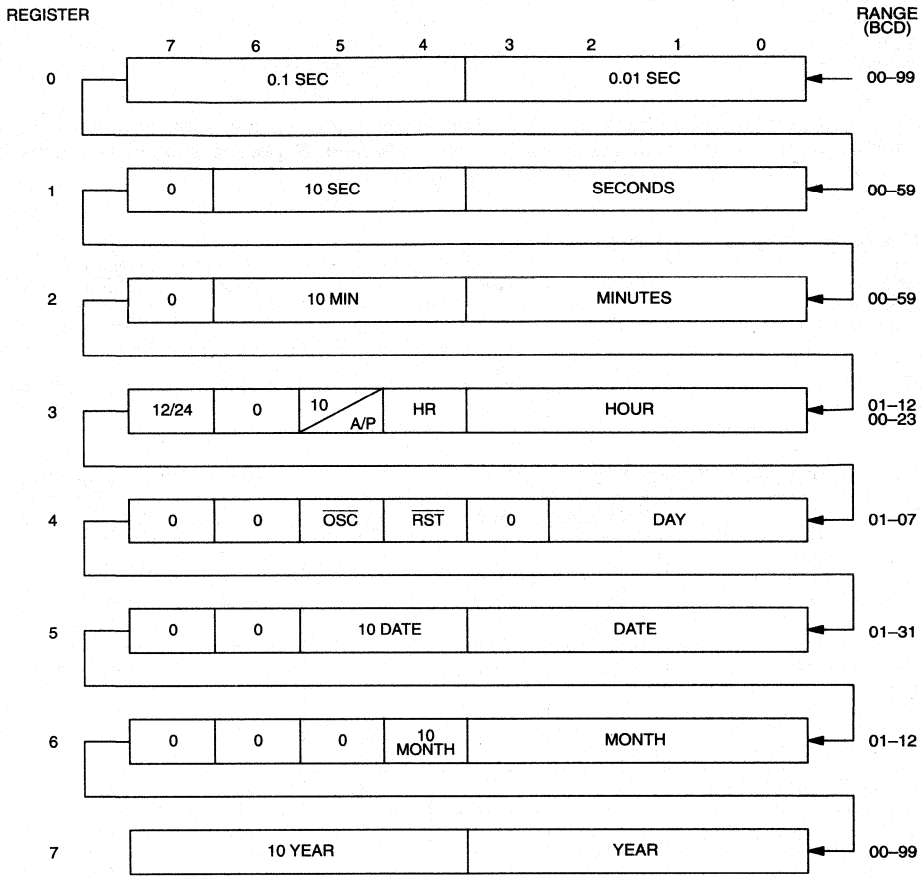
PHANTOM CLOCK REGISTER DEFINITION Figure 1



NOTE:

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Clock is less than 1 in 10^{19}. This pattern is sent to the Phantom Clock LSB to MSB.

PHANTOM CLOCK REGISTER DEFINITION Figure 2



AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logic 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logic 0, a low input on the $\overline{\text{RESET}}$ pin will cause the Phantom Clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	
Input Logic 0	V_{IL}	0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	12
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 200 ns	I_{CC01}			85	mA	

DC TEST CONDITIONS

Outputs are open; all voltages are referenced to ground.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

MEMORY AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	DS1244Y-120		DS1244Y-150		DS1244Y-200		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		60		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		40		70		100	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		150		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		ns	
Output High Z from $\overline{WE}$	t_{ODW}		40		70		80	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	50		60		80		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20		20		20		ns	4

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0-3V

Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output High Z	t_{OD}			40	ns	5
$\overline{OE}$ to Output High Z	t_{ODO}			40	ns	5
Read Recovery	t_{RR}	20			ns	
Write Cycle Time	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	
Write Recovery	t_{WR}	20			ns	10
Data Setup Time	t_{DS}	40			ns	11
Data Hold Time	t_{DH}	10			ns	11
$\overline{CE}$ Pulse Width	t_{CW}	100			ns	
$\overline{RESET}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	

POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}			2	ms	

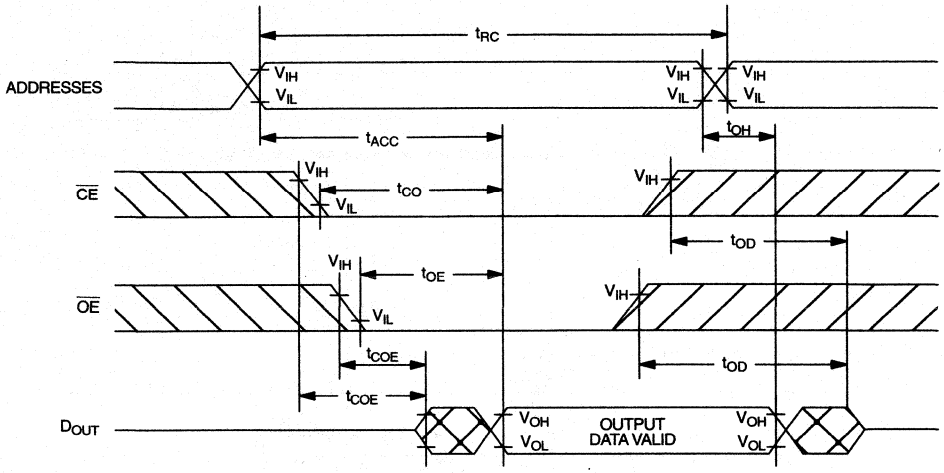
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

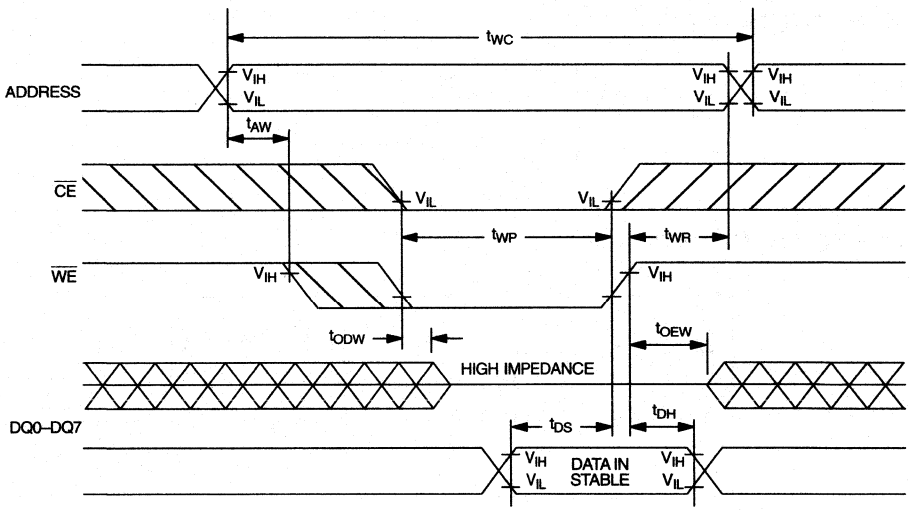
WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

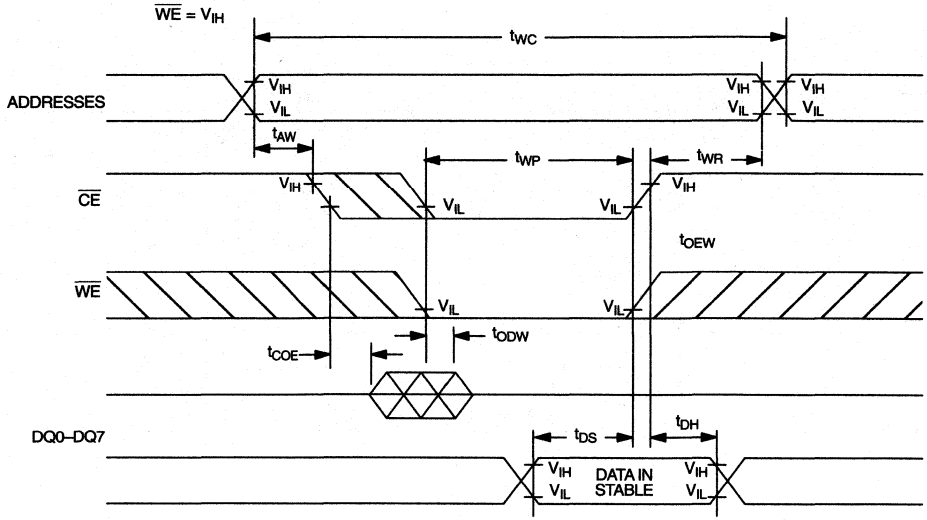
MEMORY READ CYCLE (NOTE 1)



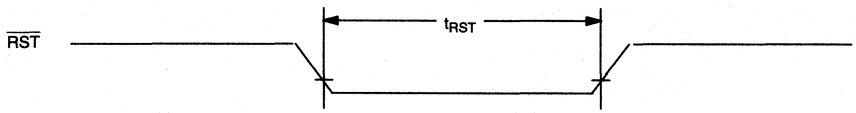
MEMORY WRITE CYCLE 1 (NOTES 2, 6, AND 7)



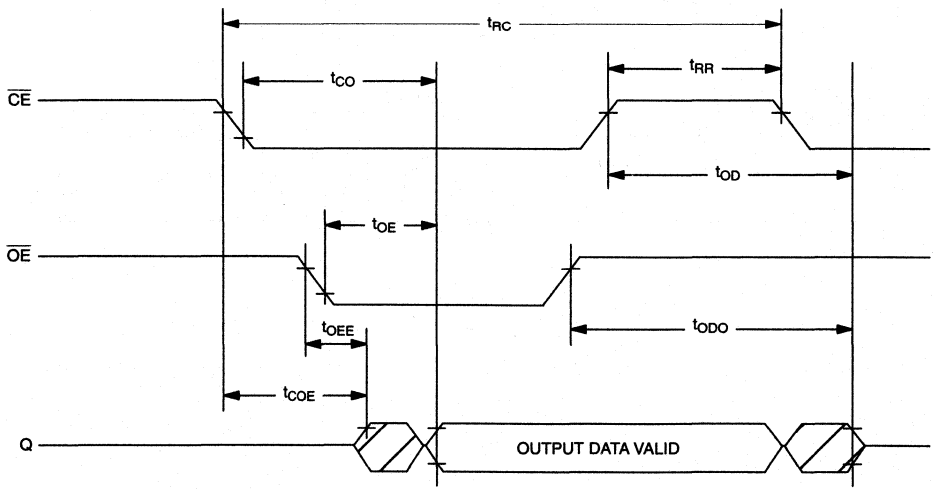
MEMORY WRITE CYCLE 2 (NOTES 2 AND 8)



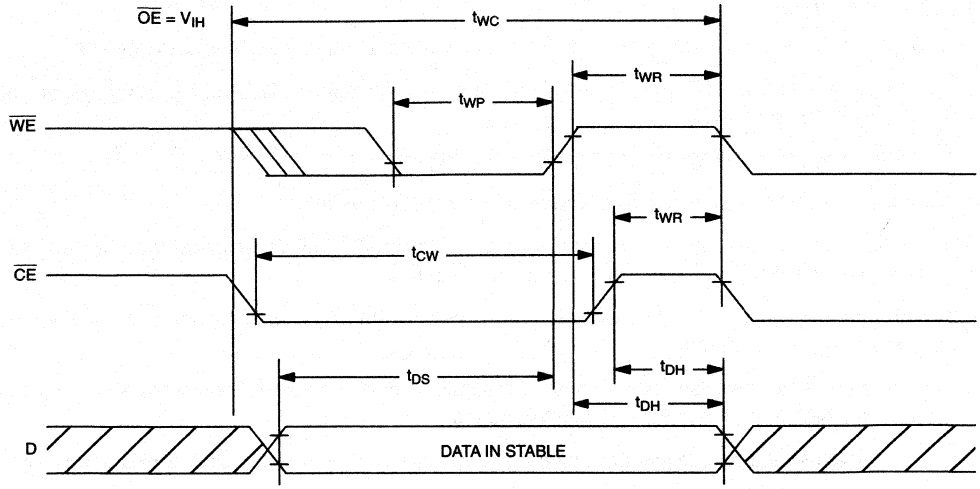
RESET FOR PHANTOM CLOCK



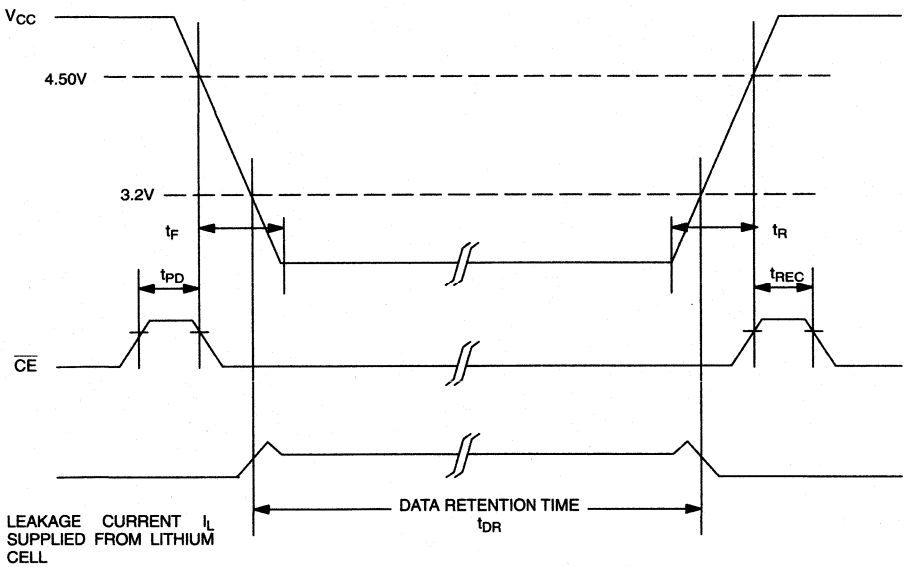
READ CYCLE TO PHANTOM CLOCK



WRITE CYCLE TO PHANTOM CLOCK



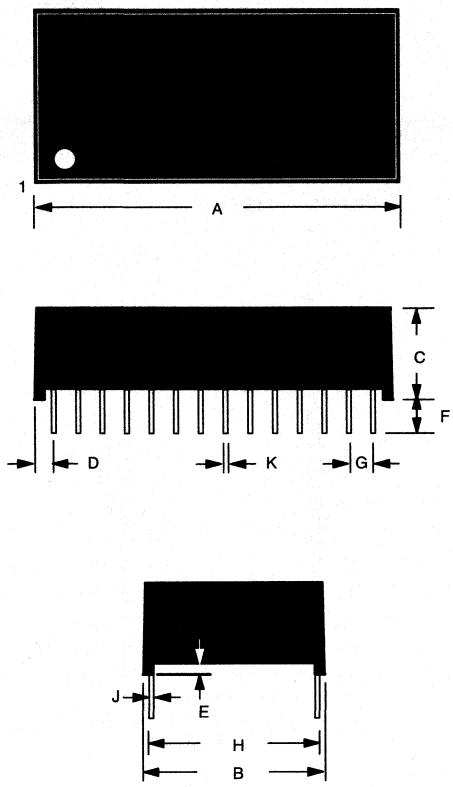
POWER-DOWN/POWER-UP CONDITION



NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 50 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} with the clock oscillator running.
10. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
11. t_{DH} and t_{DS} are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
12. $\overline{RST}$ (Pin1) has an internal pull-up resistor.

DS1244Y 256K NV SRAM WITH PHANTOM CLOCK



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

3

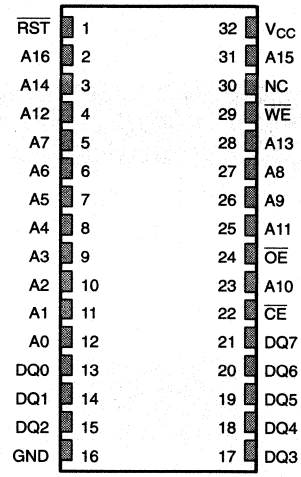
DALLAS SEMICONDUCTOR

DS1248Y
1024K NV SRAM with Phantom Clock

FEATURES

- Real time clock keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years
- 128K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C
- Over 10 years of data retention in the absence of power
- Available in 120, 150 and 200 ns access time

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
740 MIL FLUSH

PIN DESCRIPTION

A_0-A_{16}	–	Address Inputs
$\overline{CE}$	–	Chip Enable
GND	–	Ground
DQ_0-DQ_7	–	Data In/Data Out
V_{CC}	–	Power (+5V)
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
NC	–	No Connect
$\overline{RST}$	–	Reset

DESCRIPTION

The DS1248Y 1024K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 128K words by 8 bits) with a built-in real time clock. The DS1248Y has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock.

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Phantom Clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

RAM READ MODE

The DS1248Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 17 address inputs (A0-A16) defines which of the 128K bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

RAM WRITE MODE

The DS1248Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1248Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by approximately 4.0 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

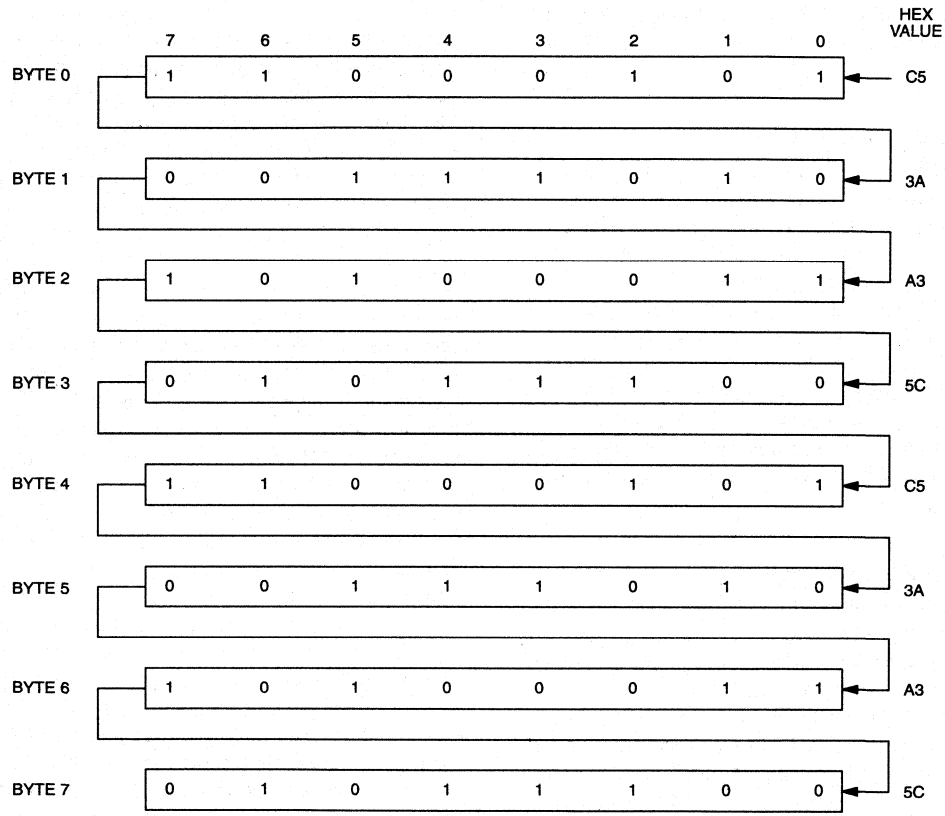
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the Phantom Clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

PHANTOM CLOCK REGISTER INFORMATION

The Phantom Clock information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the Phantom Clock register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

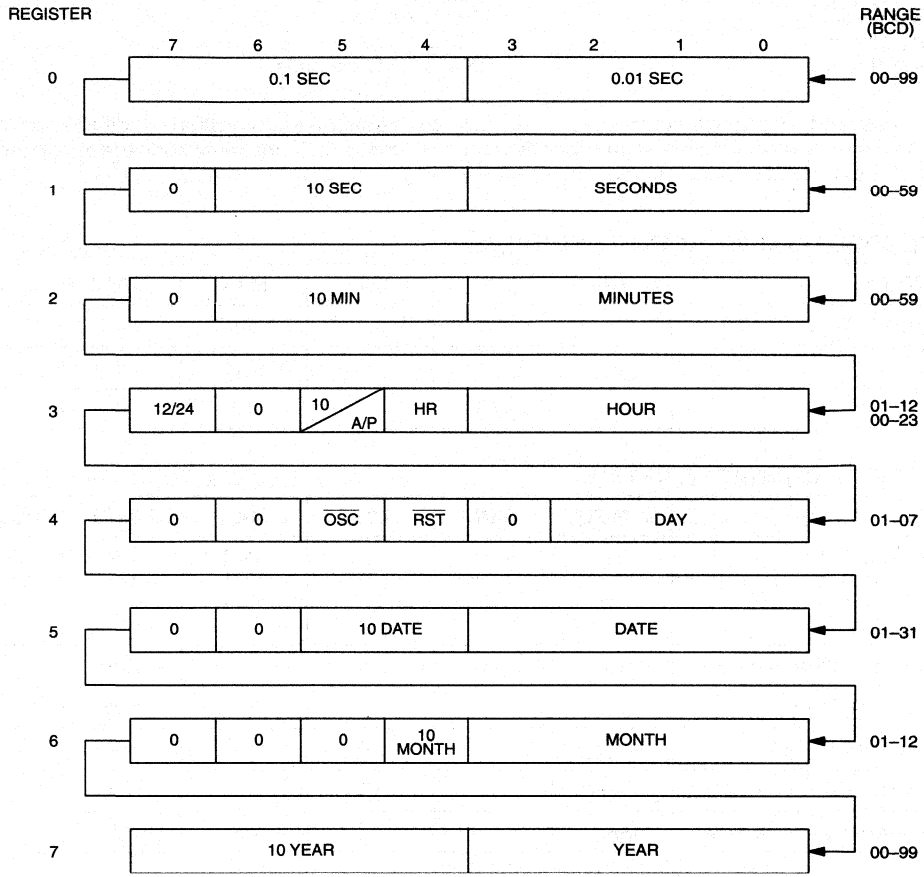
PHANTOM CLOCK REGISTER DEFINITION Figure 1



NOTE:

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Clock is less than 1 in 10^{19}. This pattern is sent to the Phantom Clock LSB to MSB.

PHANTOM CLOCK REGISTER DEFINITION Figure 2



AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logic 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logic 0, a low input on the $\overline{\text{RESET}}$ pin will cause the Phantom Clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	
Input Logic 0	V_{IL}	-0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	12
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 200 ns	I_{CC01}			85	mA	

DC TEST CONDITIONS

Outputs are open; all voltages are referenced to ground.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

MEMORY AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	DS1248Y-120		DS1248Y-150		DS1248Y-200		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		60		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		40		70		100	ns	5
Output Hold from Address Change	t_{oH}	5		5		5		ns	
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		150		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		ns	
Output High Z from $\overline{WE}$	t_{ODW}		40		70		80	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	50		60		80		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20		20		20		ns	4

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0-3V

Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output High Z	t_{OD}			40	ns	5
$\overline{OE}$ to Output High Z	t_{ODO}			40	ns	5
Read Recovery	t_{RR}	20			ns	
Write Cycle Time	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	
Write Recovery	t_{WR}	20			ns	10
Data Setup Time	t_{DS}	40			ns	11
Data Hold Time	t_{DH}	10			ns	11
$\overline{CE}$ Pulse Width	t_{CW}	100			ns	
$\overline{RESET}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	

POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}			2	ms	

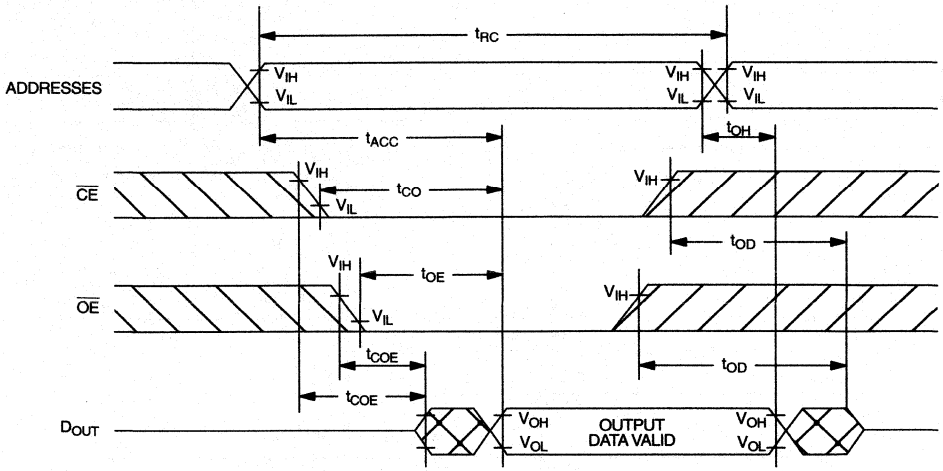
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

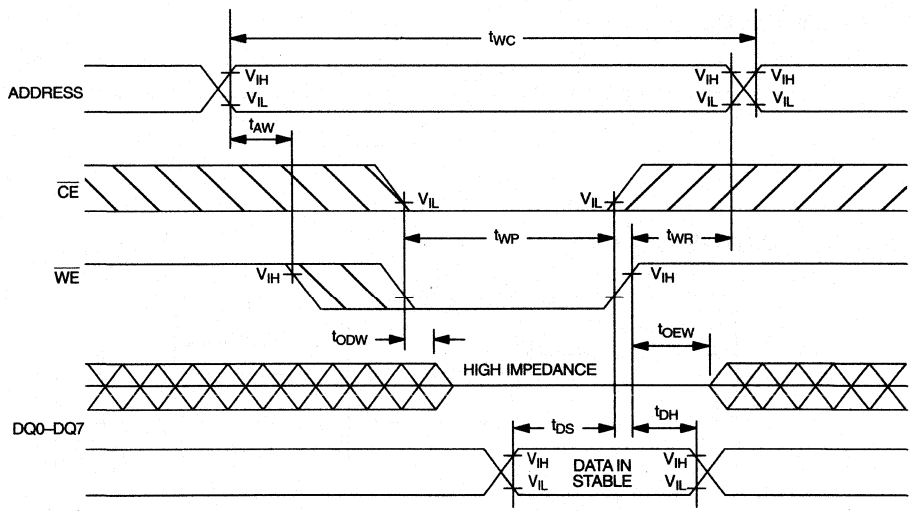
WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

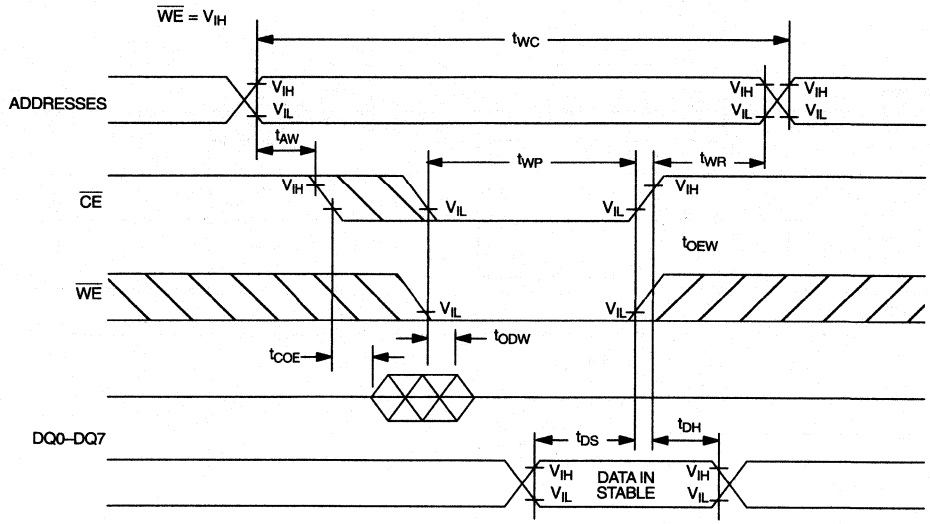
MEMORY READ CYCLE (NOTE 1)



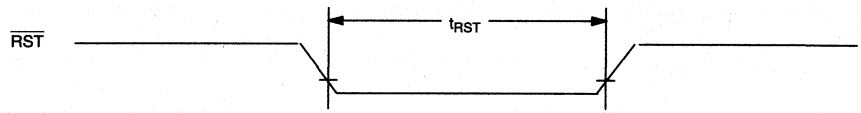
MEMORY WRITE CYCLE 1 (NOTES 2, 6, AND 7)



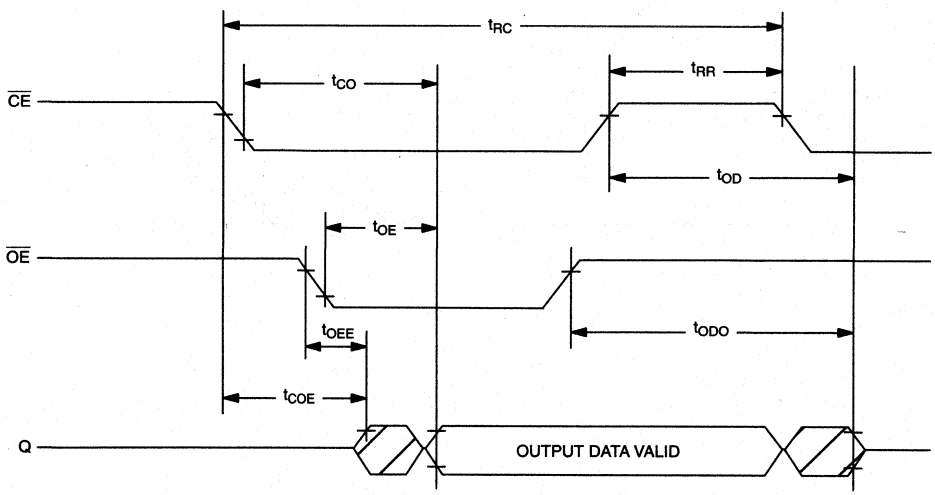
MEMORY WRITE CYCLE 2 (NOTES 2 AND 8)



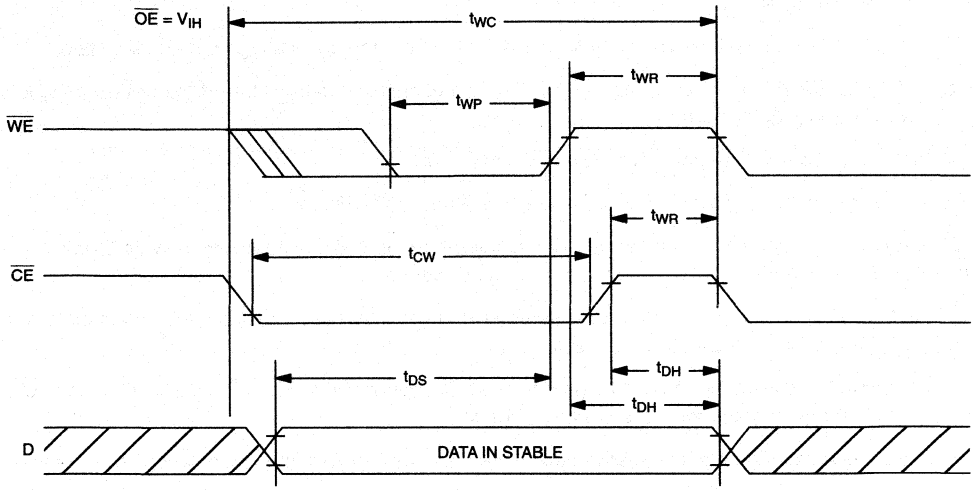
RESET FOR PHANTOM CLOCK



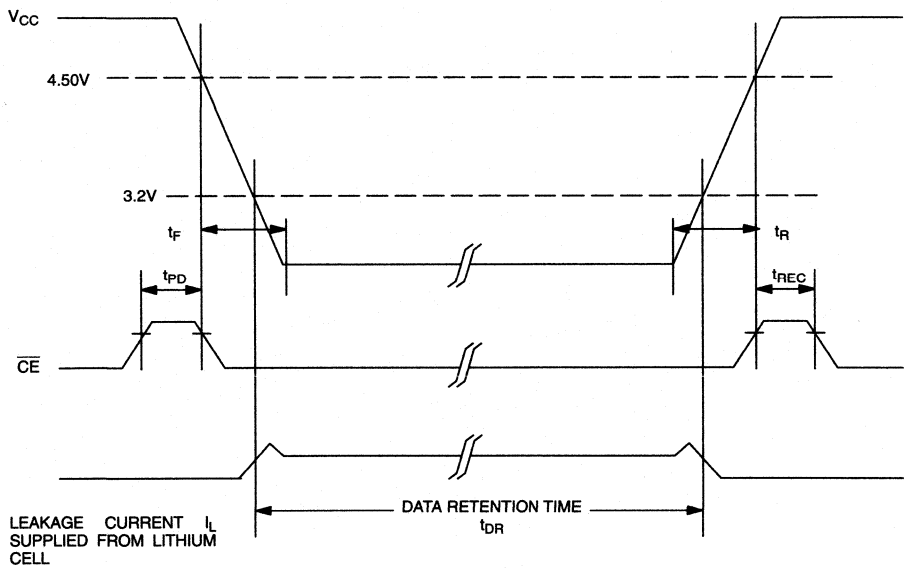
READ CYCLE TO PHANTOM CLOCK



WRITE CYCLE TO PHANTOM CLOCK



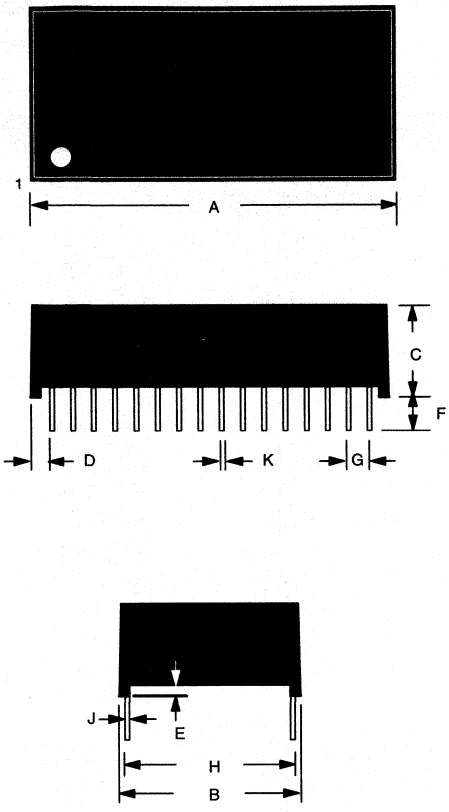
POWER-DOWN/POWER-UP CONDITION



NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 50 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} with the clock oscillator running.
10. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
11. t_{DH} and t_{DS} are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
12. $\overline{RST}$ (Pin1) has an internal pull-up resistor.

DS1248Y 1024K NV SRAM WITH PHANTOM CLOCK



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.720 43.69	1.740 44.20
B IN. MM	0.720 18.29	0.740 18.80
C IN. MM	0.395 10.03	0.415 10.54
D IN. MM	0.090 2.29	0.120 3.05
E IN. MM	0.017 0.43	0.030 0.76
F IN. MM	0.120 3.05	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

3

DALLAS SEMICONDUCTOR

DS1283
Watchdog Timekeeper Chip

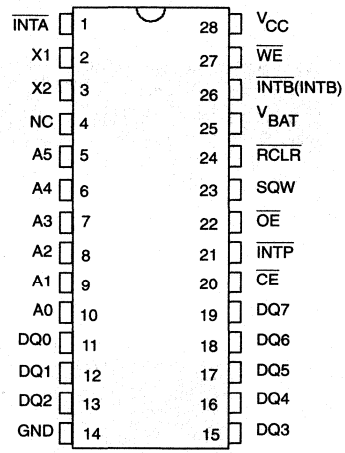
FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function provides notice of real time related occurrences
- Designed for battery operation
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±2 minutes/month at 25°C
- 50 bytes of user nonvolatile RAM
- Optional 28-pin SOIC surface mount package
- Low-power CMOS circuitry is maintained on less than 1 µA in standby mode

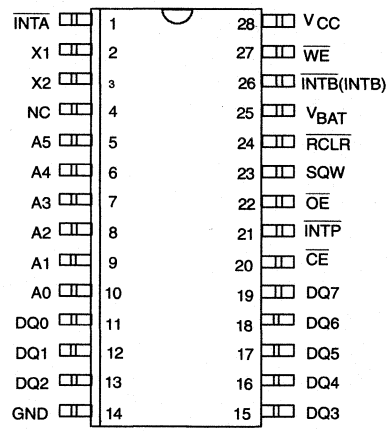
DESCRIPTION

The DS1283 Watchdog Timekeeper Chip is a self- contained real time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP or 28-pin SOIC surface mount package. The DS1283 is specifically designed to maintain internal operations from a single low voltage supply. In fact, the only two external components required by the DS1283 are a battery and crystal. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, V_{BAT}, V_{CC}, $\overline{RCLR}$, $\overline{INTB}$, and $\overline{INTP}$ see the DS1286 Watchdog Timekeeper data sheet.

PIN ASSIGNMENT



DS1283
28-Pin DIP (600 mil)



DS1283S
28-Pin SOIC (330 mil)

NOTE: Pin 4 must be left disconnected.

PIN DESCRIPTION

PIN #	NAME	I/O	DESCRIPTION
1	$\overline{INTA}$	O	Interrupt Output A (open drain)
2-3	X1,X2	I	32.768 KHz Crystal
4	NC	–	No Connection
5-10	A0-A5	I	Address Inputs: A5=Pin 5; A0=Pin 10
11	DQ0	I/O	Data Input/Output
12	DQ1	I/O	Data Input/Output
13	DQ2	I/O	Data Input/Output
14	GND	–	Ground
15	DQ3	I/O	Data Input/Output
16	DQ4	I/O	Data Input/Output
17	DQ5	I/O	Data Input/Output
18	DQ6	I/O	Data Input/Output
19	DQ7	I/O	Data Input/Output
20	$\overline{CE}$	I	Chip Enable
21	$\overline{INTP}$	O	Interrupt Output P (open drain)
22	$\overline{OE}$	I	Output Enable
23	SQW	O	Square Wave Output
24	$\overline{RCLR}$	I	RAM Clear
25	V_{BAT}	I	Battery Input
26	$\overline{INTB}$ (INTB)	O	Interrupt Output B (open drain)
27	$\overline{WE}$	I	Write Enable
28	V_{CC}	I	V_{CC} Input

PIN DESCRIPTIONS

X1, X2 – Connections for a standard 32.768 KHz quartz crystal, Daiwa part no. DT-26S, Seiko part no. DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a load capacitance (C_L) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks."

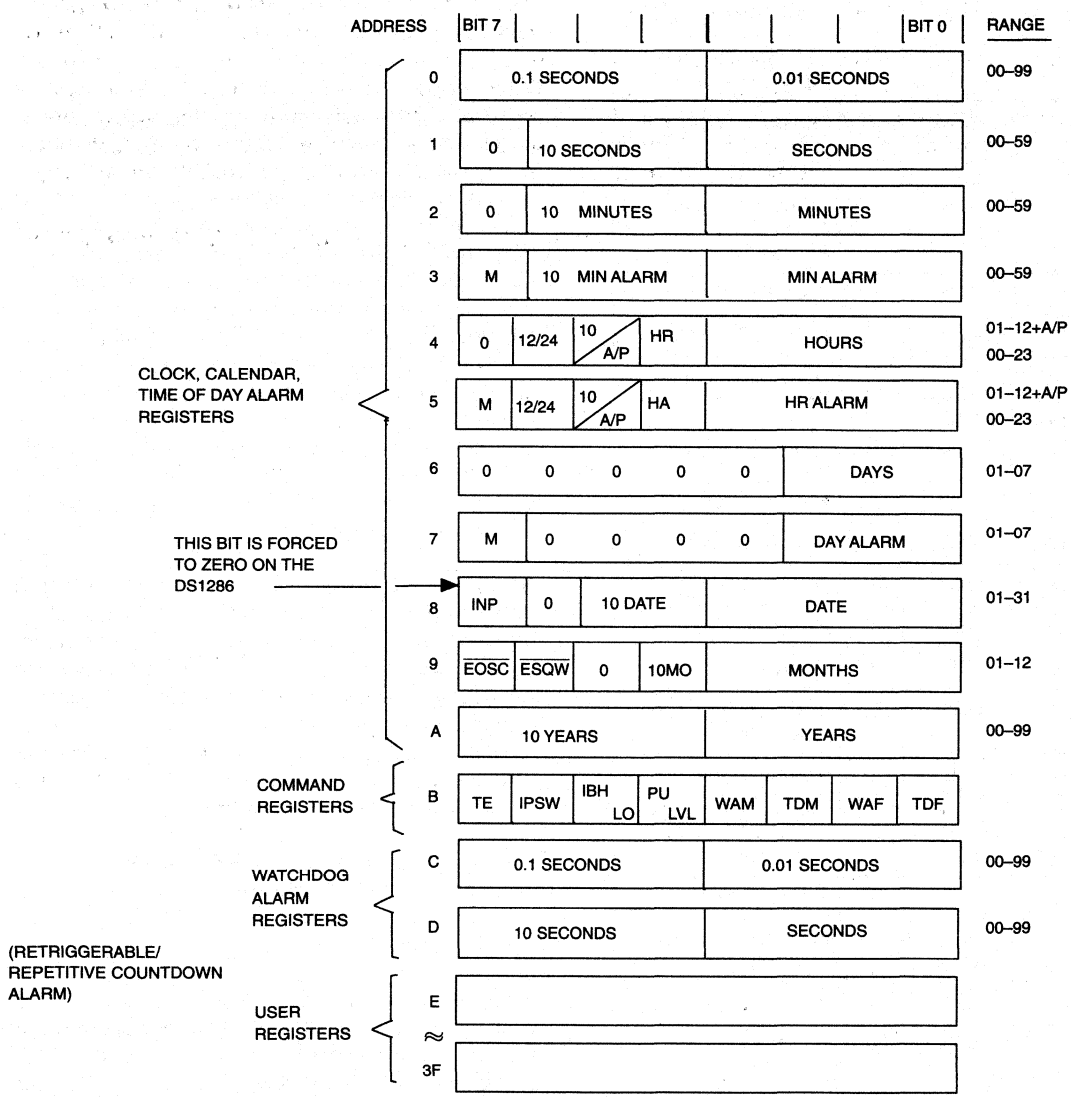
V_{BAT}, V_{CC} – Inputs for batteries or power supplies between 5.5 and 2.5 volts. The V_{CC} supply voltage should never exceed V_{BAT} + 0.3 volts. The V_{BAT} input is used to maintain all internal functions while the V_{CC} input is used to keep all inputs and outputs functional. Therefore, to keep the device fully functional, V_{BAT} and V_{CC} must be at the same voltage potential. As long as the supply voltages are between 4.5 and 5.5 volts, the timing and the input/output levels are guaranteed. In this mode, the active current drain is 2 mA ($CE=V_{IL}$) and the standby current drain is 0.5 mA ($CE=V_{IH}$). Data retention mode occurs when the V_{BAT} supply is between 5.5 and 2.5 volts and the V_{CC} supply is grounded. In the data retention mode the current drain is less than 1 µA maximum at 5.5 volts ($CE=V_{BAT}$–0.2 volts). The current drain specifications are stated with all outputs unloaded.

$\overline{RCLR}$ – The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 50 bytes of user nonvolatile RAM but does not affect the registers involved with time, alarm, and watchdog functions. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic 0 (-0.3 to +0.8 volts). The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up and should be left floating when not in use.

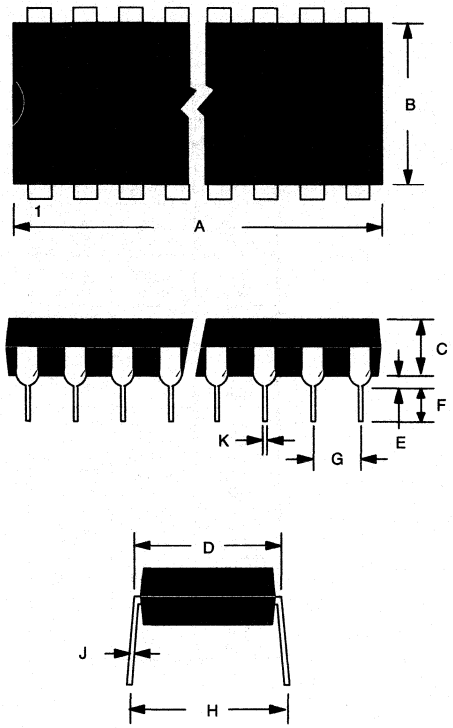
$\overline{INTB}$ – Interrupt B on the DS1283 operates identical to interrupt B on the DS1286 except that the sink and source current is limited to 500 µA. This pin should be pulled up or down if not used.

$\overline{INTP}$ – Interrupt P on the DS1283 was a missing or no connection pin on the DS1286. This interrupt works in the same manner as $\overline{INTA}$ as programmed by the IPSW bit. However, $\overline{INTP}$ is also logically ORed with the MSB of the date register (see Figure 1). This bit is called the INP bit on the DS1283 and is forced to zero on the DS1286. When the INP bit (interrupt P bit) is set to logical one, interrupt P will be held active low. When INP is set to logical zero, $\overline{INTP}$ is always at the same logic state as $\overline{INTA}$. This pin is an open drain capable of sinking 4 mA.

DS1283 WATCHDOG TIMEKEEPER REGISTERS Figure 1



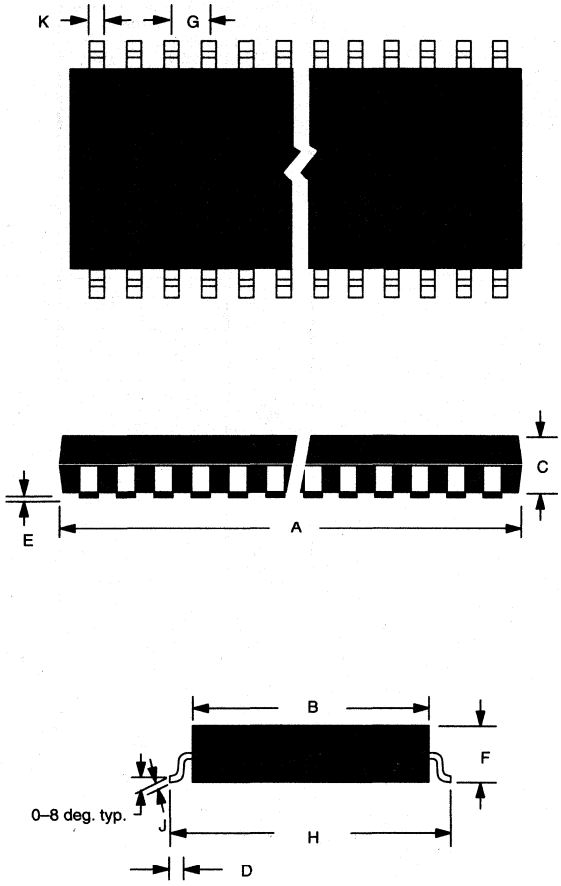
DS1283 28–PIN DIP



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.445	1.470
B IN. MM	0.530	0.550
C IN. MM	0.140	0.160
D IN. MM	0.600	0.625
E IN. MM	0.015	0.040
F IN. MM	0.120	0.145
G IN. MM	0.090	0.110
H IN. MM	0.625	0.675
J IN. MM	0.008	0.012
K IN. MM	0.015	0.022

3

DS1283 28–PIN SOIC



PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480 12.19
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51

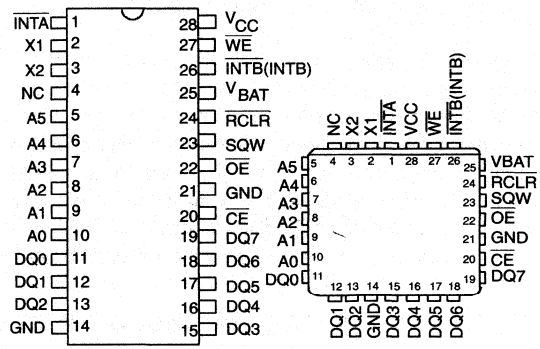
DALLAS SEMICONDUCTOR

DS1284
Watchdog Timekeeper Chip

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±2 minute/month at 25°C
- 50 bytes of user NV RAM
- Optional 28-pin PLCC surface mount package
- Low-power CMOS circuitry is maintained on less than 0.5 µA when power is supplied from battery input

PIN ASSIGNMENT



DS1284
28-Pin DIP (600 mil)

DS1284Q
28-Pin PLCC

PIN DESCRIPTION

$\overline{INTA}$	–	Interrupt Output A (open drain)
$\overline{INTB}$(INTB)	–	Interrupt Output B (open drain)
A0-A5	–	Address Inputs
DQ0-DQ7	–	Data Input/Output
$\overline{CE}$	–	Chip Enable
$\overline{OE}$	–	Output Enable
$\overline{WE}$	–	Write Enable
V_{CC}	–	+5 Volts
GND	–	Ground
NC	–	No Connection
SQW	–	Square Wave Output
X1,X2	–	32.768 KHz Crystal Connections
V_{BAT}	–	+3 Volt Battery Input
$\overline{RCLR}$	–	RAM Clear

DESCRIPTION

The DS1284 Watchdog Timekeeper Chip is a self-contained real-time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP package or a 28-pin PLCC surface mount package. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, V_{BAT}, and $\overline{RCLR}$, see the DS1286 Watchdog Timekeeper data sheet.

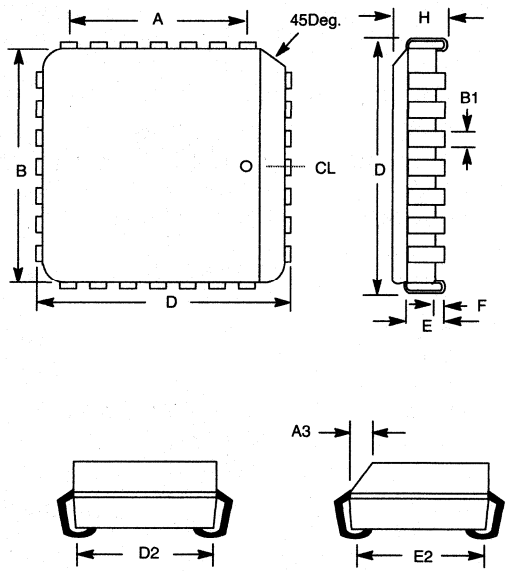
PIN DESCRIPTION

X1, X2 - Connections for a standard 32.768 KHz quartz crystal, Daiwa part part no. DT-26S, Seiko part no. DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks".

V_{BAT} - Battery input for any standard 3-volt lithium cell or other energy source. Battery voltage must be held between 2.4 and 3.7 volts for proper operation. The nominal write protect trip point voltage at which access to registers containing time, watchdog, alarm, and RAM information is denied is set by internal circuitry as 1.26 x V_{BAT}. A maximum load of 0.5 µA at 25°C in the absence of power should be used to size the external energy source. The battery should be connected directly to the V_{BAT} pin. A diode must not be placed in series with the battery to the V_{BAT} pin. Furthermore, a diode is not necessary because reverse charging current protection circuitry is provided internal to the device and has passed the requirements of Underwriters Laboratories for UL listing. An optional ground pin is provided for connection to battery negative. This pin should be grounded but can be left floating.

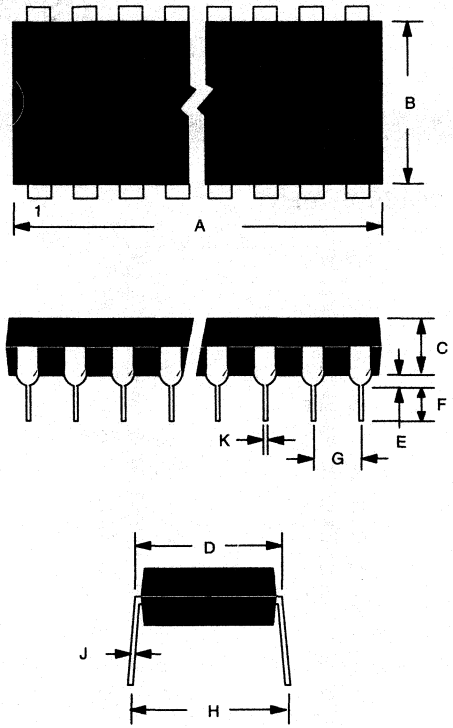
$\overline{\text{RCLR}}$ - The $\overline{\text{RCLR}}$ pin is used to clear (set to logic 1) all 50 bytes of user NV RAM but does not affect the registers involved with time, alarm, and watchdog functions. In order to clear the RAM, $\overline{\text{RCLR}}$ must be forced to an input logic zero (-0. 3 to +0.8 volts) during battery backup mode when V_{CC} is not applied. The $\overline{\text{RCLR}}$ function is designed to be used via human interface (shorting to ground or by switch) and not be driven with external buffers. This pin is internally pulled up and should be left floating when not in use.

DS1284Q 28–PIN PLCC WATCHDOG TIMEKEEPER



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.300 BSC 7.62	
B IN. MM	0.442 17.68	0.462 11.73
D IN. MM	0.480 12.2	0.500 12.7
D2 IN. MM	0.390 9.91	0.430 10.92
E IN. MM	0.090 2.29	0.120 3.05
E2 IN. MM	0.390 9.91	0.430 10.92
F IN. MM	0.015 0.38	0.020 0.518
H IN. MM	0.100 2.54	0.020 0.518

DS1284 28–PIN DIP WATCHDOG TIMEKEEPER



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.445	1.470
B IN. MM	0.530	0.550
C IN. MM	0.140	0.160
D IN. MM	0.600	0.625
E IN. MM	0.015	0.040
F IN. MM	0.120	0.145
G IN. MM	0.090	0.110
H IN. MM	0.625	0.675
J IN. MM	0.008	0.012
K IN. MM	0.015	0.022

3

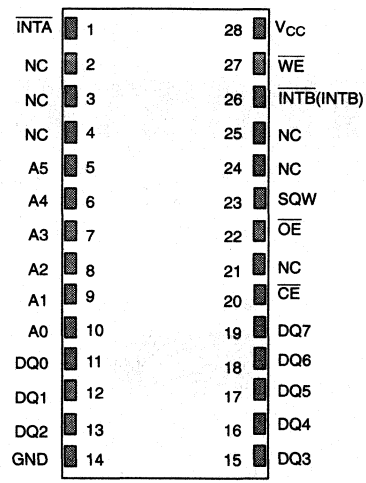
DALLAS SEMICONDUCTOR

DS1286
Watchdog Timekeeper

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real time-related activities
- Embedded lithium energy cell maintains time, watchdog, user RAM, and alarm information
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25°C
- Greater than 10 years of timekeeping in the absence of V_{CC}
- 50 bytes of user NV RAM

PIN ASSIGNMENT



28-Pin Encapsulated Package
(720 Mil Flush)

PIN DESCRIPTION

$\overline{INTA}$	-	Interrupt Output A (open drain)
$\overline{INTB}$(INTB)	-	Interrupt Output B (open drain)
A0-A5	-	Address Inputs
DQ0-DQ7	-	Data Input/Output
$\overline{CE}$	-	Chip Enable
$\overline{OE}$	-	Output Enable
$\overline{WE}$	-	Write Enable
V_{CC}	-	+5 Volts
GND	-	Ground
NC	-	No Connection
SQW	-	Square Wave Output

DESCRIPTION

The DS1286 Watchdog Timekeeper is a self-contained real time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP package. The DS1286 contains an embedded lithium energy source and a quartz crystal which eliminates the need for any external circuitry. Data contained within 64 eight-bit registers can be read or written in the same manner as bytewide static RAM. Data is maintained in the Watchdog Timekeeper by intelligent control circuitry which detects the status of V_{CC} and write protects memory when V_{CC} is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of V_{CC}. Watchdog Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date,

month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The Watchdog Timekeeper operates in either 24 hour or 12 hour format with an AM/PM indicator. The watchdog timer provides alarm windows and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week.

OPERATION - READ REGISTERS

The DS1286 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (High) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (Low). The unique address specified by the six address inputs (A0-A5) defines which of the 64 registers is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE REGISTERS

The DS1286 is in the write mode whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

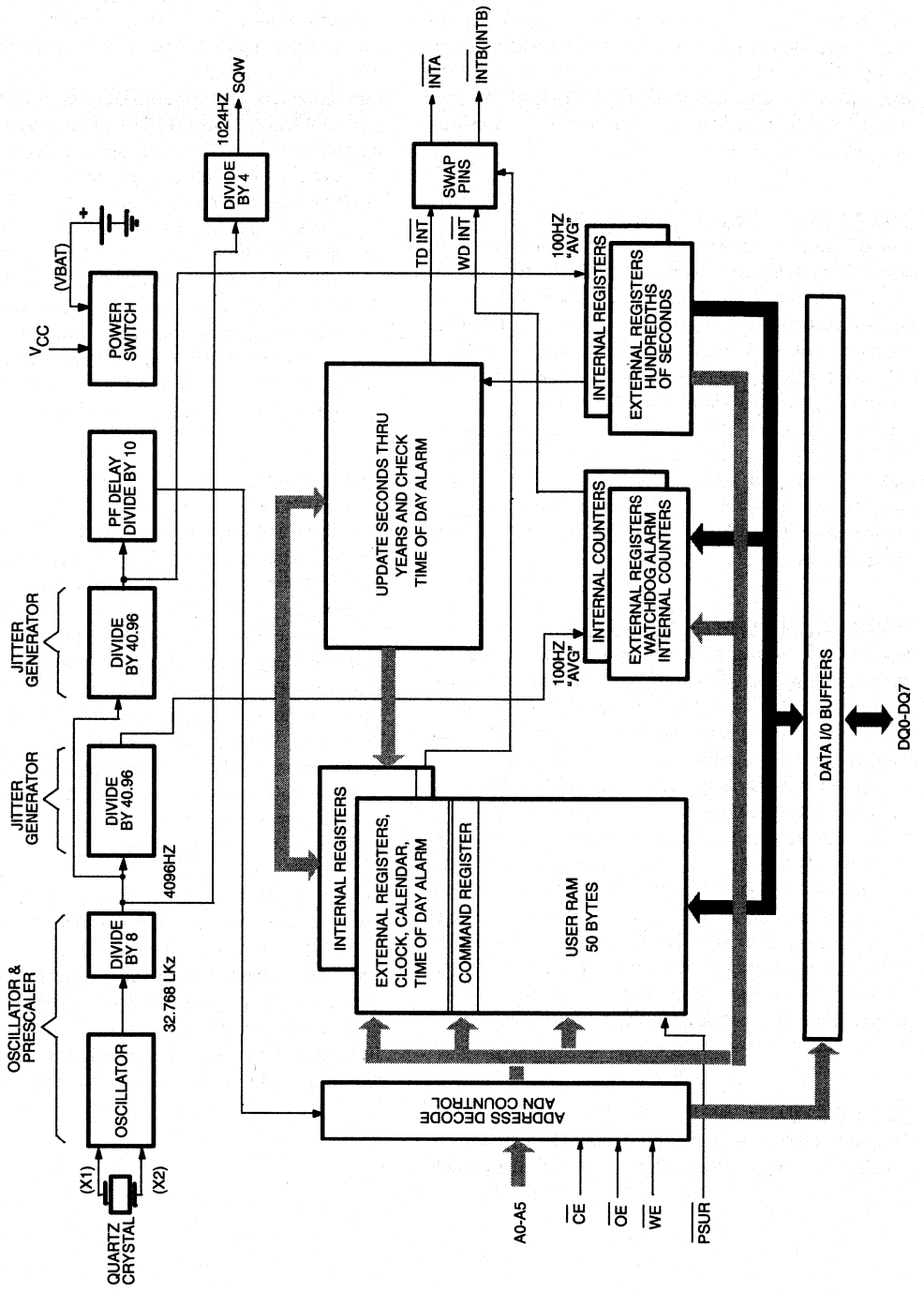
DATA RETENTION

The Watchdog Timekeeper provides full functional capability when V_{CC} is greater than 4.5 volts and write protects the register contents at 4.25 volts typical. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1286 constantly monitors V_{CC}. Should the supply voltage decay, the Watchdog Timekeeper will automatically write protect itself and all inputs to the registers become Don't Care. The two interrupts $\overline{INTA}$ and $\overline{INTB}$ (INTB) and the internal clock and timers continue to run regardless of the level of V_{CC}. However, if the active high mode is selected for $\overline{INTB}$(INTB), this pin will only go high in the presence of V_{CC}. As V_{CC} falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} and disconnects the internal lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for a period of 150 ms.

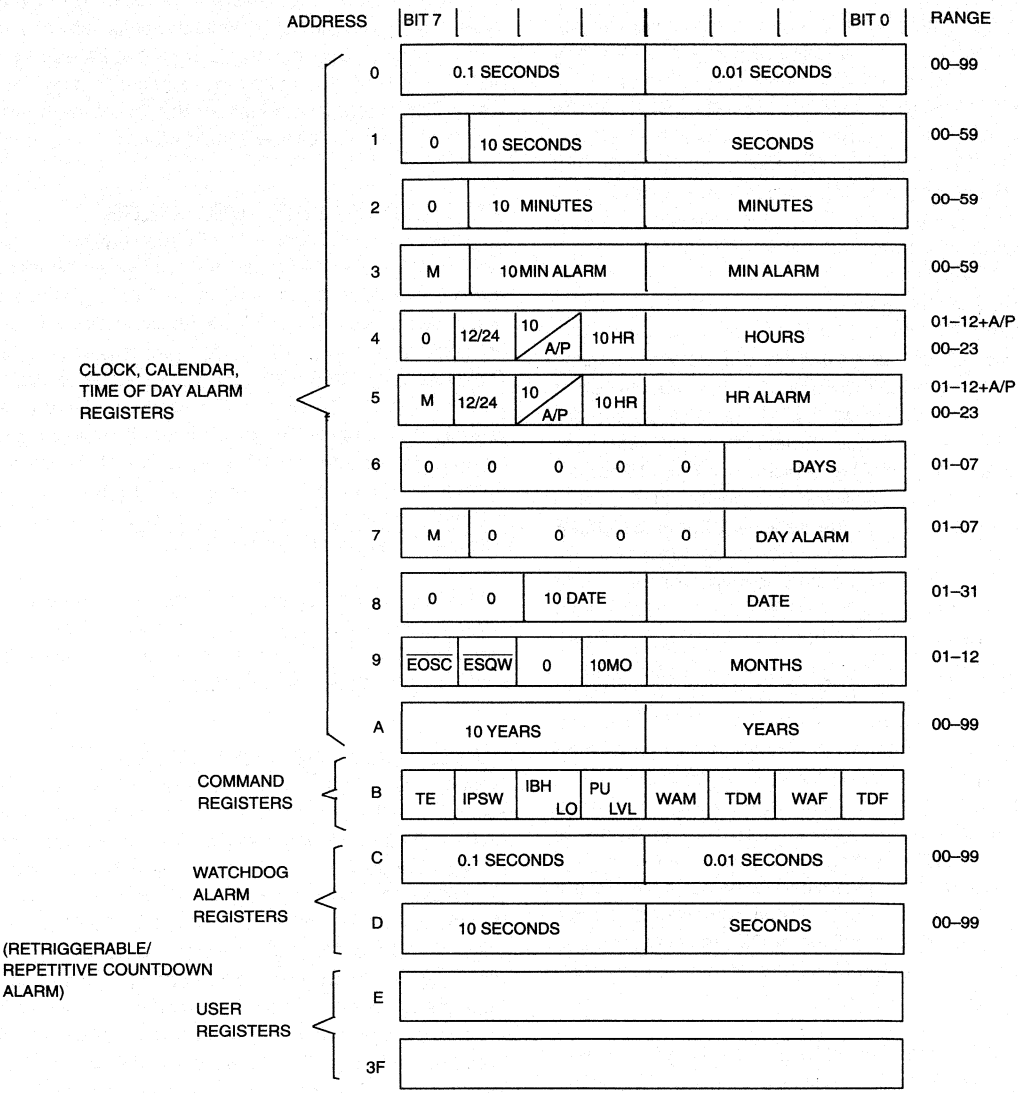
WATCHDOG TIMEKEEPER REGISTERS

The Watchdog Timekeeper has 64 registers which are eight bits wide that contain all of the Timekeeping, Alarm, Watchdog, Control, and Data information. The Clock, Calendar, Alarm, and Watchdog registers are memory locations which contain external (user-accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 50 bytes of RAM registers can only be accessed from the external address and data bus. Registers 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of Day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm registers and information which is stored in these two registers is in BCD. Registers E through 3F are user bytes and can be used to contain data at the user's discretion.

BLOCK DIAGRAM Figure 1



DS1286 WATCHDOG TIMEKEEPER REGISTERS Figure 2



TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic zero, $\overline{EOSC}$ (bit 7) enables the Real Time Clock oscillator. This bit is set to logic one as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the Square Wave Output (Pin 23). When set to logic zero, the Square Wave Output pin will output a 1024 Hz Square Wave Signal. When set to logic one the Square Wave Output pin is in a high impedance state. Bit 6 of the Hours Register is defined as the 12- or 24- hour Select Bit. When set to logic one, the 12-hour format is selected. In the 12-hour format, bit 5 is the AM/PM bit with logic one being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours). The Time of Day registers are updated every .01 seconds from the real time clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the Watchdog Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable) to a logic zero. This will freeze the External Time of Day registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic one, will put the Time of Day registers back to being updated every .01 second. No time is lost in the real time clock because the internal copy of the Time of Day register buffers is continually incremented while the external memory registers are frozen.

An alternate method of reading and writing the Time of Day registers is to ignore synchronization. However, any single read may give erroneous data as the real time clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented and Time of Day Alarm is checked during the period that hundreds of seconds read 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the Watchdog Timekeeper.

TIME OF DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the Time of Day Alarm registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logic zero, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic one. Similarly, an alarm is generated every hour when bit 7 of Registers 7 and 5 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm registers are written and read in the same format as the Time of Day registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm registers are read or written.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Registers C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer countdown is interrupted and reinitialized back to the entered value every time either of the registers is accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from ever going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm registers always read the entered value. The actual countdown register is internal and is not readable. Writing Registers C and D to zero will disable the Watchdog Alarm feature.

COMMAND REGISTER

Address location 0B is the Command Register where mask bits, control bits, and flag bits reside. Bit 0 is the Time of Day Alarm Flag (TDF). When this bit is set internally to a logic one, an alarm has occurred. The time of the alarm can be determined by reading the Time of Day Alarm registers. However, if the transfer enable bit is set to logic zero the Time of Day registers may not reflect the exact time that the alarm occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Time of Day Alarm registers are read. Bit 1 is the Watchdog Alarm Flag (WAF). When this bit is set internally to a logic one, a Watchdog Alarm has occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Watchdog Alarm registers are accessed. Bit 2 of the Command Register contains the Time of Day Alarm Mask Bit (TDM). When this bit is written to a logic one, the Time of Day Alarm Interrupt Output is deactivated regardless of the value of the Time of Day Alarm Flag. When TDM is set to logic zero, the Time of Day Interrupt Output will go to the active state which is determined by bits 0, 4, 5, and 6 of the Command Register. Bit 3 of the Command Register contains the Watchdog Alarm Mask bit (WAM). When this bit is written to a logic one, the Watchdog Interrupt Output is deactivated regardless of the value in the Watchdog Alarm registers. When WAM is set to logic zero, the Watchdog Interrupt Output will go to the active state which is determined by bits 1, 4, 5, and 6 of the Command Register. These four bits define how Interrupt Output Pins $\overline{INTA}$ and $\overline{INTB}$ (INTB) will be operated. Bit 4 of the Command Register determines whether both interrupts will output a pulse or level when activated. If Bit 4 is set to logic one, the pulse mode is selected and $\overline{INTA}$ will sink current for a minimum of 3 ms and then release. Output $\overline{INTB}$ (INTB) will either sink or source current for a minimum of 3 ms depending on the level of bit 5. When bit 5 is set to logic one, the B interrupt will source current. When bit 5 is set to logic zero, the B interrupt will sink current. Bit 6 of the Command Register directs which type of interrupt will be present on interrupt pins $\overline{INTA}$ or $\overline{INTB}$(INTB). When set to logic one, $\overline{INTA}$ becomes the Time of Day Alarm Interrupt pin and $\overline{INTB}$(INTB) becomes the Watchdog Interrupt pin. When bit 6 is set to logic zero, the interrupt functions are reversed such that the Time of Day Alarm will be output on $\overline{INTB}$(INTB) and the Watchdog Interrupt will be output on $\overline{INTA}$. Caution should be exercised when dynamically setting this bit as the interrupts will be reversed even if in an active state. Bit 7 of the Command Register is for Transfer Enable (TE). The function of this bit is described in the Time of Day registers.

3

TIME OF DAY ALARM MASK BITS Figure 3

REGISTER			
(3)MINUTES	(5)HOURS	(7)DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	10
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	10
Input Logic 0	V_{IL}	-0.3		+0.8	V	10

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
Output Leakage Current	I_{LO}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LIO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	13
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE}$ > V_{CC} -0.5	I_{CCS2}			4.0	mA	
Active Current	I_{CC}			15	mA	
Write Protection Voltage	V_{TP}		4.25		V	

CAPACITANCE

(t_A=25°C)

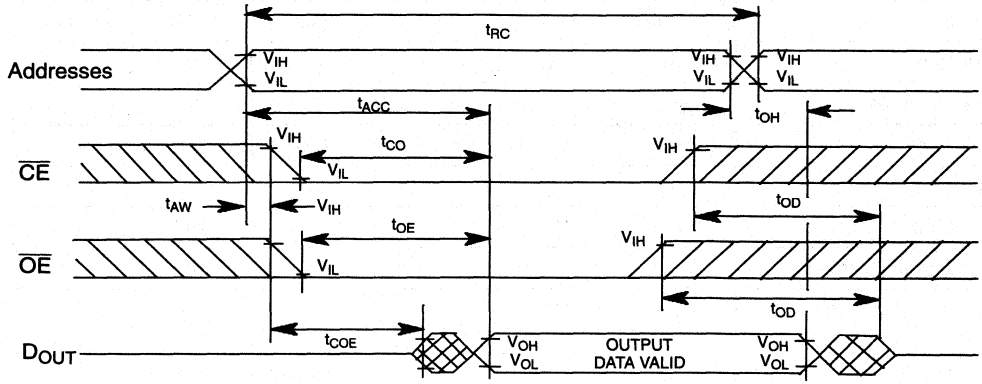
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		7	10	pF	
Output Capacitance	C_{OUT}		7	10	pF	
Input/Output Capacitance	$C_{I/O}$		7	10	pF	

AC ELECTRICAL CHARACTERISTICS

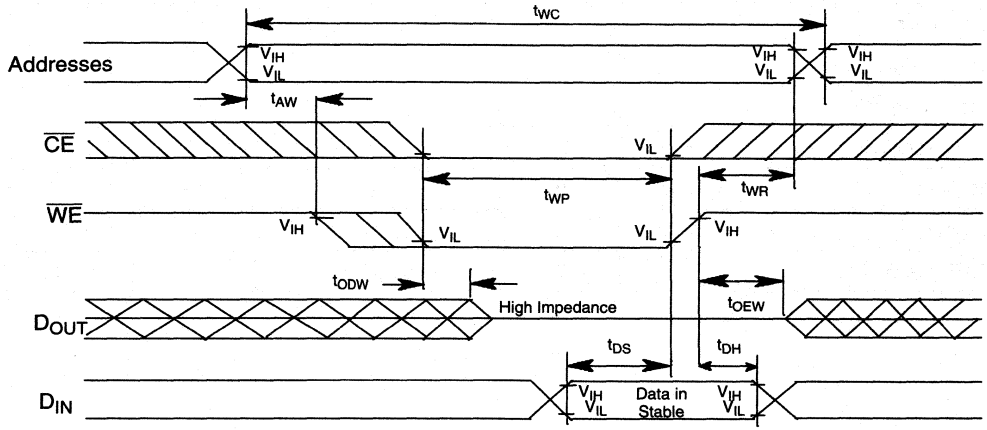
(0°C to 70° C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150			ns	1
Address Access Time	t_{ACC}			150	ns	
$\overline{CE}$ Access Time	t_{CO}			150	ns	
$\overline{OE}$ Access Time	t_{OE}			60	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10			ns	
Output High Z from Deselect	t_{OD}			60	ns	
Output Hold from Address Change	t_{OH}	10			ns	
Write Cycle Time	t_{WC}	150			ns	
Write Pulse Width	t_{WP}	140			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	10			ns	
Output High Z from $\overline{WE}$	t_{ODW}			50	ns	
Output Active from $\overline{WE}$	t_{OEW}	10			ns	
Data Setup Time	t_{DS}	45			ns	4
Data Hold Time	t_{DH}	0			ns	4,5
$\overline{INTA}$, $\overline{INTB}$ Pulse Width	t_{IPW}	3			ms	11,12

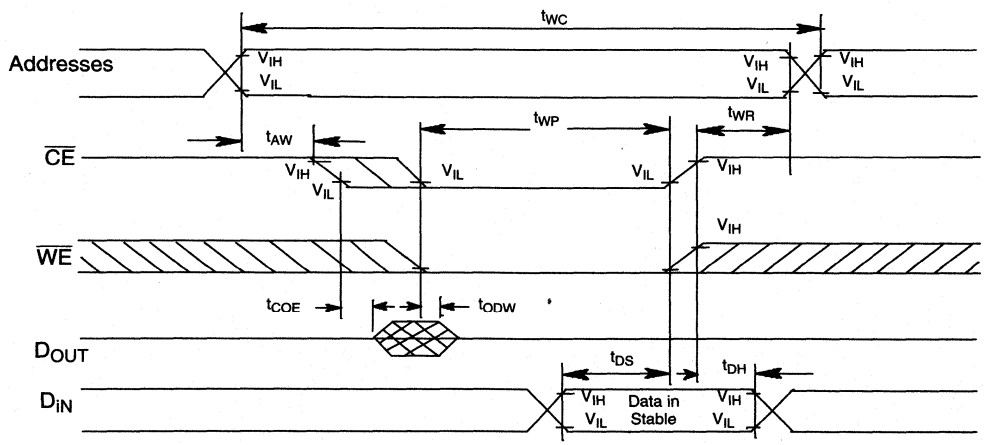
READ CYCLE (NOTE1)



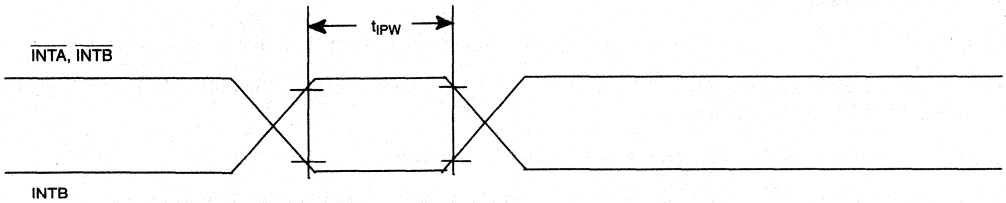
WRITE CYCLE 1 (Notes 2, 6, 7)



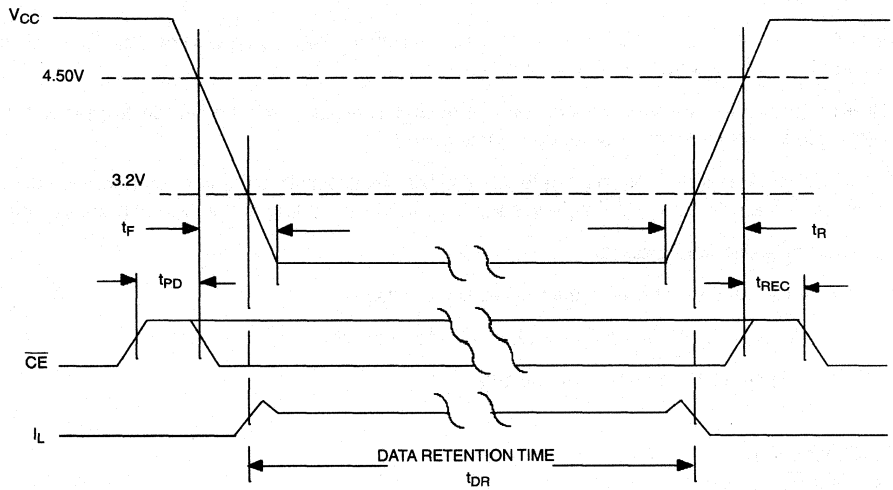
WRITE CYCLE 2 (Notes 2, 8)



TIMING DIAGRAM: INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



POWER-DOWN/POWER-UP CONDITION



Current, I_L, Supplied from Lithium Cell

POWER-UP/POWER-DOWN CONDITION

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	t_F	350			µs	
V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	100			µs	
$\overline{CE}$ at V_{IH} after Power Up	t_{REC}			150	ms	

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

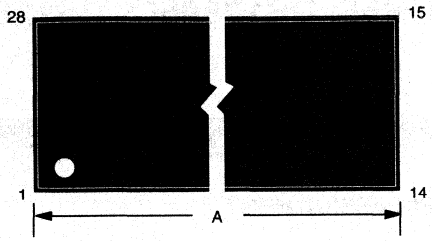
NOTES:

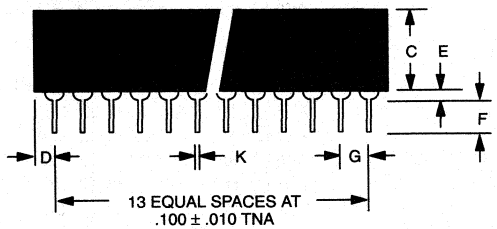
1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of the $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} or t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle, then t_{DH} = 20 ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1286 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All voltages are referenced to ground.
11. Applies to both interrupt pins when the alarms are set to pulse.
12. Interrupt output occurs within 100 ns on the alarm condition existing.
13. Both $\overline{INTA}$ and $\overline{INTB}$(INTB) are open drain outputs.

AC TEST CONDITIONS

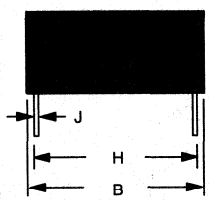
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns.

DS1286 WATCHDOG TIMEKEEPER





PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



NOTE: PINS 2, 3, 21, 24 AND 25 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

DS12885, DS12885Q, DS12885T
Real Time Clock

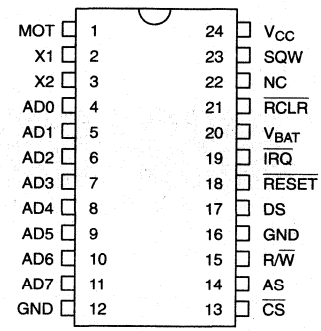
FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin configuration closely matches MC146818B and DS1285
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End of clock update cycle
- Optional 28-pin PLCC surface mount package

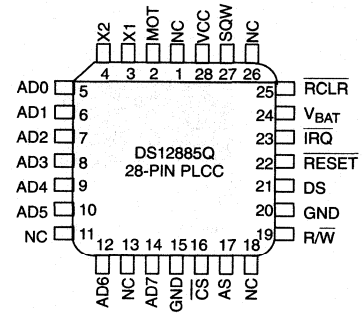
DESCRIPTION

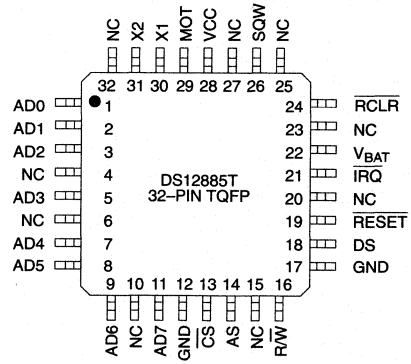
The DS12885 Real Time Clock plus RAM is designed to be a direct replacement for the DS1285. The DS12885 is identical in form, fit, and function to the DS1285, and has an additional 64 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, V_{BAT}, and $\overline{RCLR}$, see the DS12887 data sheet.

PIN ASSIGNMENT



DS12885 24–PIN DIP
DS12885S 24–PIN SOIC





PIN DESCRIPTION

AD0-AD7	-	Multiplexed Address/Data Bus
NC	-	No Connection
MOT	-	Bus Type Selection
$\overline{CS}$	-	Chip Select
AS	-	Address Strobe
R/$\overline{W}$	-	Read/Write Input
DS	-	Data Strobe
$\overline{RESET}$	-	Reset Input
$\overline{IRQ}$	-	Interrupt Request Output (open drain)
SQW	-	Square Wave Output
V_{CC}	-	+5 Volt Supply
GND	-	Ground
X1,X2	-	32.768 kHz Crystal Connections
V_{BAT}	-	+3 volt Battery Input
$\overline{RCLR}$	-	RAM Clear

PIN DESCRIPTION

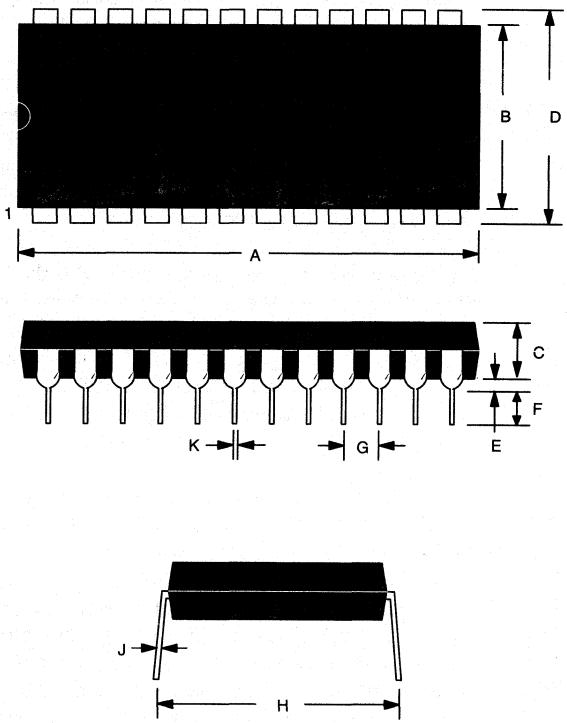
X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S, Seiko part number DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks".

V_{BAT} - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 4 volts for proper operation. A maximum load of .5 µA at 25°C in the absence of power should be used to size the external energy source.

The battery should be connected directly to the V_{BAT} pin. A diode must not be placed in series with the battery to the V_{BAT} pin. Furthermore, a diode is not necessary because reverse charging current protection circuitry is provided internal to the device and has passed the requirements of Underwriters Laboratories for UL listing.

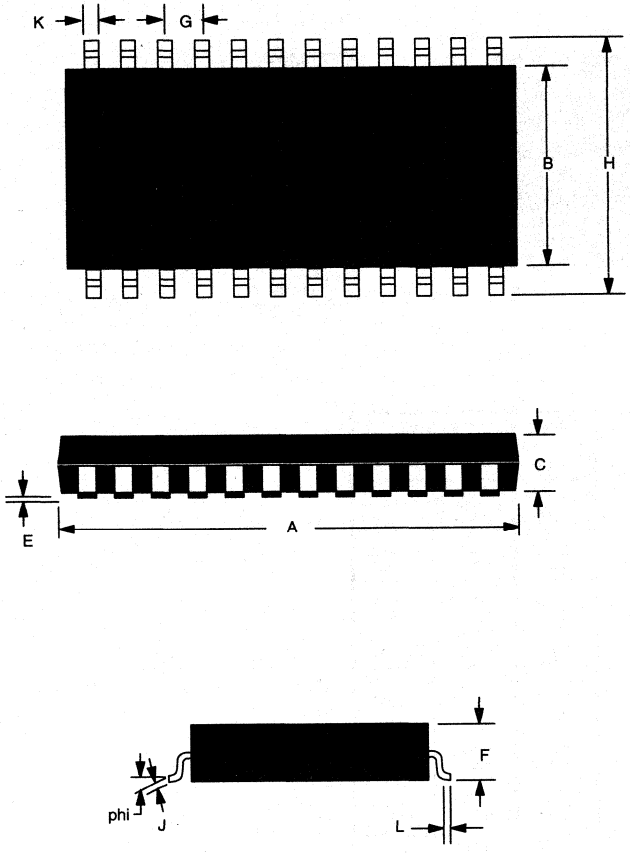
$\overline{RCLR}$ - The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 114 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic 0 (-0.3 to +0.8 volts) during battery back-up mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up. Do not use an external pull–up resistor on this pin.

DS12885 24–PIN DIP



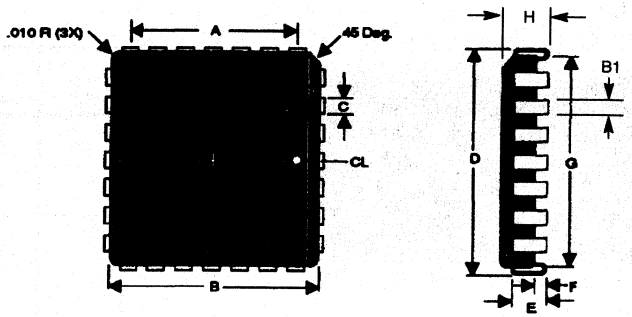
PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN.	1.245	1.270
MM	31.62	32.25
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.145	0.165
MM	3.68	4.19
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.050
MM	0.380	1.27
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.559

DS12885 24–PIN SOIC



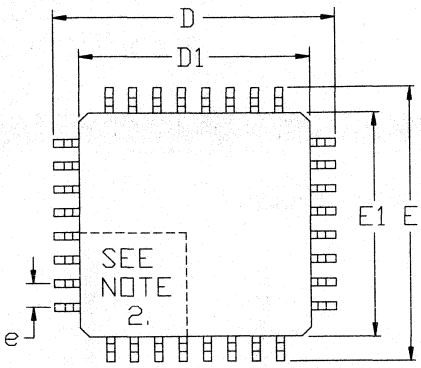
PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.602 15.29	0.612 15.54
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN. MM	0.016 0.406	0.040 1.02
phi	0°	8°

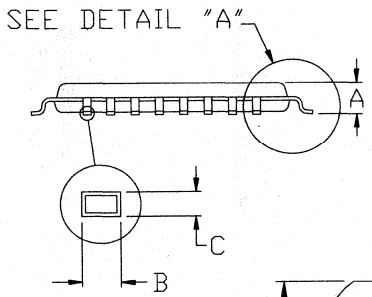
DS12885Q 28–PIN PLCC



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.300 REF 7.62	
B IN. MM	0.442 17.68	0.462 11.73
B1 IN. MM	0.013 0.33	0.021 0.53
C IN. MM	0.027 0.68	0.033 0.84
D IN. MM	0.480 12.2	0.500 12.7
E IN. MM	0.090 2.29	0.120 3.05
F IN. MM	0.020 0.51	MIN MIN
G IN. MM	0.390 9.91	0.430 10.92
H IN. MM	0.165 4.19	0.180 4.57

DS12885T 32-PIN TQFP

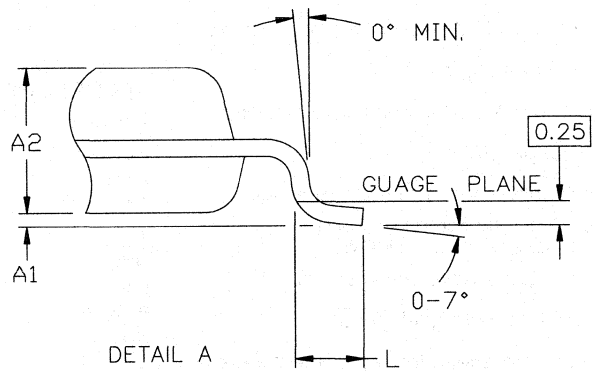




DIM	MIN	MAX
A	–	1.20
A1	0.05	0.15
A2	0.95	1.05
D	8.80	9.20
D1	7.00 BSC	
E	8.80	9.20
E1	7.00 BSC	
L	0.45	0.75
e	0.80 BSC	
B	0.30	0.45
C	0.09	0.20

NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; AT MAXIMUM MATERIAL CONDITION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. CONTROLLING DIMENSIONS: MILLIMETERS.



DIMENSIONS ARE IN MILLIMETERS

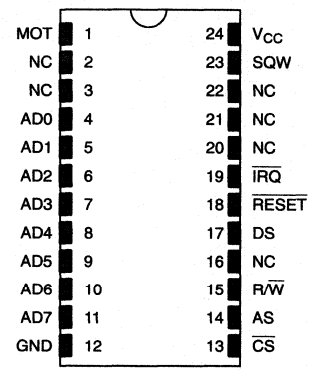
DALLAS SEMICONDUCTOR

DS12887
Real Time Clock

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818B and DS1287
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End of clock update cycle

PIN ASSIGNMENT



24 PIN ENCAPSULATED PACKAGE

PIN DESCRIPTION

AD0-AD7	-	Multiplexed Address/Data Bus
NC	-	No Connection
MOT	-	Bus Type Selection
$\overline{CS}$	-	Chip Select
AS	-	Address Strobe
R/$\overline{W}$	-	Read/Write Input
DS	-	Data Strobe
$\overline{RESET}$	-	Reset Input
$\overline{IRQ}$	-	Interrupt Request Output
SQW	-	Square Wave Output
V_{CC}	-	+5 Volt Supply
GND	-	Ground

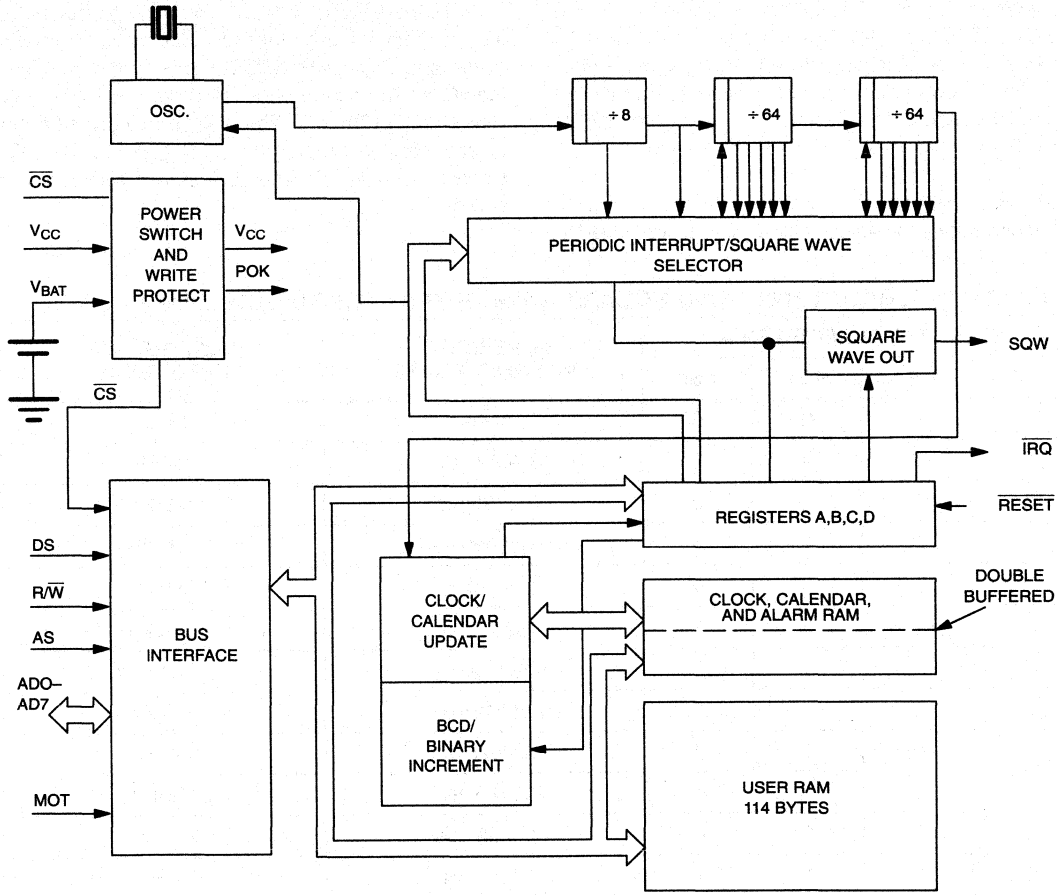
DESCRIPTION

The DS12887 Real Time Clock plus RAM is designed to be a direct replacement for the DS1287. The DS12887 is identical in form, fit, and function to the DS1287, and has an additional 64 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. A lithium energy source, quartz crystal, and write-protection circuitry are contained within a 24-pin dual in-line package. As such, the DS12887 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 114 bytes of nonvolatile static RAM. The real time clock is distinctive in that time-of-day and memory are maintained even in the absence of power.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS12887. The following paragraphs describe the function of each pin.

BLOCK DIAGRAM DS12887 Figure 1



POWER-DOWN/POWER-UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS12887 and reaches a level of greater than 4.25 volts, the device becomes accessible after 200 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts, the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin. The DS12887 is, therefore, write-protected. When the DS12887 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When V_{CC} falls below a level of approximately 3 volts, the external V_{CC} supply is switched off and an internal lithium energy source supplies power to the Real Time Clock and the RAM memory.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to an internal lithium energy source. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select) - The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 KΩ.

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 1

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz
0	1	1	0	976.5625 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS12887 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the DS12887 latches the address from AD0 to AD6. Valid write data must be present and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle the DS12887 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as $\overline{RD}$ transitions high in the case of Intel timing.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS12887.

DS (Data Strobe or Read Input) - The DS/$\overline{RD}$ pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS12887 is to drive the bidirectional bus. In write cycles the trailing edge of DS causes the DS12887 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read($\overline{RD}$). $\overline{RD}$ identifies the time period when the DS12887 drives the bus with read data. The $\overline{RD}$ signal is the same definition as the Output Enable ($\overline{OE}$) signal on a typical memory.

R/$\overline{W}$ (Read/Write Input)-The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/$\overline{W}$ is at a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active low signal called $\overline{WR}$. In this mode the R/$\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{WE}$) on generic RAMs.

$\overline{CS}$ (Chip Select Input) - The Chip Select signal must be asserted low for a bus cycle in the DS12887 to be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during $\overline{RD}$ and $\overline{WR}$ for Intel timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur. When V_{CC} is below 4.25 volts, the DS12887 internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the real time clock data and RAM data during power outages.

$\overline{IRQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS12887 that can be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

$\overline{RESET}$ (Reset Input) - The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{RESET}$ pin can be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power-up, the time $\overline{RESET}$ is low should exceed 200 ms to make sure that the internal timer that controls the DS12887 on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above 4.25 volts, the follow ing occurs:

A. Periodic Interrupt Enable (PEI) bit is cleared to zero.
B. Alarm Interrupt Enable (AIE) bit is cleared to zero.
C. Update Ended Interrupt Flag (UF) bit is cleared to zero.
D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.
E. Periodic Interrupt Flag (PF) bit is cleared to zero.
F. The device is not accessible until $\overline{RESET}$ is returned high.
G. Alarm Interrupt Flag (AF) bit is cleared to zero.
H. $\overline{IRQ}$ pin is in the high impedance state.
I. Square Wave Output Enable ($\overline{SQWE}$) bit is cleared to zero.
J. Update Ended Interrupt Enable (UIE) is cleared to zero.

In a typical application $\overline{RESET}$ can be connected to V_{CC}. This connection will allow the DS12887 to go in and out of power fail without affecting any of the control registers.

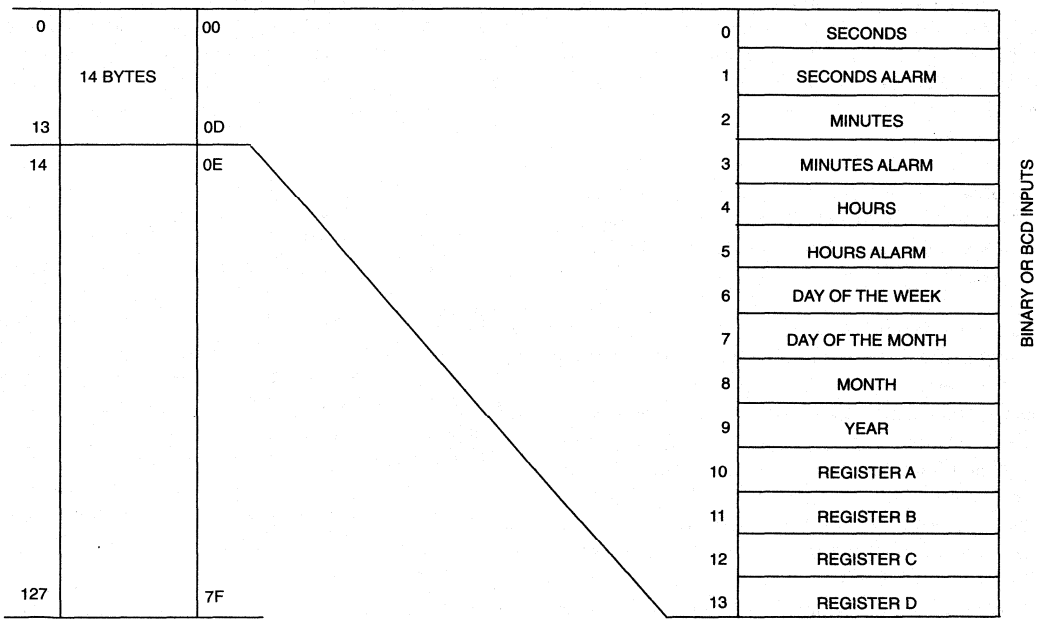
ADDRESS MAP

The address map of the DS12887 is shown in Figure 2. The address map consists of 114 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 128 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

The contents of four registers (A,B,C, and D) are described in the "Registers" section.

ADDRESS MAP DS12887 Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar, and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The 24-12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and

checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

3

TIME, CALENDAR AND ALARM DATA MODES Table 2

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

NONVOLATILE RAM

The 114 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS12887. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A zero in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases

where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts a re lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS12887. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS12887 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The DS12887 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Reg-

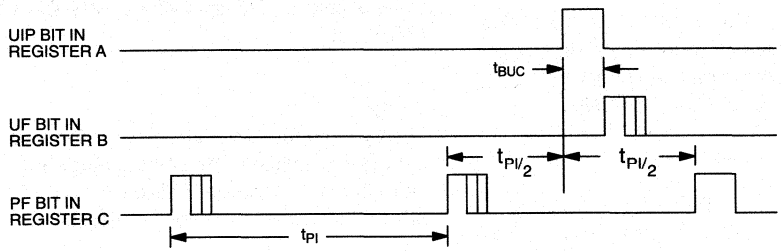
ister C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within 1 ($t_{PI/2}$ + t_{BUC}) to ensure that data is not read during the update cycle.

3

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS12887 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2

These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1, and DV2.

RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by $\overline{RESET}$.

REGISTER B

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by $\overline{RESET}$ or internal functions of the DS12887.

PIE

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS12887 functions, but is cleared to zero on $\overline{RESET}$.

AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The $\overline{RESET}$ pin clears AIE to zero. The internal functions of the DS12887 do not affect the AIE bit.

UIE

The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The $\overline{RESET}$ pin going low or the SET bit going high clears to UIE bit.

SQWE

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the $\overline{RESET}$ pin. SQWE is a read/write bit.

DM

The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{RESET}$. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write and is not affected by internal functions of $\overline{RESET}$.

DSE

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or $\overline{RESET}$.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF

The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

That is, IRQF = PF • PIE + AF • AIE + UF • UIE.

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{RESET}$ pin is low.

PF

The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{RESET}$ or a software read of Register C.

AF

A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A $\overline{RESET}$ or a read of Register C will clear AF.

UF

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C or a $\overline{RESET}$.

BIT 0 THROUGH BIT 3

These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT

The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{RESET}$.

BIT 6 THROUGH BIT 0

The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		7	15	mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	4
Input Current	I_{MOT}	-1.0		+500	µA	3
Output @ 2.4V	I_{OH}	-1.0			mA	1,5
Output @ 0.4V	I_{OL}			4.0	mA	1
Write Protect Voltage	V_{TP}	4.0	4.25	4.5	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

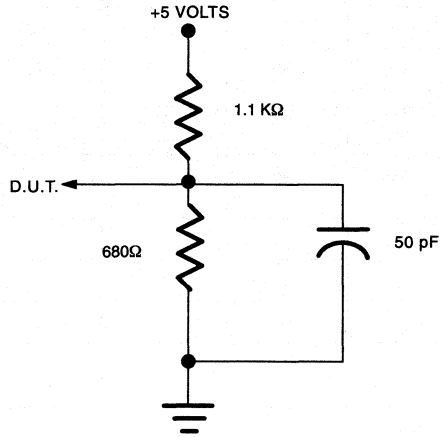
(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	385		DC	ns	
Pulse Width, DS/E Low or RD/$\overline{WR}$ High	PW_{EL}	150			ns	
Pulse Width, DS/E High or RD/$\overline{WR}$ Low	PW_{EH}	125			ns	
Input Rise and Fall Time	t_R,t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	50			ns	
Chip Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to AS/ ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	20			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	40			ns	
Output Data Delay Time From DS/E or $\overline{RD}$	t_{DDR}	20		120	ns	6
Data Setup Time	t_{DSW}	100			ns	
Reset Pulse Width	t_{RWL}	5			µs	
$\overline{IRQ}$ Release from DS	t_{IRDS}			2	µs	
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}			2	µs	

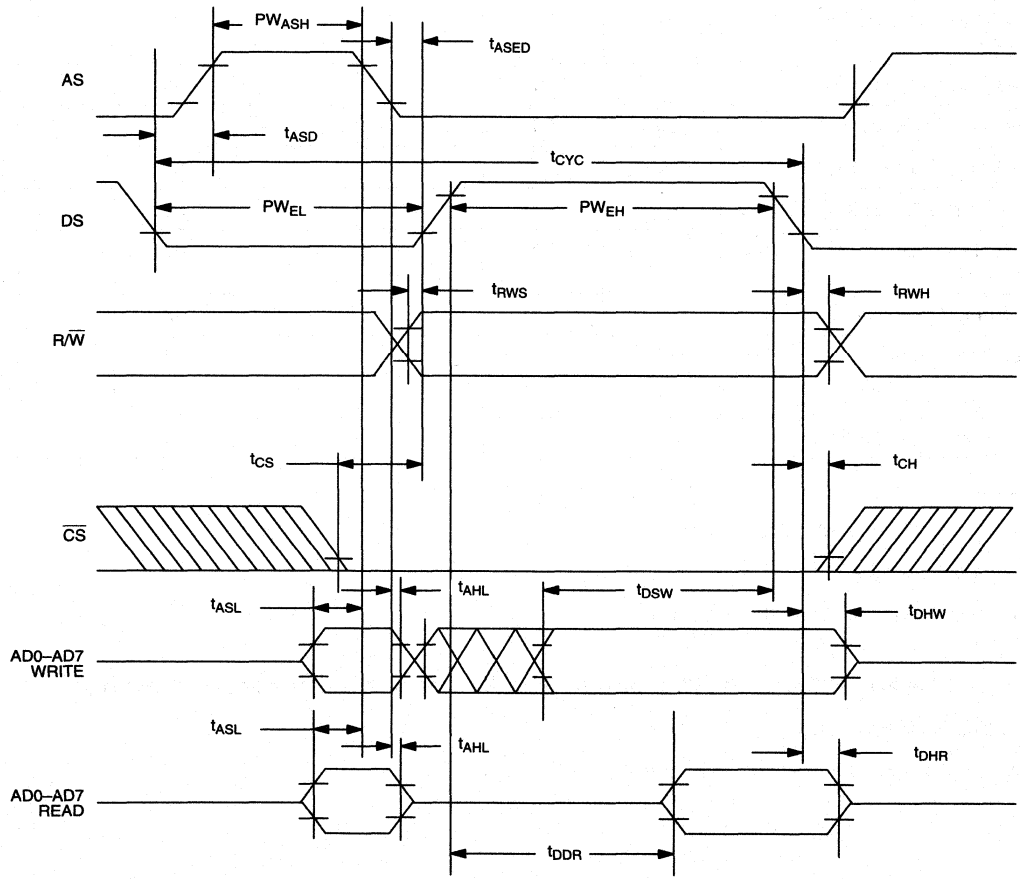
NOTES:

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pulldown of 20 KΩ.
4. Applies to the AD0-AD7 pins, the $\overline{IRQ}$ pin,and the SQW pin when each is in the high impedance state.
5. The $\overline{IRQ}$ pin is open drain.
6. Measured with a load as shown in Figure 4.

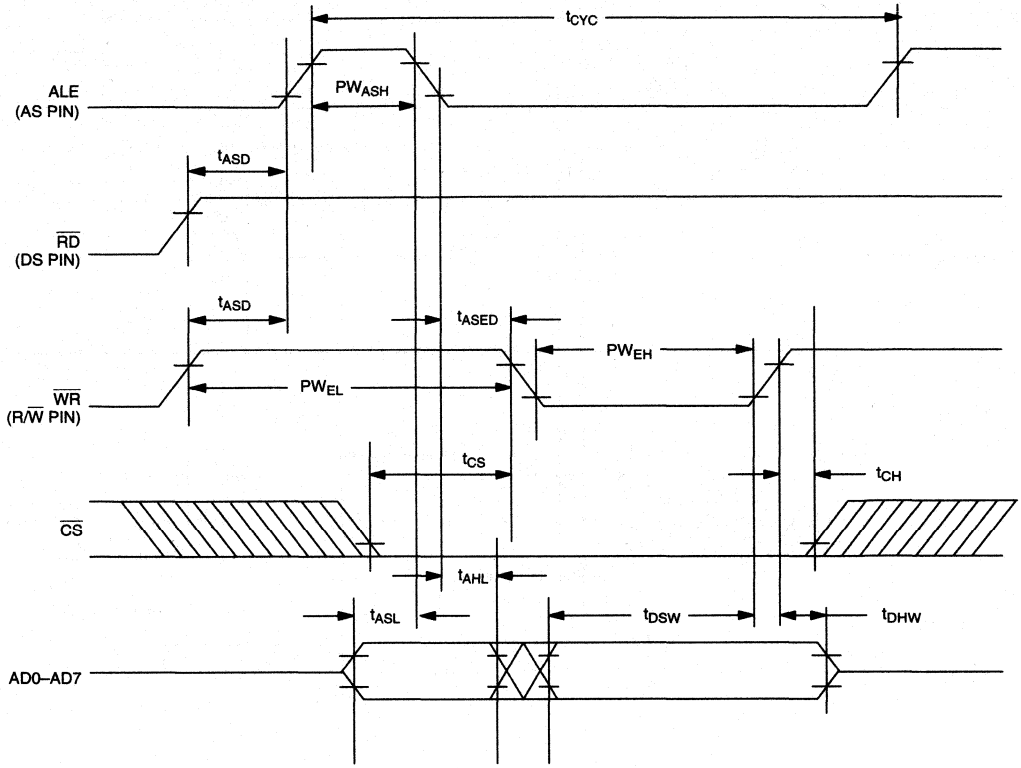
OUTPUT LOAD Figure 4



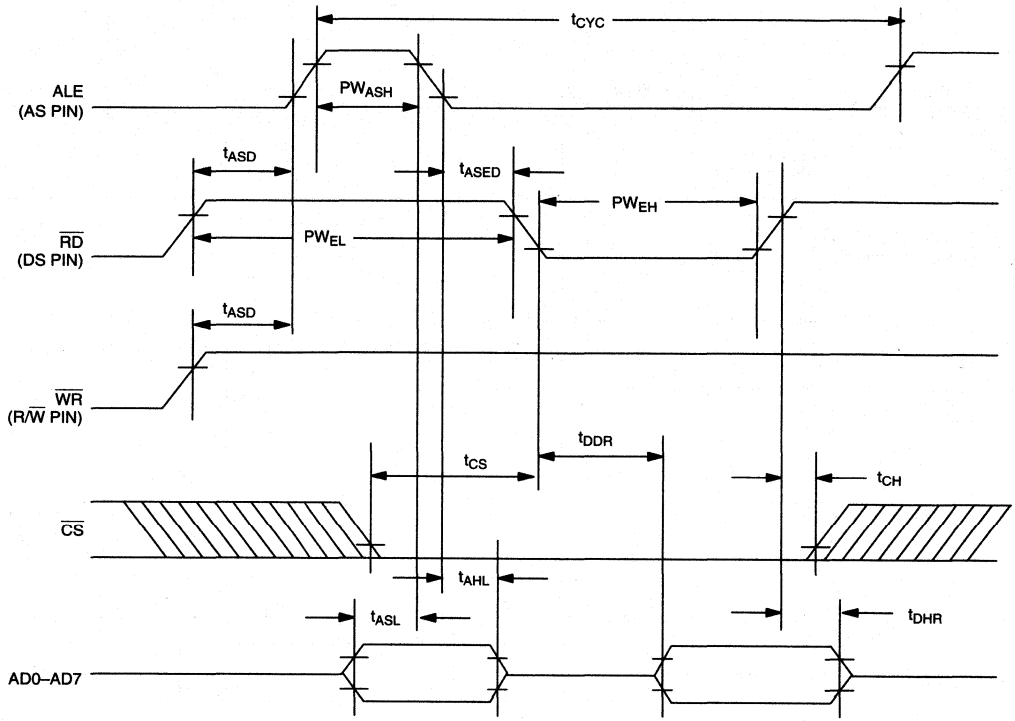
DS12887 BUS TIMING FOR MOTOROLA INTERFACE



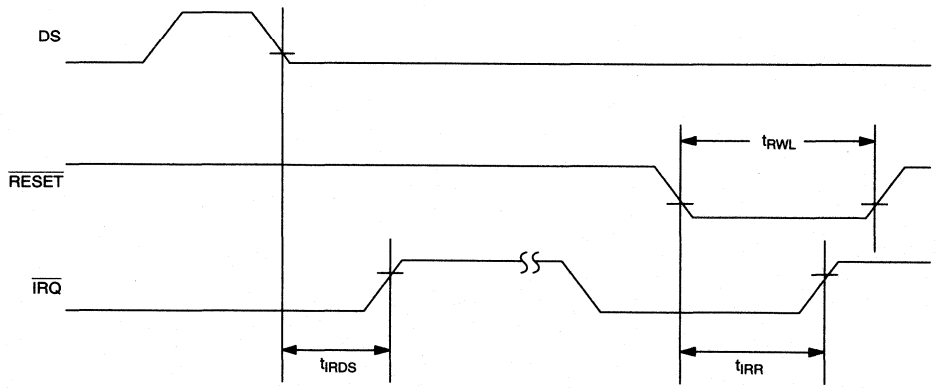
DS12887 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



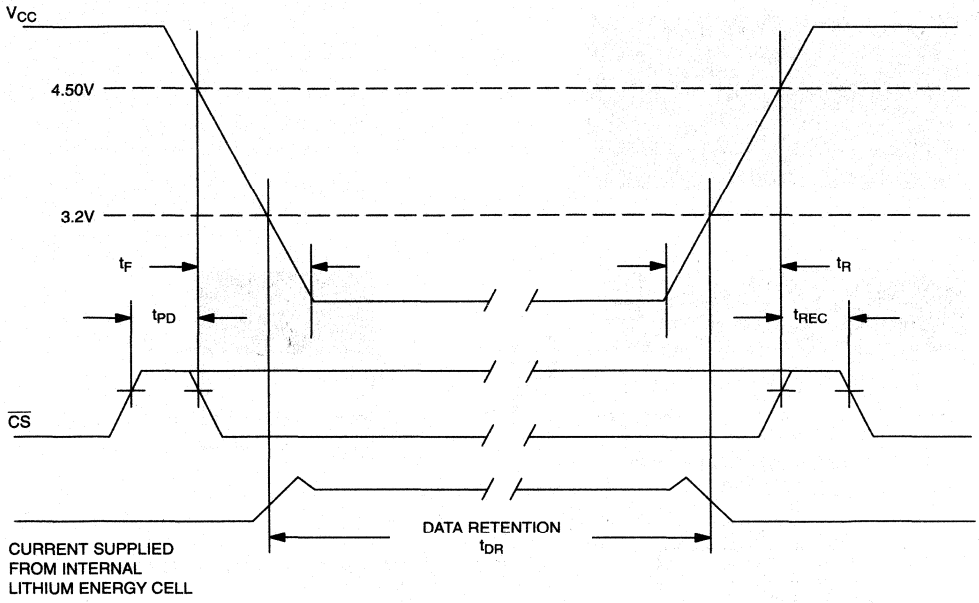
DS12887 BUS TIMING FOR INTEL INTERFACE READ CYCLE



DS12887 IRQ RELEASE DELAY TIMING



POWER DOWN/POWER UP TIMING



POWER DOWN/POWER UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} slew from 4.5V to 0V ($\overline{CS}$ at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to 4.5V ($\overline{CS}$ at V_{IH})	t_R	100			µs	
$\overline{CS}$ at V_{IH} after Power-Up	t_{REC}	20		200	ms	

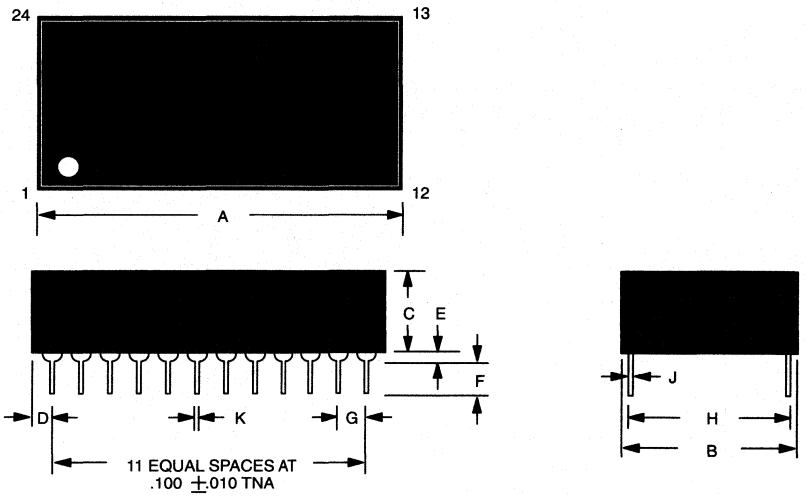
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	

NOTE:
The real time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

DS12887 REAL TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.675 17.15	0.700 17.78
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, 20, 21 AND 22 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

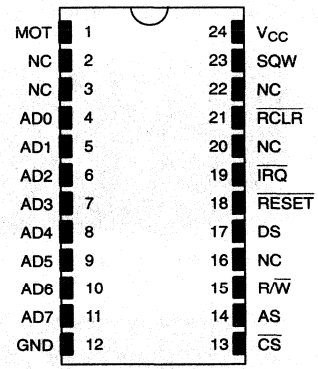
DS12887A
Real Time Clock

3

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818B and DS1287A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End of clock update cycle

PIN ASSIGNMENT



24 PIN ENCAPSULATED PACKAGE

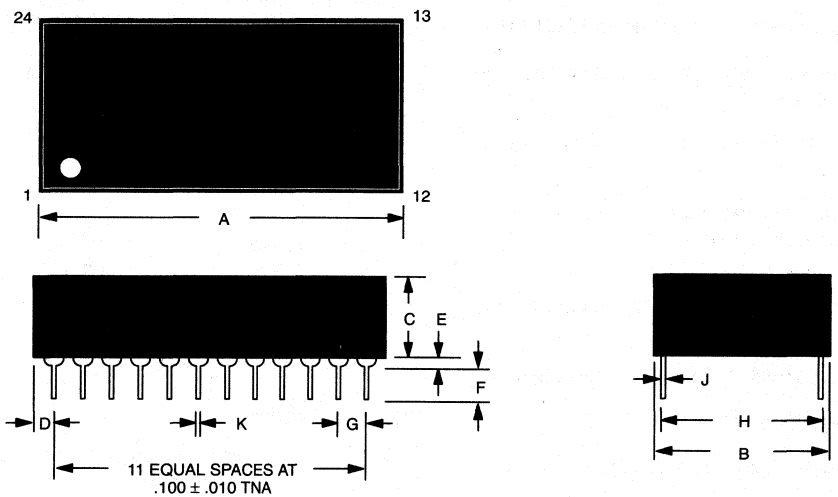
PIN DESCRIPTION

AD0-AD7	-	Multiplexed Address/Data Bus
NC	-	No Connection
MOT	-	Bus Type Selection
$\overline{CS}$	-	Chip Select
AS	-	Address Strobe
R/$\overline{W}$	-	Read/Write Input
DS	-	Data Strobe
$\overline{RESET}$	-	Reset Input
$\overline{IRQ}$	-	Interrupt Request Output
SQW	-	Square Wave Output
V_{CC}	-	+5 Volt Supply
$\overline{RCLR}$	-	RAM Clear
GND	-	Ground

DESCRIPTION

The DS12887A Real Time Clock plus RAM is designed to be a direct replacement for the DS1287A. The DS12887A is identical in form, fit, and function to the DS1287A, and has an additional 64 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 114 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic "0" (-0.3 to 0.8 volts) during battery back-up mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. All other operation, description and specification is identical to the DS12887.

DS12887A REAL TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.675 17.15	0.700 17.78
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, 20 AND 22 ARE MISSING BY DESIGN.

NOTE: THIS DEVICE CANNOT BE STORED OR SHIPPED IN CONDUCTIVE MATERIAL WHICH WILL GIVE A CONTINUITY PATH BETWEEN THE RAM CLEAR PIN AND GROUND.

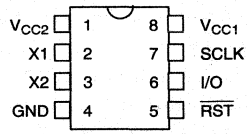
DALLAS SEMICONDUCTOR

DS1302
Trickle Charge Timekeeping Chip

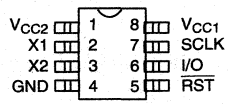
FEATURES

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation
- 31 x 8 RAM for scratchpad data storage
- Serial I/O for minimum pin count
- 2.5-5.5 volt full operation
  - Optional 2.0–5.5 volt full operation also available
- Uses less than 300 nA at 2.5 volts
- Single-byte or multiple-byte (burst mode) data transfer for read or write of clock or RAM data
- 8-pin DIP or optional 8-pin SOIC's for surface mount
- Simple 3-wire interface
- TTL-compatible (V_{CC} = 5V)
- Optional industrial temperature range -40°C to +85°C
- DS1202 compatible
- Added features over DS1202
  - Optional trickle charge capability to V_{CC1}
  - Dual power supply pins for primary and backup power supplies
  - Backup power supply pin can be used for battery or super cap input
  - Additional scratchpad memory (7 bytes)

PIN ASSIGNMENT



DS1302
8–PIN DIP (300 MIL)



DS1302S 8–PIN SOIC (200 MIL)
DS1302Z 8–PIN SOIC (150 MIL)

PIN DESCRIPTION

X1, X2	-	32.768 kHz Crystal Pins
GND	-	Ground
$\overline{RST}$	-	Reset
I/O	-	Data Input/Output
SCLK	-	Serial Clock
V_{CC1}, V_{CC2}	-	Power Supply Pins

ORDERING INFORMATION

PART #	DESCRIPTION
DS1302	Serial Timekeeping Chip; 8–pin DIP
DS1302S	Serial Timekeeping Chip; 8–pin SOIC (200 mil)
DS1302Z	Serial Timekeeping Chip; 8–pin SOIC (150 mil)

DESCRIPTION

The DS1302 Trickle Charge Timekeeping Chip contains a real time clock/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator.

Interfacing the DS1302 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: (1) $\overline{RST}$ (Reset), (2) I/O (Data line), and (3) SCLK (Serial clock). Data can be transferred to and from the clock/RAM one byte at a time or in a burst of up to 31 bytes. The DS1302 is designed to operate on very low power and retain data and clock information on less than 1 microwatt.

101095 1/12

The DS1302 is the successor to the DS1202. In addition to the basic timekeeping functions of the DS1202, the DS1302 has the additional features of dual power pins for primary and backup power supplies, programmable trickle charger for V_{CC1}, and seven additional bytes of scratchpad memory.

OPERATION

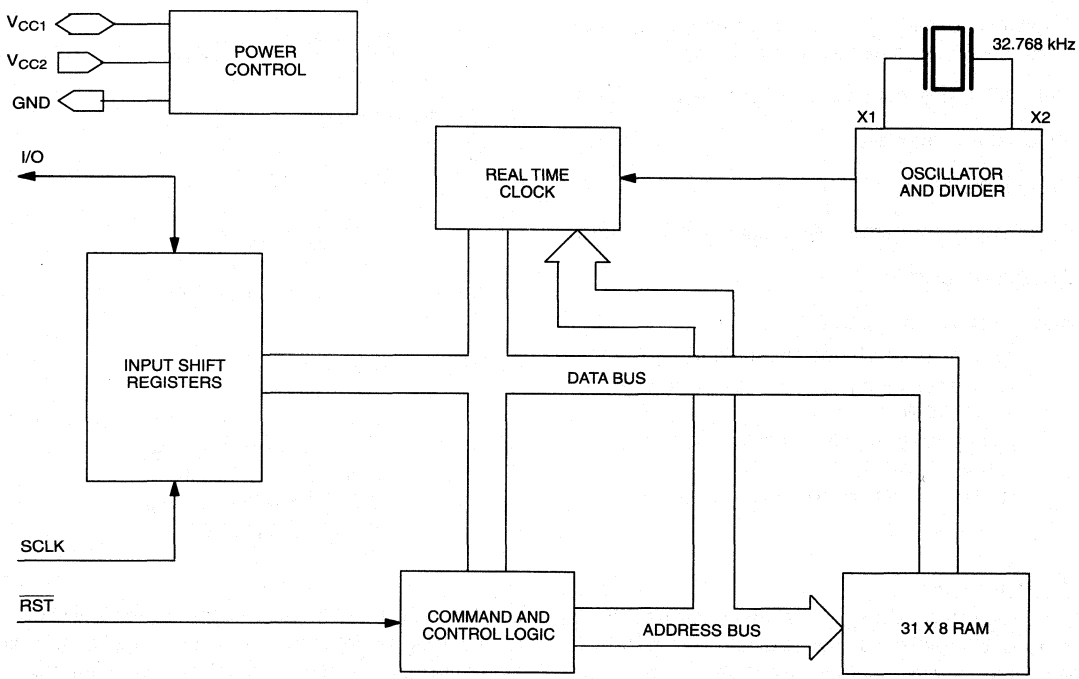
The main elements of the Serial Timekeeper are shown in Figure 1: shift register, control logic, oscillator, real time clock, and RAM. To initiate any transfer of data, $\overline{RST}$ is taken high and eight bits are loaded into the shift register providing both address and command information. Data is serially input on the rising edge of the SCLK. The first eight bits specify which of 40 bytes will be accessed, whether a read or write cycle will take place, and whether a byte or burst mode transfer is to occur.

After the first eight clock cycles have loaded the command word into the shift register, additional clocks will output data for a read or input data for a write. The number of clock pulses equals eight plus eight for byte mode or eight plus up to 248 for burst mode.

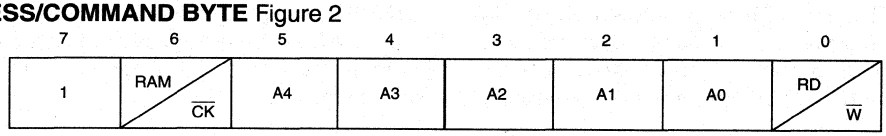
COMMAND BYTE

The command byte is shown in Figure 2. Each data transfer is initiated by a command byte. The MSB (Bit 7) must be a logic 1. If it is zero, writes to the DS1302 will be disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits one through five specify the designated registers to be input or output, and the LSB (Bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

DS1302 BLOCK DIAGRAM Figure 1



ADDRESS/COMMAND BYTE Figure 2



RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves two functions. First, $\overline{RST}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{RST}$ signal provides a method of terminating either single byte or multiple byte data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the $\overline{RST}$ input is low all data transfer terminates and the I/O pin goes to a high impedance state. Data transfer is illustrated in Figure 3. At power–up, $\overline{RST}$ must be a logic 0 until $V_{CC} \geq 2.5$ volts. Also SCLK must be at a logic 0 when $\overline{RST}$ is driven to a logic 1 state.

DATA INPUT

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as $\overline{RST}$ remains high. This operation permits continuous burst mode read capability. Also, the I/O pin is tri–stated upon each rising edge of SCLK. Data is output starting with bit 0.

BURST MODE

Burst mode may be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits one through five = logical one). As before, bit six specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 9 through 31 in the Clock/Calendar Registers or location 31 in the RAM registers. Reads or writes in burst mode start with bit 0 of address 0.

As in the case with the DS1202, when writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred. However, when writing to RAM in burst mode it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written to will be transferred to RAM regardless of whether all 31 bytes are written or not.

CLOCK/CALENDAR

The clock/calendar is contained in seven write/read registers as shown in Figure 4. Data contained in the clock/calendar registers is in binary coded decimal format (BCD).

CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock oscillator is stopped and the DS1302 is placed into a low-power standby mode with a current drain of less than 100 nanoamps. When this bit is written to logic 0, the clock will start.

AM-PM/12-24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10 hour bit (20-23 hours).

WRITE PROTECT REGISTER

Bit 7 of write protect register is the write protect bit. The first seven bits (bits 0–6) are forced to zero and will always read a zero when read. Before any write operation to the clock or RAM, bit 7 must be zero. When high, the write protect bit prevents a write operation to any other register.

TRICKLE CHARGE REGISTER

This register controls the trickle charge characteristics of the DS1302. The simplified schematic of Figure 5 shows the basic components of the trickle charger. The trickle charge select (TCS) bits (bits 4–7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 will enable the trickle charger. All other patterns will disable the trickle charger. The DS1302 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2 – 3) select whether one diode or two diodes are connected between V_{CC2} and V_{CC1}. If DS is 01, one diode is selected or if DS is 10, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independent of

TCS. The RS bits (bits 0–1) select the resistor that is connected between V_{CC2} and V_{CC1}. The resistor selected by the resistor select (RS) bits is as follows:

RS Bits	Resistor	Typical Value
00	None	None
01	R1	2KΩ
10	R2	4KΩ
11	R3	8KΩ

If RS is 00, the trickle charger is disabled independent of TCS.

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to V_{CC2} and a super cap is connected to V_{CC1}. Also assume that the trickle charger has been enabled with 1 diode and resistor R1 between V_{CC2} and V_{CC1}. The maximum current I_{max} would therefore be calculated as follows:

$$I_{max} = (5.0V - \text{diode drop}) / R1$$
$$\sim (5.0V - 0.7V) / 2K\Omega$$
$$\sim 2.2\ mA$$

Obviously, as the super cap charges, the voltage drop between V_{CC2} and V_{CC1} will decrease and therefore the charge current will decrease.

CLOCK/CALENDAR BURST MODE

The clock/calendar command byte specifies burst mode operation. In this mode the first eight clock/calendar registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

If the write protect bit is set high when a write clock/calendar burst mode is specified, no data transfer will occur to any of the eight clock/calendar registers (this includes the control register). The trickle charger is not accessible in burst mode.

RAM

The static RAM is 31 x 8 bytes addressed consecutively in the RAM address space.

RAM BURST MODE

The RAM command byte specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

REGISTER SUMMARY

A register data format summary is shown in Figure 4.

CRYSTAL SELECTION

A 32.768 kHz crystal, Daiwa Part No. DT26S, Seiko Part No. DS-VT-200 or equivalent, can be directly connected to the DS1302 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (CL) of 6 pF.

POWER CONTROL

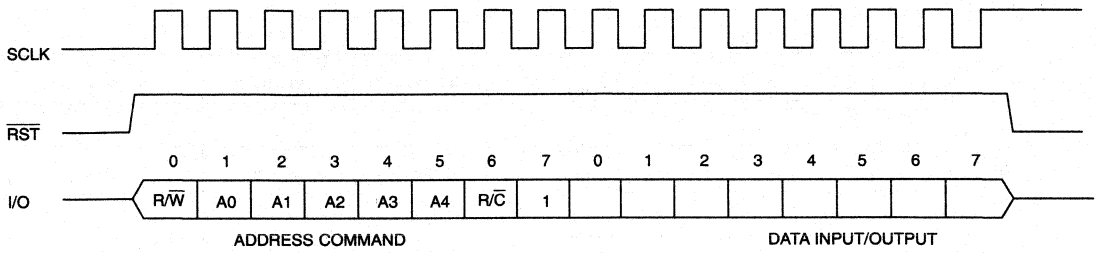
V_{CC1} provides low power operation in single supply and battery operated systems as well as low power battery backup.

V_{CC2} provides the primary power in dual supply systems where V_{CC1} is connected to a backup source to maintain the time and data in the absence of primary power.

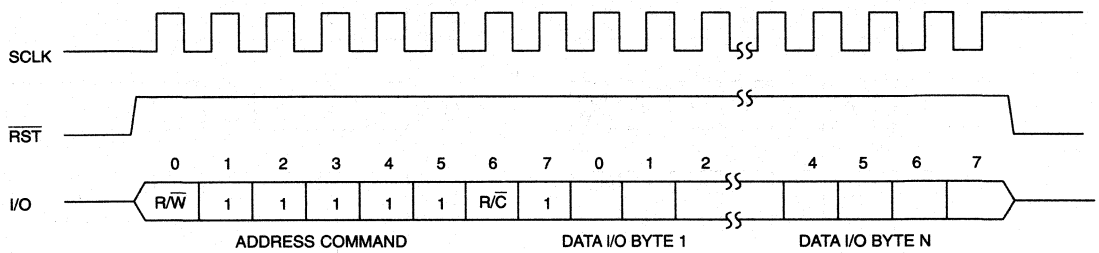
The DS1302 will operate from the larger of V_{CC1} or V_{CC2}. When V_{CC2} is greater than $V_{CC1} + 0.2V$, V_{CC2} will power the DS1302. When V_{CC2} is less than V_{CC1}, V_{CC1} will power the DS1302.

DATA TRANSFER SUMMARY Figure 3

SINGLE BYTE TRANSFER



BURST MODE TRANSFER



FUNCTION	BYTE N	SCLK n
CLOCK	8	72
RAM	31	256

REGISTER ADDRESS/DEFINITION Figure 4

REGISTER ADDRESS

A. CLOCK

	7	6	5	4	3	2	1	0
SEC	1	0	0	0	0	0	0	RD/$\overline{W}$
MIN	1	0	0	0	0	0	1	RD/$\overline{W}$
HR	1	0	0	0	0	1	0	RD/$\overline{W}$
DATE	1	0	0	0	0	1	1	RD/$\overline{W}$
MONTH	1	0	0	0	1	0	0	RD/$\overline{W}$
DAY	1	0	0	0	1	0	1	RD/$\overline{W}$
YEAR	1	0	0	0	1	1	0	RD/$\overline{W}$
CONTROL	1	0	0	0	1	1	1	RD/$\overline{W}$
TRICKLE CHARGER	1	0	0	1	0	0	0	RD/$\overline{W}$
CLOCK BURST	1	0	1	1	1	1	1	RD/$\overline{W}$

B. RAM

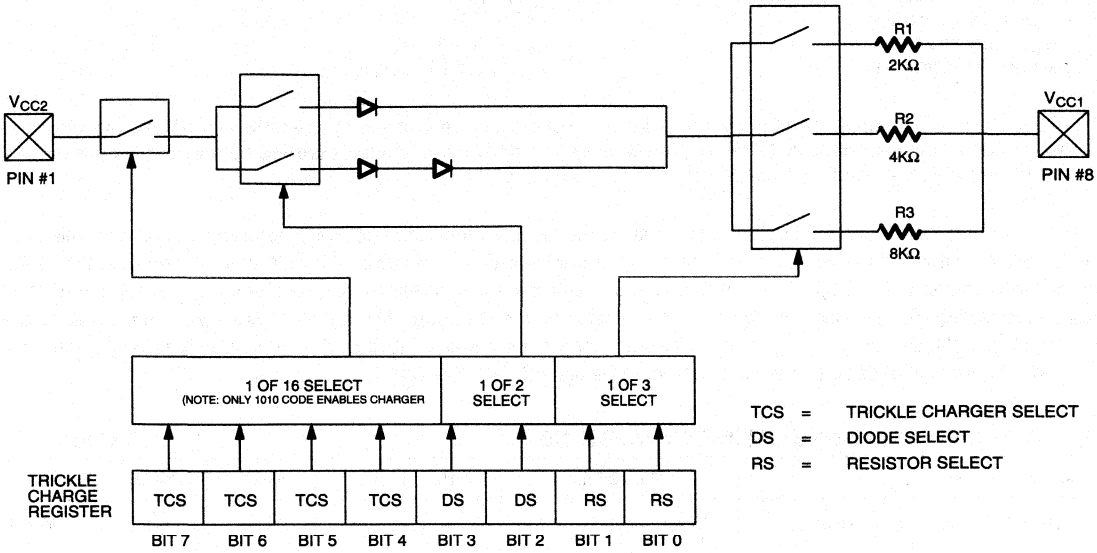
RAM 0	1	1	0	0	0	0	0	RD/$\overline{W}$
RAM 30	1	1	1	1	1	1	0	RD/$\overline{W}$
RAM BURST	1	1	1	1	1	1	1	RD/$\overline{W}$

REGISTER DEFINITION

00–59	CH	10 SEC		SEC				
00–59	0	10 MIN		MIN				
01–12 00–23	12/24	0	10 A/P	HR	HR			
01–28/29 01–30 01–31	0	0	10 DATE		DATE			
01–12	0	0	0	10 M	MONTH			
01–07	0	0	0	0	0	DAY		
0–99	10 YEAR				YEAR			
	WP	0	0	0	0	0	0	0
	TCS	TCS	TCS	TCS	DS	DS	RS	RS

RAM DATA 0								
RAM DATA 30								

DS1302 PROGRAMMABLE TRICKLE CHARGER Figure 5



3

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

The Dallas Semiconductor DS1302 is built to the highest quality standards and manufactured for long term reliability. All Dallas Semiconductor devices are made using the same quality materials and manufacturing methods. However, standard versions of the DS1302 are not exposed to environmental stresses, such as burn–in, that some industrial applications require. Products which have successfully passed through this series of environmental stresses are marked IND or N, denoting their extended operating temperature and reliability rating. For specific reliability information on this product, please contact the factory in Dallas at (214) 450–0448.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Supply Voltage V_{CC1}, V_{CC2}	V_{CC1}, V_{CC2}		2.5		5.5	V	1, 11
Logic 1 Input	V_{IH}		2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	V_{CC}=2.5V	–0.3		+0.3	V	1
		V_{CC}=5V	–0.3		+0.8		

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 2.5 to 5.5V*)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}				+500	µA	6
I/O Leakage	I_{LO}				+500	µA	6
Logic 1 Output	V_{OH}	V_{CC}=2.5V	1.6			V	2
		V_{CC}=5V	2.4				
Logic 0 Output	V_{OL}	V_{CC}=2.5V			0.4	V	3
		V_{CC}=5V			0.4		
Active Supply Current	I_{CC1A}	V_{CC1}=2.5V			0.4	mA	5, 12
		V_{CC1}=5V			1.2		
Timekeeping Current	I_{CC1T}	V_{CC1}=2.5V			0.3	µA	4,12
		V_{CC1}=5V			1		
Standby Current	I_{CC1S}	V_{CC1}=2.5V		100		nA	10, 12, 14
		V_{CC1}=5V		100			
Active Supply Current	I_{CC2A}	V_{CC2}=2.5V			0.425	mA	5, 13
		V_{CC2}=5V			1.28		

*Unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS (cont'd)

(0°C to 70°C; V_{CC} = 2.5 to 5.5V*)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Timekeeping Current	I_{CC2T}	V_{CC2}=2.5V			25.3	µA	4,13
		V_{CC2}=5V			81		
Standby Current	I_{CC2S}	V_{CC2}=2.5V			25	µA	10, 13
		V_{CC2}=5V			80		
Trickle Charge Resistors	R1 R2 R3			2 4 8		KΩ KΩ KΩ	
Trickle Charger Diode Voltage Drop	V_{TD}			0.7		V	

*Unless otherwise noted.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		10		pF	
I/O Capacitance	$C_{I/O}$		15		pF	
Crystal Capacitance	C_X		6		pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = +5V ± 10%*)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	V_{CC}=2.5V	200			ns	7
		V_{CC}=5V	50				
CLK to Data Hold	t_{CDH}	V_{CC}=2.5V	280			ns	7
		V_{CC}=5V	70				
CLK to Data Delay	t_{CDD}	V_{CC}=2.5V			800	ns	7, 8, 9
		V_{CC}=5V			200		
CLK Low Time	t_{CL}	V_{CC}=2.5V	1000			ns	7
		V_{CC}=5V	250				
CLK High Time	t_{CH}	V_{CC}=2.5V	1000			ns	7
		V_{CC}=5V	250				
CLK Frequency	t_{CLK}	V_{CC}=2.5V			0.5	MHz	7
		V_{CC}=5V	DC		2.0		
CLK Rise and Fall	t_R, t_F	V_{CC}=2.5V			2000	ns	
		V_{CC}=5V			500		
RST to CLK Setup	t_{CC}	V_{CC}=2.5V	4			µs	7
		V_{CC}=5V	1				

*Unless otherwise noted.

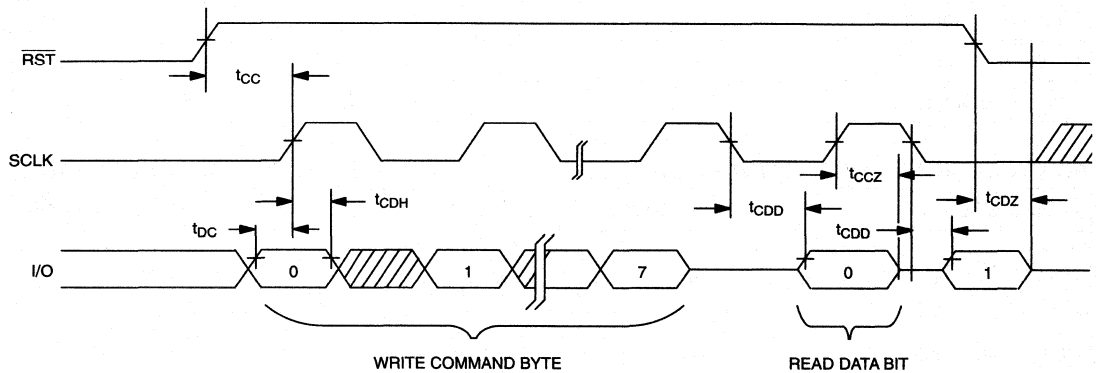
AC ELECTRICAL CHARACTERISTICS (cont'd)

(0°C to 70°C; V_{CC} = +5V ± 10%*)

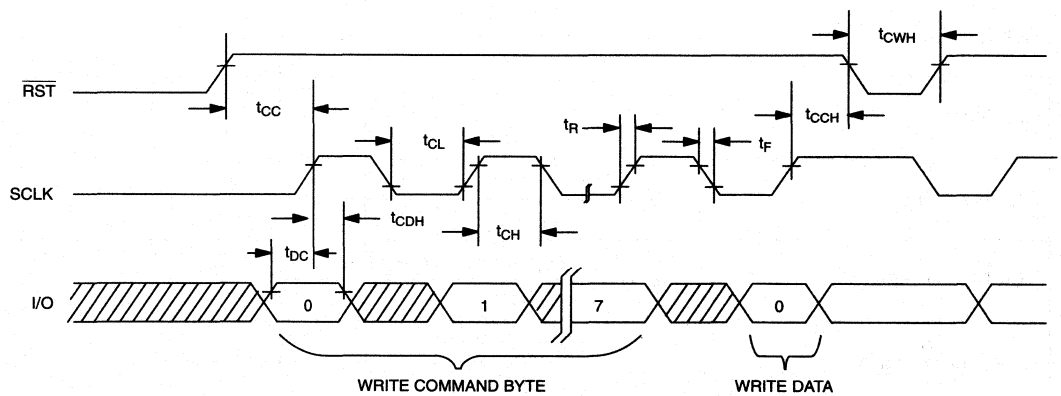
PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
CLK to RST Hold	t_{CCH}	V_{CC}=2.5V	240			ns	7
		V_{CC}=5V	60				
RST Inactive Time	t_{CWH}	V_{CC}=2.5V	4			µs	7
		V_{CC}=5V	1				
RST to I/O High Z	t_{CDZ}	V_{CC}=2.5V			280	ns	7
		V_{CC}=5V			70		
SCLK to I/O High Z	t_{CCZ}	V_{CC}=2.5V			280	ns	7
		V_{CC}=5V			70		

*Unless otherwise noted.

TIMING DIAGRAM: READ DATA TRANSFER Figure 5



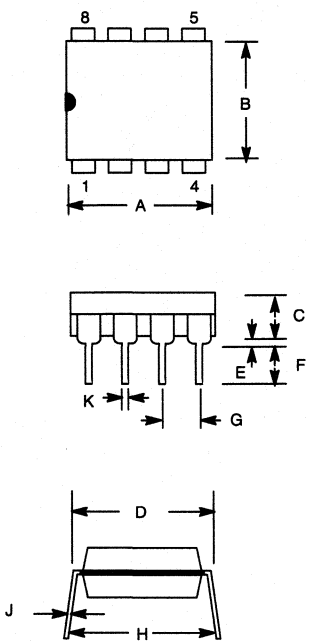
TIMING DIAGRAM: WRITE DATA TRANSFER Figure 6



NOTES:

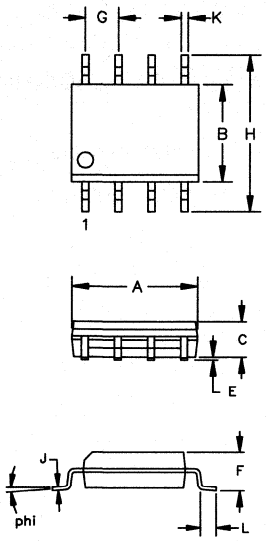
1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 mA at V_{CC}=5V and .4 mA at V_{CC}=2.5V, V_{OH}=V_{CC} for capacitive loads.
3. Logic zero voltages are specified at a sink current of 4 mA at V_{CC}=5V and 1.5 mA at V_{CC}=2.5V, V_{OL}=GND for capacitive loads.
4. I_{CC1T} and I_{CC2T} are specified with I/O open, $\overline{RST}$ set to a logic 0, and clock halt flag=0 (oscillator enabled).
5. I_{CC1A} and I_{CC2A} are specified with the I/O pin open, $\overline{RST}$ high, SCLK=2 MHz at V_{CC}=5V; SCLK=500 kHz, V_{CC}=2.5V and clock halt flag=0 (oscillator enabled).
6. $\overline{RST}$, SCLK, and I/O all have 40KΩ pulldown resistors to ground.
7. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10 ms maximum rise and fall time.
8. Measured at V_{OH}=2.4V or V_{OL}=0.4V.
9. Load capacitance = 50 pF.
10. I_{CC1S} and I_{CC2S} are specified with $\overline{RST}$, I/O, and SCLK open. The clock halt flag must be set to logic one (oscillator disabled).
11. V_{CC}=V_{CC2}, when V_{CC2}>V_{CC1}+0.2V; V_{CC}=V_{CC1}, when V_{CC1}>V_{CC2}.
12. V_{CC2}=0 volts.
13. V_{CC1}=0 volts.
14. Typical values are at 25°C.

DS1302 SERIAL TIMEKEEPER 8–PIN DIP



PKG	8-PIN	
DIM	MIN	MAX
A IN.	0.360	0.400
MM	9.14	10.16
B IN.	0.240	0.260
MM	6.10	6.60
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.300	0.325
MM	7.62	8.26
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.140
MM	3.04	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.320	0.370
MM	8.13	9.40
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1302S SERIAL TIMEKEEPER 8–PIN SOIC (150 MIL AND 200 MIL)



PKG	8-PIN (150 MIL)		8-PIN (200 MIL)	
DIM	MIN	MAX	MIN	MAX
A IN. MM	0.188 4.78	0.196 4.98	0.203 5.16	0.213 5.41
B IN. MM	0.150 3.81	0.158 4.01	0.203 5.16	0.213 5.41
C IN. MM	0.048 1.22	0.062 1.57	0.070 1.78	0.074 1.88
E IN. MM	0.004 0.10	0.010 0.25	0.004 0.10	0.010 0.25
F IN. MM	0.053 1.35	0.069 1.75	0.074 1.88	0.084 2.13
G IN. MM	0.050 BSC 1.27 BSC			
H IN. MM	0.230 5.84	0.244 6.20	0.302 7.67	0.318 8.08
J IN. MM	0.007 0.18	0.011 0.28	0.006 0.15	0.010 0.25
K IN. MM	0.012 0.30	0.020 0.51	0.013 0.33	0.020 0.51
L IN. MM	0.016 0.41	0.050 1.27	0.019 0.48	0.030 0.76
phi	0°	8°	0°	8°

56–G2008–001
56–G4010–001

DALLAS SEMICONDUCTOR

DS1305
Serial Alarm Real Time Clock (RTC)

FEATURES

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation
- 96 byte nonvolatile RAM for data storage
- Two Time of Day Alarms – programmable on combination of seconds, minutes, hours, and day of the week
- Serial interface supports Motorola Serial Peripheral Interface (SPI) serial data ports or standard 3– wire interface
- Burst Mode for reading/writing successive addresses in clock/RAM
- Dual power supply pins for primary and backup power supplies
- Optional trickle charge output to backup supply
- 2.5 – 5.5 volt operation
- Optional 2.0–5.5 volt full operation also available
- Optional industrial temperature range –40°C to +85°C
- Available in space–efficient 20–pin TSSOP package

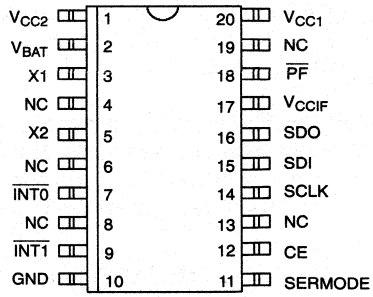
ORDERING INFORMATION

DS1305	16–Pin DIP
DS1305N	16–Pin DIP (Industrial)
DS1305E	20–Pin TSSOP
DS1305EN	20–Pin TSSOP (Industrial)

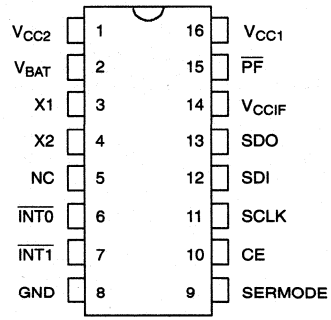
DESCRIPTION

The DS1305 Serial Alarm Real Time Clock provides a full BCD clock calendar which is accessed via a simple serial interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24–hour or 12–hour format with AM/PM indicator. In addition 96 bytes of nonvolatile RAM are provided for data storage.

PIN ASSIGNMENT



DS1305 20-PIN TSSOP (173 mil)



DS1305 16–PIN DIP (300 mil)

PIN DESCRIPTION

V_{CC1}	–	Primary Power Supply
V_{CC2}	–	Backup Power Supply
V_{BAT}	–	+3 Volt Battery Input
V_{CCIF}	–	Interface Logic Power Supply Input
GND	–	Ground
X1, X2	–	32,768 Hz Crystal Connection
$\overline{INT0}$	–	Interrupt 0 Output
$\overline{INT1}$	–	Interrupt 1 Output
SDI	–	Serial Data In
SDO	–	Serial Data Out
CE	–	Chip Enable
SCLK	–	Serial Clock
SERMODE	–	Serial Interface Mode
$\overline{PF}$	–	Power Fail Output

An interface logic power supply input pin (V_{CCIF}) allows the DS1305 to drive SDO and $\overline{PF}$ pins to a level that is compatible with the interface logic. This allows an easy interface to 3 volt logic in mixed supply systems.

The DS1305 offers dual power supplies as well as a battery input pin. The dual power supplies support a programmable trickle charge circuit which allows a rechargeable energy source (such as a super cap or rechargeable battery) to be used for a backup supply. The V_{BAT} pin allows the device to be backed up by a non–rechargeable battery. The DS1305 is fully operational from 2.5 to 5.5 volts.

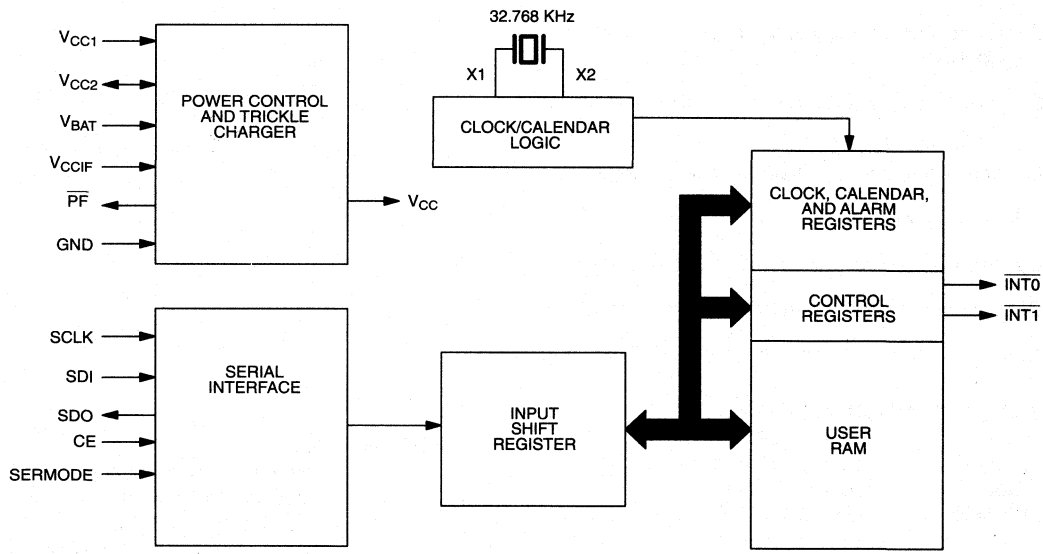
Two programmable time of day alarms are provided by the DS1305. Each alarm can generate an interrupt on a programmable combination of seconds, minutes, hours, and day. "Don't care" states can be inserted into one or more fields if it is desired for them to be ignored for the alarm condition. The time of day alarms can be programmed to assert two different interrupt outputs or to assert one common interrupt output. Both interrupt outputs operate when the device is powered by V_{CC1}, V_{CC2}, or V_{BAT}.

The DS1305 supports a direct interface to Motorola SPI serial data ports or standard 3–wire interface. An easy–to–use address and data format is implemented in which data transfers can occur one byte at a time or in multiple byte burst mode.

OPERATION

The block diagram in Figure 1 shows the main elements of the Serial Alarm RTC. The following paragraphs describe the function of each pin.

DS1305 BLOCK DIAGRAM Figure 1



SIGNAL DESCRIPTIONS

V_{CC1} – DC power is provided to the device on this pin. V_{CC1} is the primary power supply.

V_{CC2} – This is the secondary power supply pin. In systems using the trickle charger, the rechargeable energy source is connected to this pin.

V_{BAT} – Battery input for any standard 3 volt lithium cell or other energy source.

V_{CCIF} (Interface Logic Power Supply Input) – The V_{CCIF} pin allows the DS1305 to drive SDO and $\overline{PF}$ output pins to a level that is compatible with the interface logic, thus allowing an easy interface to 3 volt logic in mixed supply systems. This pin is physically connected to the source connection of the p–channel transistors in the output buffers of the SDO and $\overline{PF}$ pins.

SERMODE (Serial Interface Mode Input) – The SERMODE pin offers the flexibility to choose between two serial interface modes. When connected to GND, standard 3–wire communication is selected. When connected to V_{CC}, Motorola SPI communication is selected.

SCLK (Serial Clock Input) – SCLK is used to synchronize data movement on the serial interface for either the SPI or 3–wire interface.

SDI (Serial Data Input) – When SPI communication is selected, the SDI pin is the serial data input for the SPI bus. When 3–wire communication is selected, this pin must be tied to the SDO pin (the SDI and SDO pins function as a single I/O pin when tied together).

SDO (Serial Data Output) – When SPI communication is selected, the SDO pin is the serial data output for the SPI bus. When 3–wire communication is selected, this pin must be tied to the SDI pin (the SDI and SDO pins function as a single I/O pin when tied together).

CE (Chip Enable) – The Chip Enable signal must be asserted high during a read or a write for both 3–wire and SPI communication. This pin has an internal 55K pull–down resistor (typical).

$\overline{INT0}$ (Interrupt 0 Output) – The $\overline{INT0}$ pin is an active low output of the DS1305 that can be used as an interrupt input to a processor. The $\overline{INT0}$ pin can be programmed to be asserted by only Alarm 0 or can be programmed to be asserted by either Alarm 0 or Alarm 1. The $\overline{INT0}$ pin remains low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is set. The $\overline{INT0}$ pin operates when the DS1305 is powered by V_{CC1}, V_{CC2}, or V_{BAT}. The $\overline{INT0}$ pin is an open drain output and requires an external pull–up resistor.

$\overline{INT1}$ (Interrupt 1 Output) – The $\overline{INT1}$ pin is an active low output of the DS1305 that can be used as an interrupt input to a processor. The $\overline{INT1}$ pin can be programmed to be asserted by alarm 1 only. The $\overline{INT1}$ pin remains low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is set. The $\overline{INT1}$ pin operates when the DS1305 is powered by V_{CC1}, V_{CC2}, or V_{BAT}. The $\overline{INT1}$ pin is an open drain output and requires an external pull–up resistor

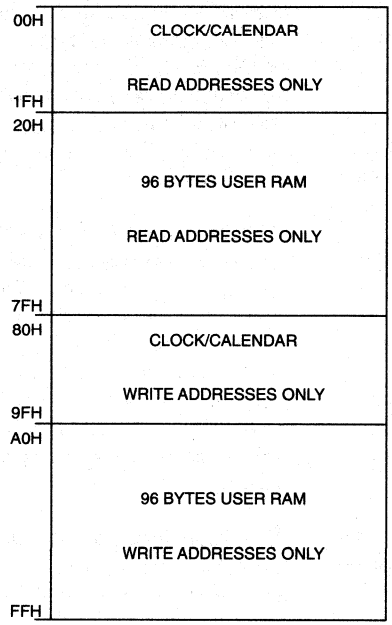
$\overline{PF}$ (Power Fail Output) – The $\overline{PF}$ pin is used to indicate loss of the primary power supply (V_{CC1}). When V_{CC1} is less than V_{CC2} or is less than V_{BAT}, the $\overline{PF}$ pin will be driven low.

X1, X2 – Connections for a standard 32.768 KHz quartz crystal, Daiwa part number DS–26S, Seiko part number DS–VT–200, or equivalent. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6 pF. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks". The DS1305 can also be driven by an external 32.768 KHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

RTC AND RAM ADDRESS MAP

The address map for the RTC and RAM registers of the DS1305 is shown in Figure 2. Data is written to the RTC by writing to address locations 80h to 9Fh and is written to the RAM by writing to address locations A0h to FFh. RTC data is read by reading address locations 00h to 1Fh and RAM data is read by reading address locations 20h to 7Fh.

ADDRESS MAP Figure 2



CLOCK, CALENDAR, AND ALARM

The time and calendar information is obtained by reading the appropriate register bytes. The real time clock registers are illustrated in Figure 3. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. Note that some bits are set to zero. These bits will always read 0 regardless of how they are written. Also note that registers 12h to 1Fh (read) and registers 92h to 9Fh are reserved. These registers will always read 0 regardless of how they are written. The contents of the time, calendar, and alarm registers are in the Binary–Coded Decimal (BCD) format.

RTC REGISTERS Figure 3

HEX ADDRESS READ	HEX ADDRESS WRITE	BIT7						BIT 0		
00H	80H	0	10 SEC						SEC	
01H	81H	0	10 MIN						MIN	
02H	82H	0	12/24	10 A/P	10 HR				HOURS	
03H	83H	0	0	0	0				DAY	
04H	84H	0	0	10 DATE					DATE	
05H	85H	0	0	10 MONTH					MONTH	
06H	86H	10 YEAR							YEAR	
07H	87H	M	10 SEC ALARM						SEC ALARM	ALARM 0
08H	88H	M	10 MIN ALARM						MIN ALARM	
09H	89H	M	12/24	10 A/P	10 HA				HOUR ALARM	
0AH	8AH	M	0	0	0				DAY ALARM	
0BH	8BH	M	10 SEC ALARM						SEC ALARM	ALARM 1
0CH	8CH	M	10 MIN ALARM						MIN ALARM	
0DH	8DH	M	12/24	10 A/P	10 HA				HOUR ALARM	
0EH	8EH	M	0	0	0				DAY ALRM	
0FH	8FH	CONTROL REGISTER								
10H	90H	STATUS REGISTER								
11H	91H	TRICKLE CHARGER REGISTER								
12H–1FH	92H–9FH	RESERVED								

The DS1305 can be run in either 12–hour or 24–hour mode. Bit 6 of the hours register is defined as the 12– or 24–hour mode select bit. When high, the 12–hour mode is selected. In the 12–hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24–hour mode, bit 5 is the second 10 hour bit (20–23 hours).

The DS1305 contains two time of day alarms. Time of Day Alarm 0 can be set by writing to registers 87h to 8Ah. Time of Day Alarm 1 can be set by writing to registers 8Bh to 8Eh. The alarms can be programmed (by the INTCN bit of the Control Register) to operate in two different modes – each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time of day alarm registers are mask bits (Table 1). When all of the mask bits are logic 0, a time of day alarm will only occur once per week when the values stored in timekeeping registers 00h to 03h match the values stored in the time of day alarm registers. An alarm will be generated every day when bit 7 of the day alarm register is set to a logic 1. An alarm will be generated every hour when bit 7 of the day and hour alarm registers is set to a logic 1. Similarly, an alarm will be generated every minute when bit 7 of the day, hour, and minute alarm registers is set to a logic 1. When bit 7 of the day, hour, minute, and seconds alarm registers is set to a logic 1, alarm will occur every second.

TIME OF DAY ALARM MASK BITS Table 1

ALARM REGISTER MASK BITS (BIT 7)				
SECONDS	**MINUTES**	**HOURS**	**DAYS**	
1	1	1	1	Alarm once per second
0	1	1	1	Alarm when seconds match
0	0	1	1	Alarm when minutes and seconds match
0	0	0	1	Alarm when hours, minutes, and seconds match
0	0	0	0	Alarm when day, hours, minutes, and seconds match

SPECIAL PURPOSE REGISTERS

The DS1305 has three additional registers (Control Register, Status Register, and Trickle Charger Register) that control the real time clock, interrupts, and trickle charger.

CONTROL REGISTER (READ 0FH, WRITE 8FH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
$\overline{EOSC}$	WP	0	0	0	INTCN	AIE1	AIE0

$\overline{EOSC}$ (Enable oscillator) – This bit when set to logic 0 will start the oscillator. When this bit is set to a logic 1, the oscillator is stopped and the DS1305 is placed into a low–power standby mode with a current drain of less than 100 nanoamps when power is supplied by V_{BAT} or V_{CC2}.

WP (Write Protect) – Before any write operation to the clock or RAM, this bit must be logic 0. When high, the write protect bit prevents a write operation to any other register and the WP bit is the only bit in the control register that can be written.

INTCN (Interrupt Control) – This bit controls the relationship between the two time of day alarms and the interrupt output pins. When the INTCN bit is set to a logic 1, a match between the timekeeping registers and the Alarm 0 registers will activate the $\overline{INT0}$ pin (provided that the alarm is enabled) and a match between the timekeeping registers and the Alarm 1 registers will activate the $\overline{INT1}$ pin (provided that the alarm is enabled). When the INTCN bit is set to a logic 0, a match between the timekeeping registers and either Alarm 0 or Alarm 1 will activate the $\overline{INT0}$ pin (provided that the alarms are enabled). $\overline{INT1}$ has no function when INTCN is set to a logic 0.

AIE0 (Alarm Interrupt Enable 0) – When set to a logic 1, this bit permits the Interrupt 0 Request Flag (IRQF0) bit in the status register to assert $\overline{INT0}$. When the AIE0 bit is set to logic 0, the IRQF0 bit does not initiate the $\overline{INT0}$ signal.

AIE1 (Alarm Interrupt Enable 1) – When set to a logic 1, this bit permits the Interrupt 1 Request Flag (IRQF1) bit in the status register to assert $\overline{INT1}$ (when INTCN=1) or to assert $\overline{INT0}$ (when INTCN=0). When the AIE1 bit is set to logic 0, the IRQF1 bit does not initiate an interrupt signal.

STATUS REGISTER (READ 10H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	0	0	0	0	0	IRQF1	IRQF0

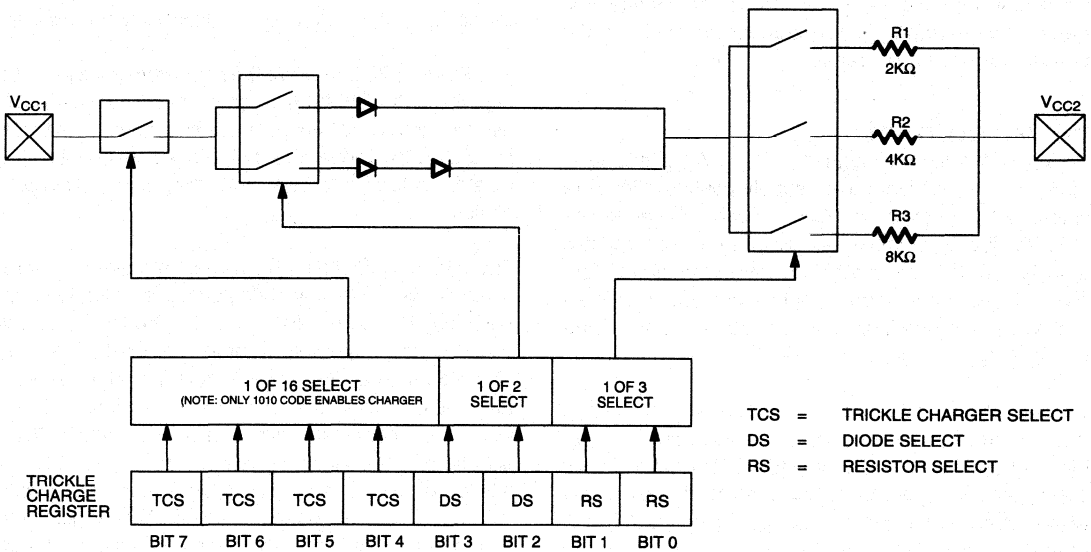
IRQF0 (Interrupt 0 Request Flag) – A logic 1 in the Interrupt Request Flag bit indicates that the current time has matched the Alarm 0 registers. If the AIE0 bit is also a logic 1, the $\overline{INT0}$ pin will go low. IRQF0 is cleared when any of the Alarm 0 registers are read or written.

IRQF1 (Interrupt 1 Request Flag) – A logic 1 in the Interrupt Request Flag bit indicates that the current time has matched the Alarm 1 registers. This flag can be used to generate an interrupt on either $\overline{INT0}$ or $\overline{INT1}$ depending on the status of the INTCN bit in the Control Register. If the INTCN bit is set to a logic 1 and IRQF1 is at a logic 1 (and AIE1 bit is also a logic 1), the $\overline{INT1}$ pin will go low. If the INTCN bit is set to a logic 0 and IRQF1 is at a logic 1 (and AIE0 bit is also a logic 1), the $\overline{INT0}$ pin will go low. IRQF1 is cleared when any of the Alarm 1 registers are read or written.

TRICKLE CHARGE REGISTER (READ 11H, WRITE 91H)

This register controls the trickle charge characteristics of the DS1305. The simplified schematic of Figure 4 shows the basic components of the trickle charger. The trickle charge select (TCS) bits (bits 4–7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 will enable the trickle charger. All other patterns will disable the trickle charger. The DS1305 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2–3) select whether one diode or two diodes are connected between V_{CC1} and V_{CC2}. If DS is 01, one diode is selected. If DS is 10, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independent of TCS. The RS bits select the resistor that is connected between V_{CC1} and V_{CC2}. The resistor is selected by the resister select (RS) bits as shown in Table 2.

PROGRAMMABLE TRICKLE CHARGER Figure 4



TRICKLE CHARGER RESISTOR SELECT

Table 2

RS BITS	RESISTOR	TYPICAL VALUE
00	None	None
01	R1	2KΩ
10	R2	4KΩ
11	R3	8KΩ

If RS is 00, the trickle charger is disabled independent of TCS.

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5 volts is applied to V_{CC1} and a super cap is connected to V_{CC2}. Also assume that the trickle charger has been enabled with 1 diode and resister R1 between V_{CC1} and V_{CC2}. The maximum current I_{MAX} would therefore be calculated as follows:

$$I_{MAX} = (5.0V - \text{diode drop})/R1$$
$$\sim (5.0V - 0.7V)/2K\Omega$$
$$\sim 2.2mA$$

Obviously, as the super cap charges, the voltage drop between V_{CC1} and V_{CC2} will decrease and therefore the charge current will decrease.

POWER CONTROL

Power is provided through the V_{CC1}, V_{CC2}, and V_{BAT} pins. Three different power supply configurations are illustrated in Figure 5. Configuration 1 shows the DS1305 being backed up by a non–rechargeable energy source such as a lithium battery. In this configuration, the system power supply is connected to V_{CC1} and V_{CC2} is grounded. The DS1305 will be write protected if V_{CC1} is less than V_{BAT}.

Configuration 2 illustrates the DS1305 being backed up by a rechargeable energy source. In this case, the V_{BAT} pin is grounded, V_{CC1} is connected to the primary power supply, and V_{CC2} is connected to the secondary supply (the rechargeable energy source). The DS1305 will operate from the larger of V_{CC1} or V_{CC2}. When V_{CC1} is greater than V_{CC2} + 0.2V (typical), V_{CC1} will power the DS1305. When V_{CC1} is less than V_{CC2}, V_{CC2} will power the DS1305. The DS1305 does not write protect itself in this configuration.

Configuration 3 shows the DS1305 in battery operate mode where the device is powered only by a single battery. In this case, the V_{CC1} and V_{BAT} pins are grounded and the battery is connected to the V_{CC2} pin.

SERIAL INTERFACE

The DS1305 offers the flexibility to choose between two serial interface modes. The DS1305 can communicate with the SPI interface or with a standard 3–wire interface. The interface method used is determined by the SERMODE pin. When this pin is connected to V_{CC}, SPI communication is selected. When this pin is connected to ground, standard 3–wire communication is selected.

SERIAL PERIPHERAL INTERFACE (SPI)

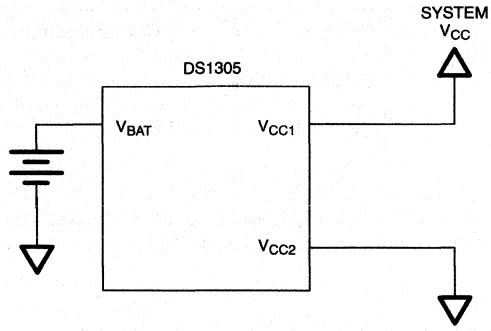
The serial peripheral interface (SPI) is a synchronous bus for address and data transfer and is used when interfacing with the SPI bus on specific Motorola microcontrollers such as the 68HC05C4 and the 68HC11A8. The SPI mode of serial communication is selected by tying the SERMODE pin to V_{CC}. Four pins are used for the SPI. The four pins are the SDO (Serial Data Out), SDI (Serial Data In), CE (Chip Enable), and SCLK (Serial Clock). The DS1305 is the slave device in an SPI application, with the microcontroller being the master.

The SDI and SDO pins are the serial data input and output pins for the DS1305, respectively. The CE input is used to initiate and terminate a data transfer. The SCLK pin is used to synchronize data movement between the master (microcontroller) and the slave (DS1305) devices.

The shift clock (SCLK), which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. The inactive clock polarity is programmable in some microcontrollers. The DS1305 offers an important feature in that the level of the inactive clock is determined by sampling SCLK when CE becomes active. Therefore either SCLK polarity can be accommodated. Input data (SDI) is latched on the internal strobe edge and output data (SDO) is shifted out on the shift edge (see Table 3 and Figure 6). There is one clock for each bit transferred. Address and data bits are transferred in groups of eight.

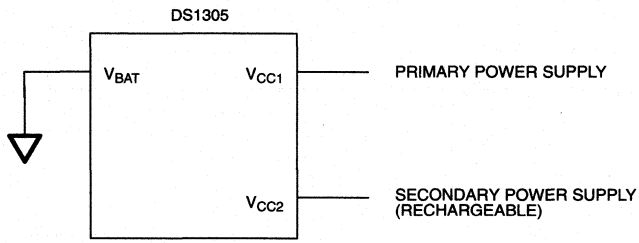
POWER SUPPLY CONFIGURATIONS FOR THE DS1305 Figure 5

Configuration 1: Backup Supply is a Non–Rechargeable Lithium Battery



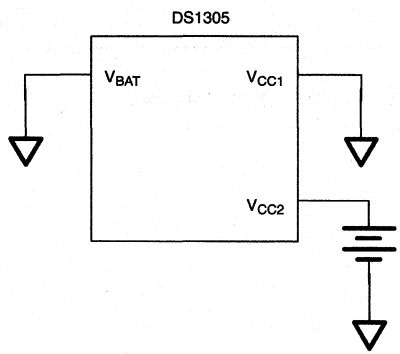
Note: Device is write protected if $V_{CC} < V_{BAT}$.

Configuration 2: Backup Supply is a Rechargeable Battery or Super Capacitor



Note: Device does not provide automatic write protection.

Configuration 3: Battery Operate Mode

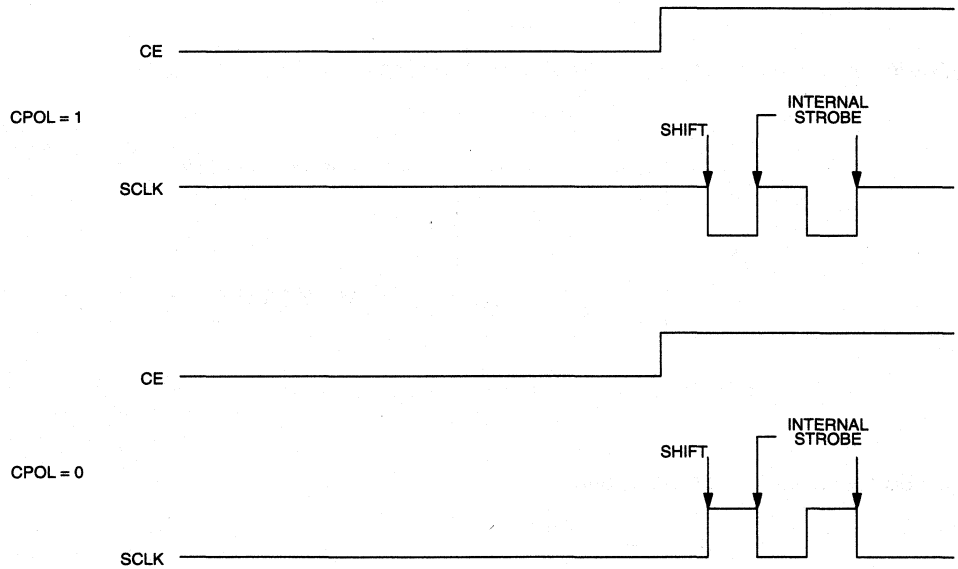


FUNCTION TABLE Table 3

MODE	CE	SCLK	SDI	SDO
Disable Reset	L	Input Disabled	Input Disabled	High Z
Write	H	CPOL=1* ↑ CPOL=0 ↓	Data Bit Latch	High Z
Read	H	CPOL=1 ↓ CPOL=0 ↑	X	Next data bit shift**

* CPOL is the "Clock Polarity" bit that is set in the control register of the microcontroller.
** SDO remains at High Z until eight bits of data are ready to be shifted out during a read.

SERIAL CLOCK AS A FUNCTION OF MICROCONTROLLER CLOCK POLARITY (CPOL) Figure 6

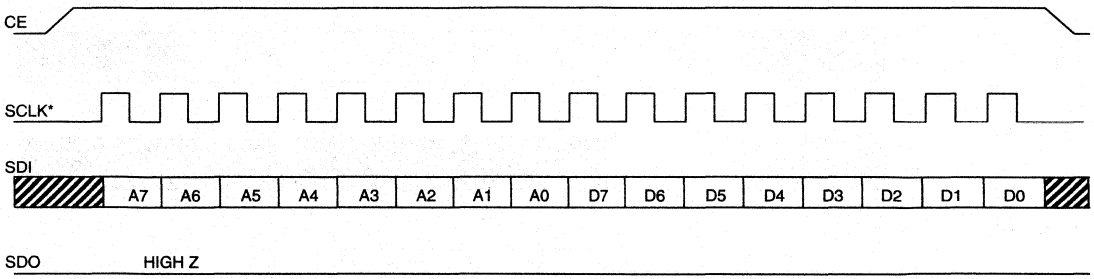


NOTE: CPOL is a bit that is set in the microcontroller's Control Register.

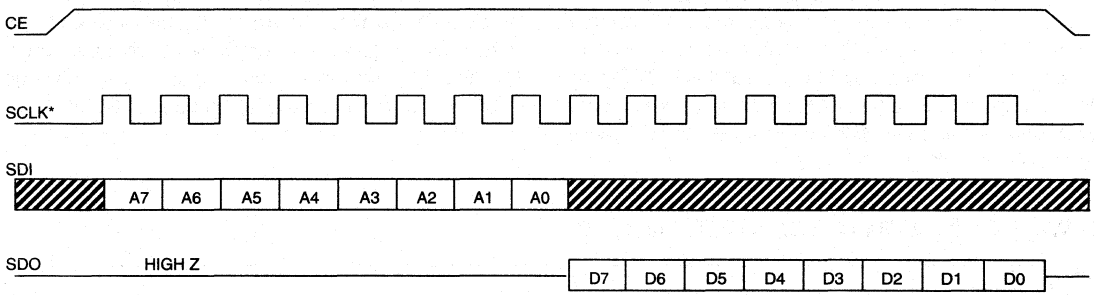
ADDRESS AND DATA BYTES

Address and data bytes are shifted MSB first into the serial data input (SDI) and out of the serial data output (SDO). Any transfer requires the address of the byte to specify a write or read to either a RTC or RAM location, followed by one or more bytes of data. Data is transferred out of the SDO for a read operation and into the SDI for a write operation (see Figure 7 and 8).

SPI SINGLE BYTE WRITE Figure 7



SPI SINGLE BYTE READ Figure 8

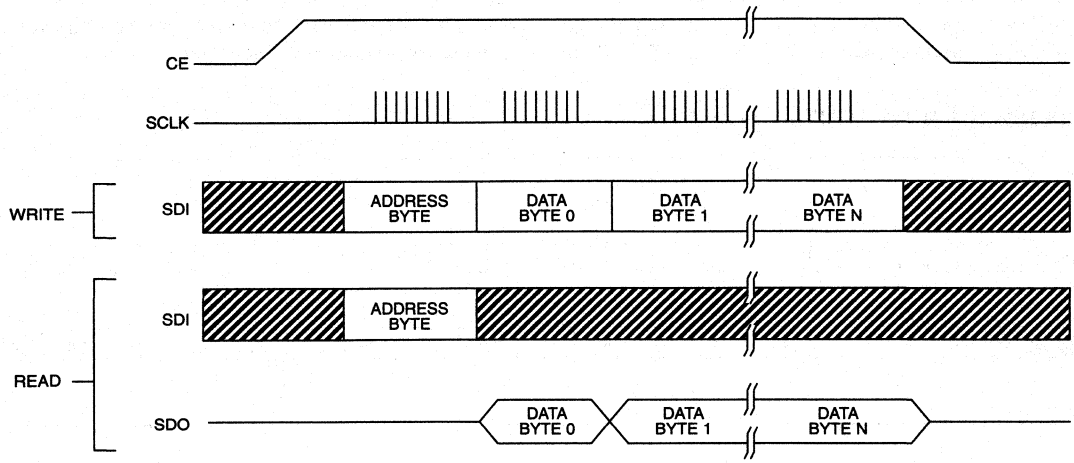


* SCLK can be either polarity.

The address byte is always the first byte entered after CE is driven high. The most significant bit (A7) of this byte determines if a read or write will take place. If A7 is 0, one or more read cycles will occur. If A7 is 1, one or more write cycles will occur.

Data transfers can occur one byte at a time or in multiple byte burst mode. After CE is driven high an address is written to the DS1305. After the address, one or more data bytes can be written or read. For a single byte transfer one byte is read or written and then CE is driven low. For a multiple byte transfer, however, multiple bytes can be read or written to the DS1305 after the address has been written. Each read or write cycle causes the RTC register or RAM address to automatically increment. Incrementing continues until the device is disabled. When the RTC is selected, the address wraps to 00h after incrementing to 1Fh (during a read) and wraps to 80h after incrementing to 9Fh (during a write). When the RAM is selected, the address wraps to 20h after incrementing to 7Fh (during a read) and wraps to A0h after incrementing to FFh (during a write).

SPI MULTIPLE BYTE BURST TRANSFER Figure 9

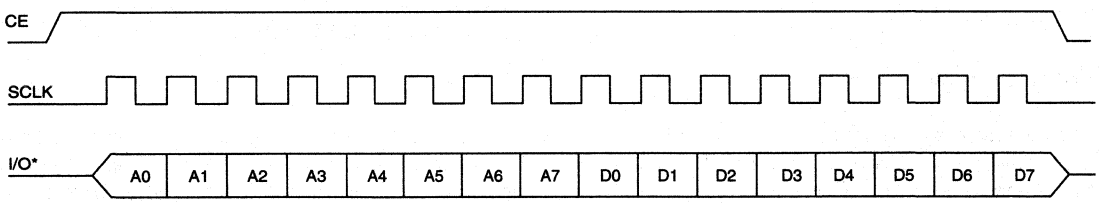


3–WIRE INTERFACE

The 3–wire interface mode operates similar to the SPI mode. However, in 3–wire mode there is one I/O instead of separate data in and data out signals. The 3–wire interface consists of the I/O (SDI and SDO pins tied together), CE, and SCLK pins. In 3–wire mode, each byte is shifted in LSB first unlike SPI mode where each byte is shifted in MSB first.

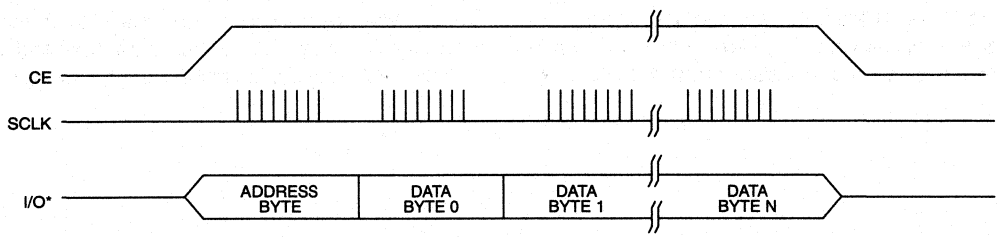
As is the case with the SPI mode, an address byte is written to the device followed by a single data byte or multiple data bytes. Figure 10 illustrates a read and write cycle. Figure 11 illustrates a multiple byte burst transfer. In 3–wire mode, data is input on the rising edge of SCLK and output on the falling edge of SCLK.

3–WIRE SINGLE BYTE TRANSFER Figure 10



* I/O is SDI and SDO tied together

3–WIRE MULTIPLE BYTE BURST TRANSFER Figure 11



* I/O is SDI and SDO tied together

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

The Dallas Semiconductor DS1305 is built to the highest quality standards and manufactured for long term reliability. All Dallas Semiconductor devices are made using the same quality materials and manufacturing methods. However, standard versions of the DS1305 are not exposed to environmental stresses, such as burn–in, that some industrial applications require. Products which have successfully passed through this series of environmental stresses are marked IND or N, denoting their extended operating temperature and reliability rating. For specific reliability information on this product, please contact the factory in Dallas at (214) 450–0448.

3

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C*)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Supply Voltage V_{CC1}, V_{CC2}	V_{CC1}, V_{CC2}		2.5		5.5	V	1, 9
Logic 1 Input	V_{IH}		2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	V_{CC}=2.5V	–0.3		+0.3	V	1
		V_{CC}=5V	–0.3		+0.8		
V_{BAT} Battery Voltage	V_{BAT}		2.5		5.5	V	1
V_{CCIF} Supply Voltage	V_{CCIF}		2.5		5.5	V	14

DC ELECTRICAL CHARACTERISTICS

(0°C to +70°C*; V_{CC} = 2.5 to 5.5V**)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}				+500	µA	
Output Leakage	I_{LO}				1	µA	
Logic 0 Output	V_{OL}	V_{CC}=2.5V			0.4	V	2
		V_{CC}=5V			0.4		
Logic 1 Output	V_{OH}	V_{CCIF}=2.5V	1.6		0.4	V	13
		V_{CCIF}=5V	2.4		0.4		
V_{CC1} Active Supply Current	I_{CC1A}	V_{CC1}=2.5V			0.425	mA	4, 10
		V_{CC1}=5V			1.28		
V_{CC1} Timekeeping Current	I_{CC1T}	V_{CC1}=2.5V			25.3	µA	3, 10
		V_{CC1}=5V			81		
V_{CC1} Standby Current	I_{CC1S}	V_{CC1}=2.5V			25	µA	8, 10
		V_{CC1}=5V			80		
V_{CC2} Active Supply Current	I_{CC2A}	V_{CC2}=2.5V			0.4	mA	4, 11
		V_{CC2}=5V			1.2		
V_{CC2} Timekeeping Current	I_{CC2T}	V_{CC2}=2.5V			0.3	µA	3, 11
		V_{CC2}=5V			1		

* –40°C to 85°C for industrial device
**Unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS (cont'd)

(0°C to +70°C*; V_{CC} = 2.5 to 5.5V**)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
V_{CC2} Standby Current	I_{CC2S}	V_{CC2}=2.5V			100	nA	8, 11
		V_{CC2}=5V			100		
Battery Timekeeping Current	I_{BATT}	V_{BAT}=3V			300	nA	12
Battery Standby Current	I_{BATS}	V_{BAT}=3V			100	nA	12
Trickle Charge Resistors	R1 R2 R3			2 4 8		KΩ KΩ KΩ	
Trickle Charger Diode Voltage Drop	V_{TD}			0.7		V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		10		pF	
Output Capacitance	C_O		15		pF	
Crystal Capacitance	C_X		6		pF	

3–WIRE AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C*; V_{CC} = 2.5V to 5.5V**)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	V_{CC}=2.5V	200			ns	5, 6
		V_{CC}=5V	50				
CLK to Data Hold	t_{CDH}	V_{CC}=2.5V	280			ns	5, 6
		V_{CC}=5V	70				
CLK to Data Delay	t_{CDD}	V_{CC}=2.5V			800	ns	5, 6, 7
		V_{CC}=5V			200		
CLK Low Time	t_{CL}	V_{CC}=2.5V	1000			ns	6
		V_{CC}=5V	250				
CLK High Time	t_{CH}	V_{CC}=2.5V	1000			ns	6
		V_{CC}=5V	250				
CLK Frequency	t_{CLK}	V_{CC}=2.5V			0.6	MHz	6
		V_{CC}=5V	DC		2.0		
CLK Rise and Fall	t_R, t_F	V_{CC}=2.5V			2000	ns	
		V_{CC}=5V			500		

* –40°C to 85°C for industrial device
**Unless otherwise noted.

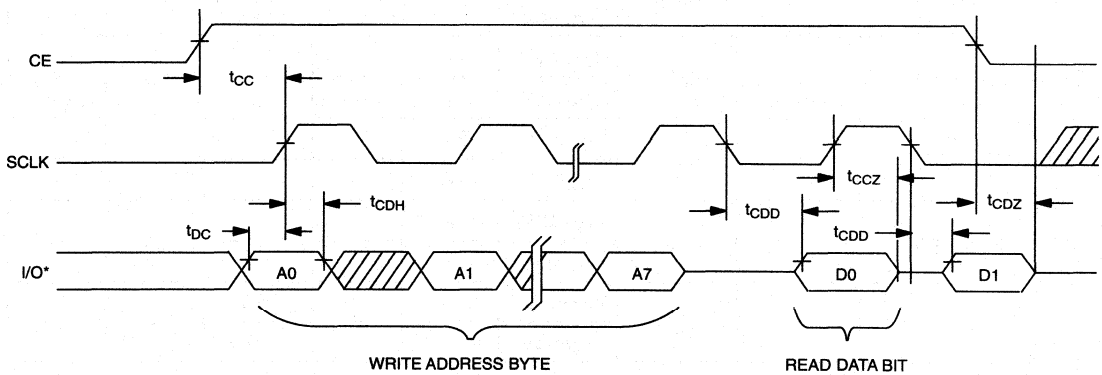
3–WIRE AC ELECTRICAL CHARACTERISTICS (cont'd) (0°C to 70°C*; V_{CC} = 2.5 to 5.5V**)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
CE to CLK Setup	t_{CC}	V_{CC}=2.5V	4			µs	6
		V_{CC}=5V	1				
CLK to CE Hold	t_{CCH}	V_{CC}=2.5V	240			ns	6
		V_{CC}=5V	60				
CE Inactive Time	t_{CWH}	V_{CC}=2.5V	4			µs	6
		V_{CC}=5V	1				
CE to Output High Z	t_{CDZ}	V_{CC}=2.5V			280	ns	5, 6
		V_{CC}=5V			70		
SCLK to Output High Z	t_{CCZ}	V_{CC}=2.5V			280	ns	5, 6
		V_{CC}=5V			70		

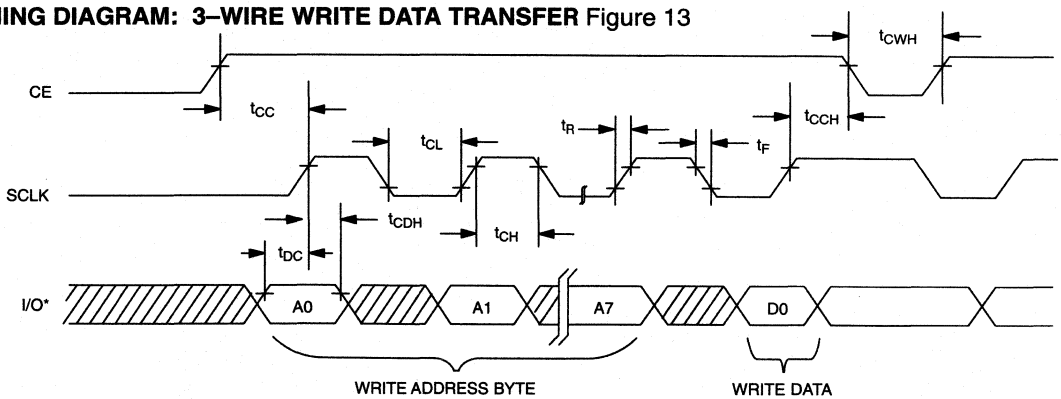
* –40°C to 85°C for industrial device
**Unless otherwise noted.

3

TIMING DIAGRAM: 3–WIRE READ DATA TRANSFER Figure 12



TIMING DIAGRAM: 3–WIRE WRITE DATA TRANSFER Figure 13



* I/O is SDI and SDO tied together.

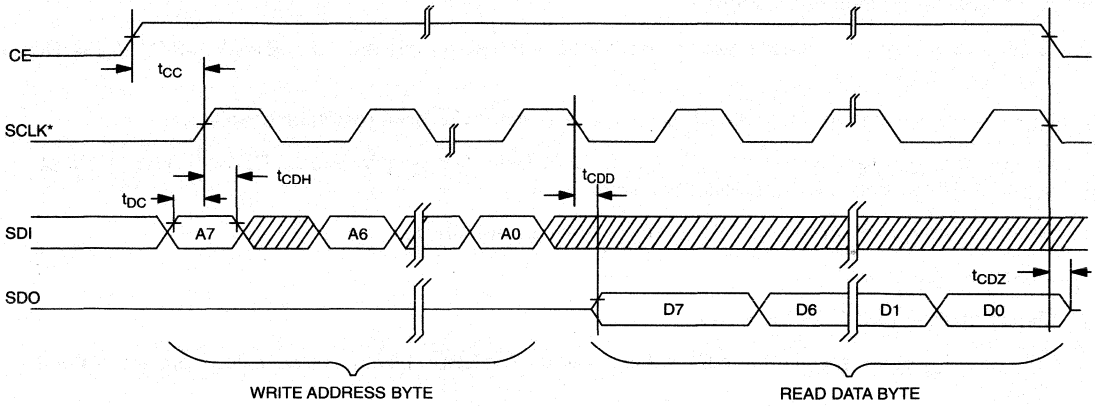
SPI AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C*; V_{CC} = 2.5 to 5.5V**)

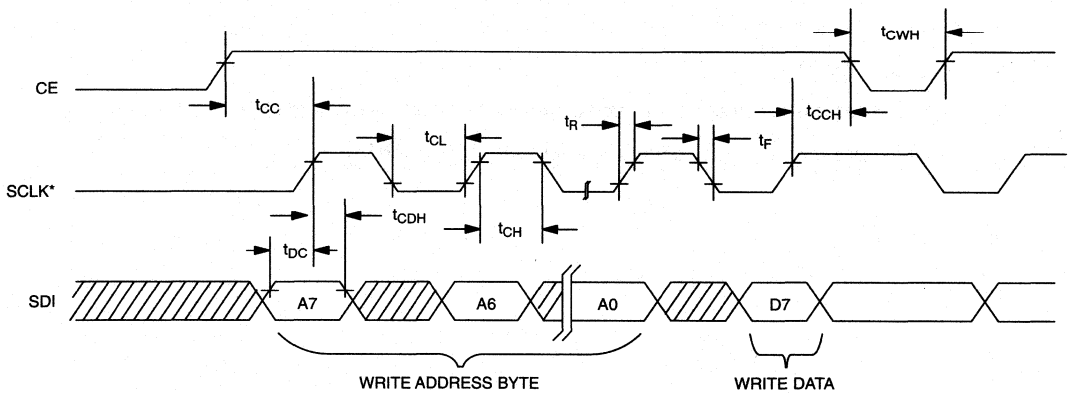
PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	V_{CC}=2.5V	200			ns	5, 6
		V_{CC}=5V	50				
CLK to Data Hold	t_{CDH}	V_{CC}=2.5V	280			ns	5, 6
		V_{CC}=5V	70				
CLK to Data Delay	t_{CDD}	V_{CC}=2.5V			800	ns	5, 6, 7
		V_{CC}=5V			200		
CLK Low Time	t_{CL}	V_{CC}=2.5V	1000			ns	6
		V_{CC}=5V	250				
CLK High Time	t_{CH}	V_{CC}=2.5V	1000			ns	6
		V_{CC}=5V	250				
CLK Frequency	t_{CLK}	V_{CC}=2.5V			0.6	MHz	6
		V_{CC}=5V	DC		2.0		
CLK Rise and Fall	t_R, t_F	V_{CC}=2.5V			2000	ns	
		V_{CC}=5V			500		
CE to CLK Setup	t_{CC}	V_{CC}=2.5V	4			µs	6
		V_{CC}=5V	1				
CLK to CE Hold	t_{CCH}	V_{CC}=2.5V	240			ns	6
		V_{CC}=5V	60				
CE Inactive Time	t_{CWH}	V_{CC}=2.5V	4			µs	6
		V_{CC}=5V	1				
CE to Output High Z	t_{CDZ}	V_{CC}=2.5V			280	ns	5, 6
		V_{CC}=5V			70		

* –40°C to 85°C for industrial device
**Unless otherwise noted.

TIMING DIAGRAM: SPI READ DATA TRANSFER Figure 14



TIMING DIAGRAM: SPI WRITE DATA TRANSFER Figure 15

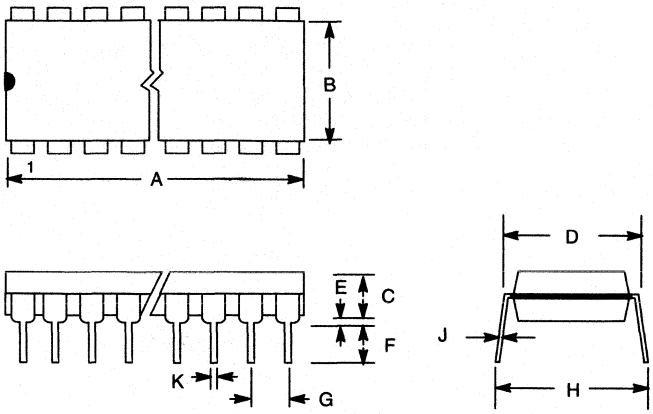


* SCLK can be either polarity

NOTES:

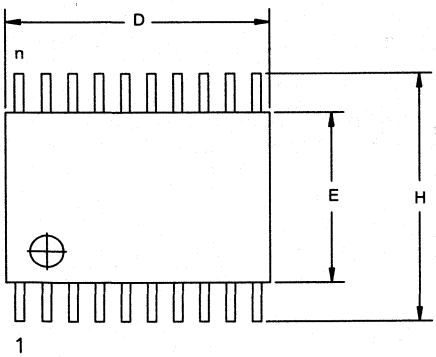
1. All voltages are referenced to ground.
2. Logic zero voltages are specified at a sink current of 4 mA at V_{CC}=5V and 1.5 mA at V_{CC}=2.5V, V_{OL}=GND for capacitive loads.
3. I_{CC1T} and I_{CC2T} are specified with CE set to a logic 0 and $\overline{EOSC}$ bit=0 (oscillator enabled).
4. I_{CC1A} and I_{CC2A} are specified with CE=V_{CC}, SCLK=2 MHz (0–V_{CC}) at V_{CC}=5V; SCLK=500 kHz (0–5V) at V_{CC}=2.5V and $\overline{EOSC}$ bit=0 (oscillator enabled).
5. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10 ms maximum rise and fall time.
6. Measured with 50 pF load.
7. Measured at V_{OH}=2.4V or V_{OL}=0.4V.
8. I_{CC1S} and I_{CC2S} are specified with CE set to a logic 0. The $\overline{EOSC}$ bit must be set to logic one (oscillator disabled).
9. V_{CC}=V_{CC1}, when V_{CC1}>V_{CC2}+0.2V (typical); V_{CC}=V_{CC2}, when V_{CC2}>V_{CC1}.
10. V_{CC2}=0 volts.
11. V_{CC1}=0 volts.
12. (V_{CC1} =V_{CC2}) < V_{BAT}.
13. Logic one voltages are specified at a source current of 1 mA at V_{CC}=5V and 0.4 mA at 2.5V, V_{OH}=V_{CC}.
14. V_{CCIF} must be less than or equal to the largest of V_{CC1}, V_{CC2}, and V_{BAT}.

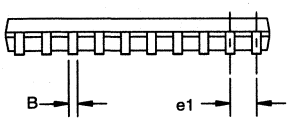
DS1305 16–PIN DIP (300 MIL)

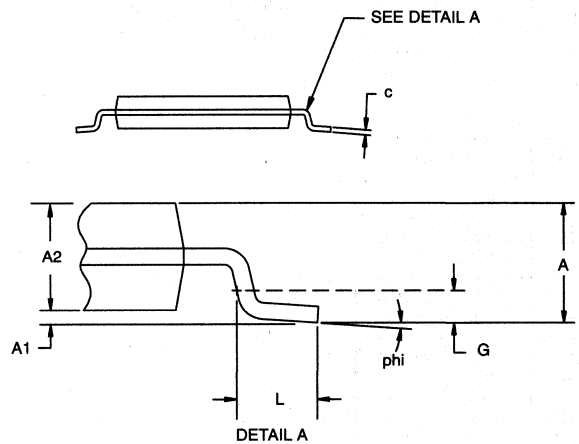


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.740 18.80	0.780 19.81
B IN. MM	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.05	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.320 8.13	0.370 9.40
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

DS1305 20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

56–G2010–000

DALLAS SEMICONDUCTOR

DS1307
64 X 8 Serial Real Time Clock

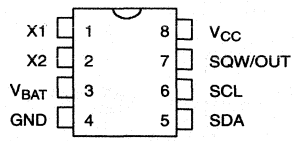
FEATURES

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation
- 56 byte nonvolatile RAM for data storage
- 2–wire serial interface
- Programmable squarewave output signal
- Automatic power fail detect and switch circuitry
- Consumes less than 500 nA in battery backup mode at 25°C
- Optional industrial temperature range –40°C to +85°C
- Available in 8–pin DIP or SOIC

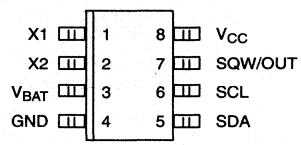
ORDERING INFORMATION

DS1307	Serial Timekeeping Chip; 8–pin DIP
DS1307Z	Serial Timekeeping Chip; 8–pin SOIC (150 mil)

PIN ASSIGNMENT



DS1307 8–PIN DIP (300 MIL)



DS1307Z 8–PIN SOIC (150 MIL)

PIN DESCRIPTION

V_{CC}	–	Primary Power Supply
X1, X2	–	32.768 KHz Crystal Connection
V_{BAT}	–	+3 Volt Battery Input
GND	–	Ground
SDA	–	Serial Data
SCL	–	Serial Clock
SQW/OUT	–	Square wave/Output Driver

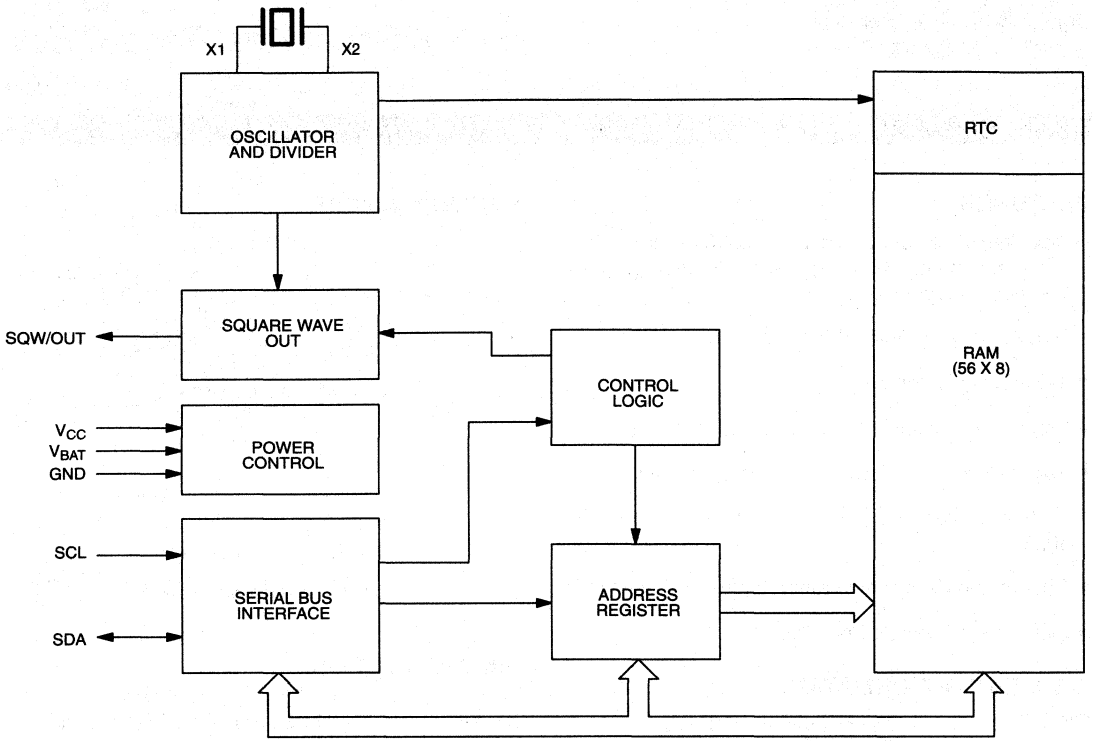
DESCRIPTION

The DS1307 Serial Real Time Clock is a low power full BCD clock calendar plus 56 bytes of nonvolatile SRAM. Address and data are transferred serially via a 2–wire bi–directional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24–hour or 12–hour format with AM/PM indicator. The DS1307 has a built–in power sense circuit which detects power failures and automatically switches to the battery supply.

OPERATION

The DS1307 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by a register address. Subsequent registers can be accessed sequentially until a STOP condition is executed. When V_{CC} falls below 1.25 x V_{BAT} the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{BAT} the device switches into a low current battery backup mode. Upon power up, the device switches from battery to V_{CC} when V_{CC} is greater than V_{BAT}+0.2V and recognizes inputs when V_{CC} is greater than 1.25 x V_{BAT}. The block diagram in Figure 1 shows the main elements of the Serial Real Time Clock. The following paragraphs describe the function of each pin.

DS1307 BLOCK DIAGRAM Figure 1



SIGNAL DESCRIPTIONS

V_{CC}, GND – DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When a 3 volt battery is connected to the device and V_{CC} is below 1.25 x V_{BAT}, reads and writes are inhibited. However, the Timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below V_{BAT} the RAM and timekeeper are switched over to the external 3 volt battery.

V_{BAT} – Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.5 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry as 1.25 x V_{BAT} nominal. A Lithium battery with 35 mAh or greater will back up the DS1307 for more than 10 years in the absence of power.

SCL (Serial Clock Input) – SCL is used to synchronize data movement on the serial interface.

SDA (Serial Data Input/Output) – SDA is the input/output pin for the 2–wire serial interface. The SDA pin is open drain which requires an external pull–up resistor.

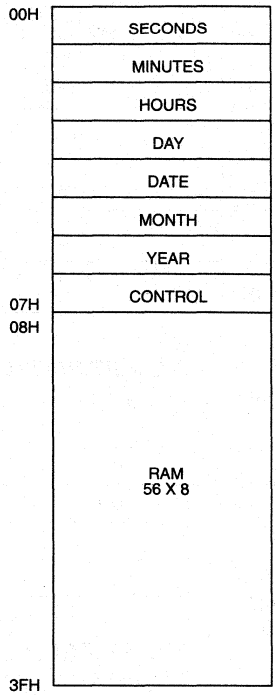
SQW/OUT (Square Wave/ Output Driver) – When enabled, the SQWE bit set to 1, the SQW/OUT pin outputs one of four square wave frequencies (1 Hz, 4 KHz, 8 KHz, 32 KHz). The SQW/OUT pin is open drain which requires an external pull–up resistor.

X1, X2 – Connections for a standard 32.768 KHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 12.5 pF.

RTC AND RAM ADDRESS MAP

The address map for the RTC and RAM registers of the DS1307 is shown in Figure 2. The real time clock registers are located in address locations 00h to 07h. The RAM registers are located in address locations 08h to 3Fh. During a multibyte access, when the address pointer reaches 3Fh, the end of RAM space, it wraps around to location 00h, the beginning of the clock space.

DS1307 ADDRESS MAP Figure 2



CLOCK, CALENDAR, AND ALARM

The time and calendar information is obtained by reading the appropriate register bytes. The real time clock registers are illustrated in Figure 3. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the Binary–Coded Decimal (BCD) format. Bit 7 of Register 0 is the Clock Halt (CH) bit. When this bit is set to a one, the oscillator is disabled. When cleared to a zero, the oscillator is enabled.

The DS1307 can be run in either 12–hour or 24–hour mode. Bit 6 of the hours register is defined as the 12– or 24–hour mode select bit. When high, the 12–hour mode is selected. In the 12–hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24–hour mode, bit 5 is the second 10 hour bit (20–23 hours).

DS1307 TIMEKEEPER REGISTERS Figure 3

	BIT7							BIT0	
00H	CH	10 SECONDS			SECONDS				00–59
	X	10 MINUTES			MINUTES				00–59
	X	12/24	10 HR A/P	10 HR	HOURS				01–12 00–23
	X	X	X	X	X	DAY			0–7
	X	X	10 DATE		DATE				01–28/29 01–30 01–31
	X	X	10 MONTH		MONTH				01–12
	10 YEAR				YEAR				00–99
07H	OUT	X	X	SQWE	X	X	RS1	RS0	

CONTROL REGISTER

The DS1307 Control Register is used to control the operation of the SQW/OUT pin.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT	X	X	SQWE	X	X	RS1	RS0

OUT (Output control): This bit controls the output level of the SQW/OUT pin when the square wave output is disabled. If SQWE = 0, the logic level on the SQW/OUT pin is 1 if OUT = 1 and is 0 if OUT = 0.

SQWE (Square wave Enable): This bit when set to a logic 1 will enable the oscillator output. The frequency of the square wave output depends on the value of the RS0 and RS1 bits.

RS (Rate Select): These bits control the frequency of the square wave output when the square wave output has been enabled. Table 1 lists the square wave frequencies that can be selected with the RS bits.

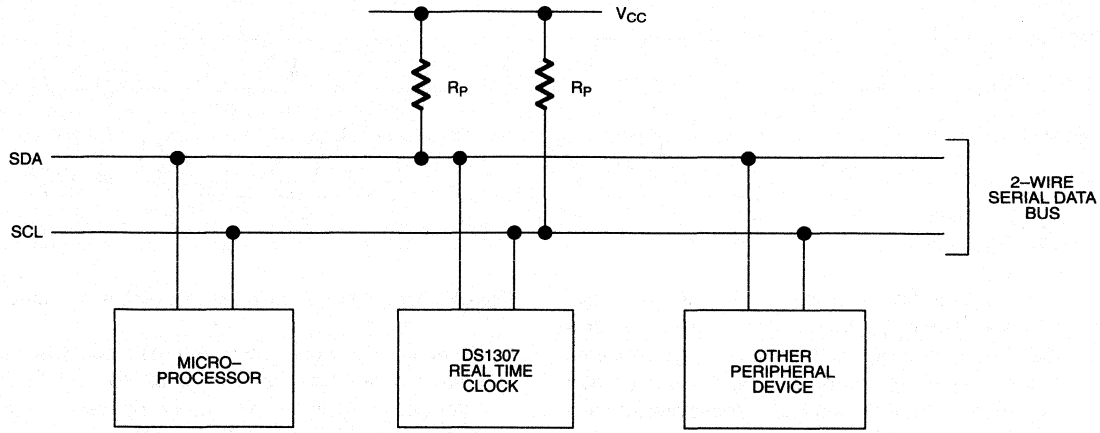
SQUAREWAVE OUTPUT FREQUENCY Table 1

RS1	RS0	SQW OUTPUT FREQUENCY
0	0	1 Hz
0	1	4 KHz
1	0	8 KHz
1	1	32 KHz

2–WIRE SERIAL DATA BUS

The DS1307 supports a bi–directional 2–wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1307 operates as a slave on the 2–wire bus. A typical bus configuration using this 2–wire protocol is show in Figure 4.

TYPICAL 2–WIRE BUS CONFIGURATION Figure 4



The following bus protocol has been defined (see Figure 5).

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

Stop data transfer: A change in the state of the data line from low to high, while the clock line is high defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte–wise and each receiver acknowledges with a ninth bit.

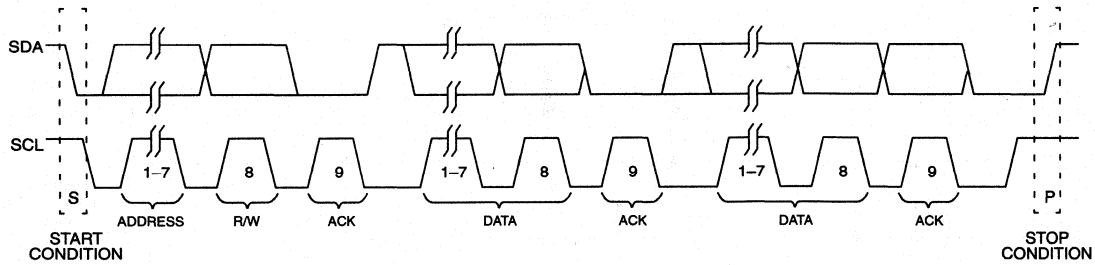
Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. When receiving data from a slave a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

DATA TRANSFER

Figures 5, 6, and 7 detail how data transfer is accomplished on the 2–wire bus. Depending on the state of the R/$\overline{W}$ bit in the transmission protocols as shown in Figures 6 and 7, two types of data transfer are possible:

DATA TRANSFER ON 2–WIRE SERIAL BUS Figure 5



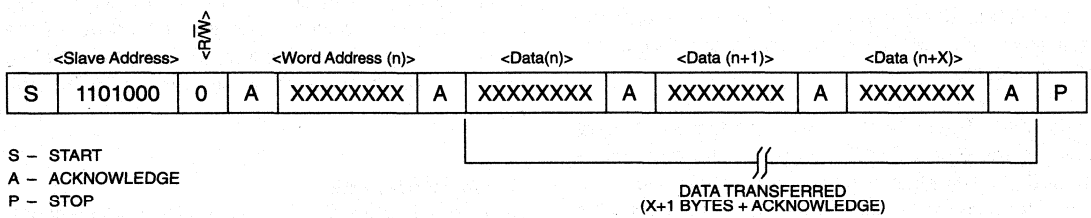
1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transfered with the most significant bit (MSB) first.
2. Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transfered with the most significant bit (MSB) first.

The DS1307 may operate in the following two modes:

1. Slave receiver mode (DS1307 write mode): Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (See Figure 6). The address byte is the first byte received after the start condition is generated by the master. The address byte contains the 7 bit DS1307 address, which is 1101000, followed by the direction bit (R/W\) which for a write is a 0. After receiving and decoding the address byte the DS1307 outputs an acknowledge on the SDA line. After the DS1307 acknowledges the slave address + write bit, the master transmits a register address to the DS1307 This will set the register pointer on the DS1307. The master will then begin transmitting each byte of data with the DS1307 acknowledging each byte received. The master will generate a stop condition to terminate the data write.

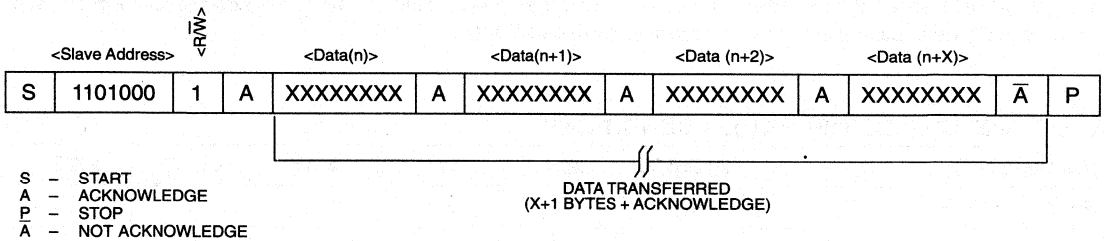
DATA WRITE – SLAVE RECEIVER MODE Figure 6



2. Slave transmitter mode (DS1307 read mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1307 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (See Figure 7). The address byte is the first byte received after the start condition is generated by the master. The address byte contains the 7 bit DS1307 address, which is 1101000, followed by the direction bit (R/W\) which for a read is a 1. After receiving and decoding the address byte the DS1307 inputs an acknowledge on the SDA line. The DS1307 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The DS1307 must receive a Not Acknowledge to end a read.

3

DATA READ – SLAVE TRANSMITTER MODE Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

The Dallas Semiconductor DS1307 is built to the highest quality standards and manufactured for long term reliability. All Dallas Semiconductor devices are made using the same quality materials and manufacturing methods. However, standard versions of the DS1307 are not exposed to environmental stresses, such as burn–in, that some industrial applications require. Products which have successfully passed through this series of environmental stresses are marked IND or N, denoting their extended operating temperature and reliability rating. For specific reliability information on this product, please contact the factory at (214) 450–0448.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	–0.3		+0.8	V	1
V_{BAT} Battery Voltage	V_{BAT}	2.5		3.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}			1	µA	10
I/O Leakage	I_{LO}			1	µA	11
Logic 0 Output	V_{OL}			0.4	V	2
Active Supply Current	I_{CCA}			1.5	mA	9
Standby Current	I_{CCS}			200	µA	3
Battery Current (OSC ON); SQW/OUT OFF	I_{BAT1}		300	500	nA	4
Battery Current (OSC ON); SQW/OUT ON (32 KHz)	I_{BAT2}		480	800	nA	4

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.5V to 5.5V)

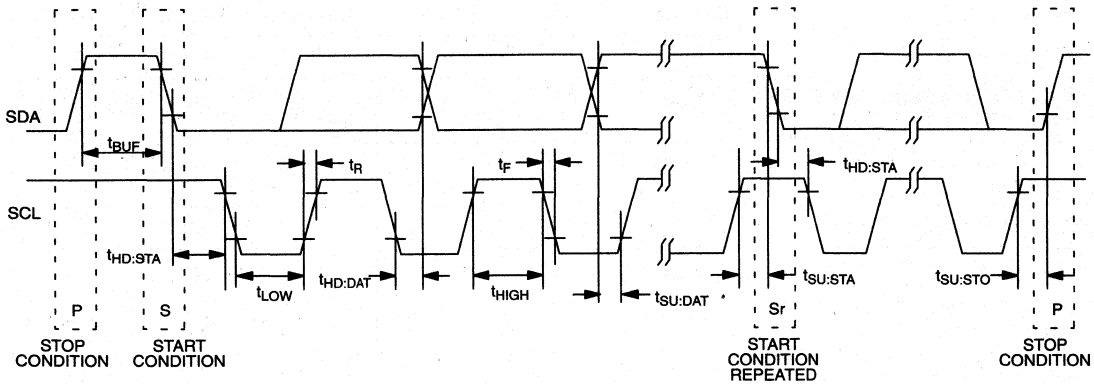
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	0		100	KHz	
Bus Free Time Between a STOP and START Condition	t_{BUF}	4.7			µs	
Hold Time (Repeated) START Condition	$t_{HD:STA}$	4.0			µs	5
LOW Period of SCL Clock	t_{LOW}	4.7			µs	
HIGH Period of SCL Clock	t_{HIGH}	4.0			µs	
Set–up Time for a Repeated START Condition	$t_{SU:STA}$	4.7			µs	
Data Hold Time	$t_{HD:DAT}$	0			µs	6, 7
Data Set–up Time	$t_{SU:DAT}$	250			ns	
Rise Time of Both SDA and SCL Signals	t_R			1000	ns	
Fall Time of Both SDA and SCL Signals	t_F			300	ns	
Set–up Time for STOP Condition	$t_{SU:STO}$	4.7			µs	
Capacitive Load for each Bus Line	C_B			400	pF	8
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Capacitance			12.5		pF	

3

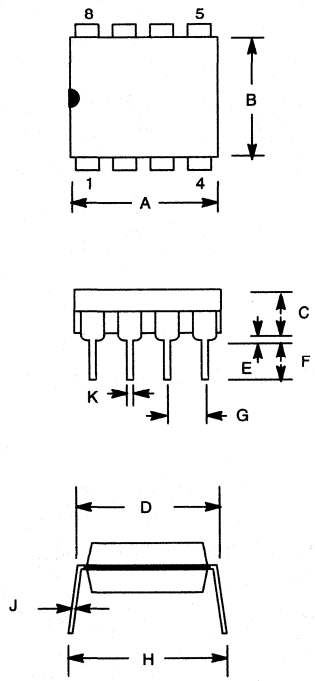
NOTES:

1. All voltages are referenced to ground.
2. Logic zero voltages are specified at a sink current of 5 mA at V_{CC}=4.5V, V_{OL}=GND for capacitive loads.
3. I_{CCS} specified with V_{CC}=5.0V and SDA, SCL=5.0V.
4. V_{CC}=0V, V_{BAT}=3V.
5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8. C_B – total capacitance of one bus line in pF.
9. I_{CCA} – SCL clocking at max frequency = 100 KHz.
10. SCL only.
11. SDA and SQW/OUT

TIMING DIAGRAM

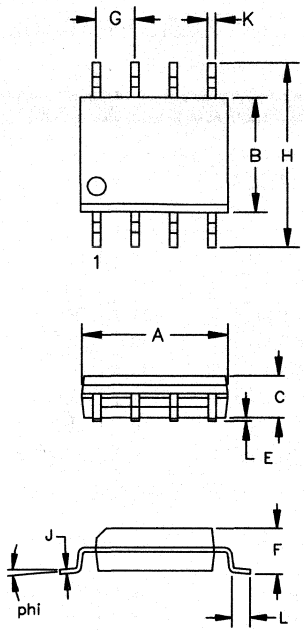


DS1307 64 X 8 SERIAL REAL TIME CLOCK 8–PIN DIP



PKG	8-PIN	
DIM	MIN	MAX
A IN. MM	0.360 9.14	0.400 10.16
B IN. MM	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.320 8.13	0.370 9.40
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

DS1307Z 64 X 8 SERIAL REAL TIME CLOCK 8–PIN SOIC (150 MIL)



PKG	8-PIN (150 MIL)	
DIM	MIN	MAX
A IN. MM	0.188 4.78	0.196 4.98
B IN. MM	0.150 3.81	0.158 4.01
C IN. MM	0.048 1.22	0.062 1.57
E IN. MM	0.004 0.10	0.010 0.25
F IN. MM	0.053 1.35	0.069 1.75
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.230 5.84	0.244 6.20
J IN. MM	0.007 0.18	0.011 0.28
K IN. MM	0.012 0.30	0.020 0.51
L IN. MM	0.016 0.41	0.050 1.27
phi	0°	8°

56–G2008–001

PRELIMINARY

DALLAS SEMICONDUCTOR

DS1315
Phantom Time Chip

FEATURES

- Real time clock keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adjusts for months with fewer than 31 days
- Automatic leap year correction
- No address space required to communicate with RTC
- Provides nonvolatile controller functions for battery backup of SRAM
- Supports redundant battery attachment for high-reliability applications
- Full ±10% V_{CC} operating range
- 5 volt operation

OPTIONS

- Industrial (–45°C to +85°C) operating temperature ranges
- 3 volt operating range
- Packaging: 16–pin DIP, 16 pin SOIC and 20 pin TSSOP

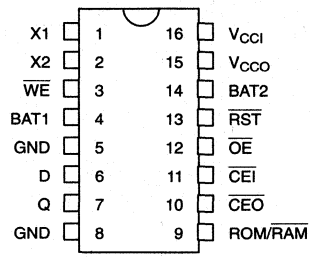
ORDERING INFORMATION

DS1315XX–XX

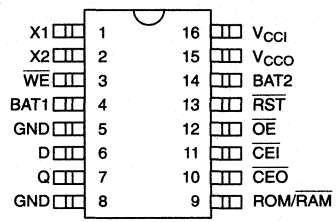
- 3V–3 volt operation*
  5V–5 volt operation
- blank–commercial temp range
  N–industrial temp range
- S–16–pin SOIC
  E–20–pin TSSOP*

*Contact factory for availability

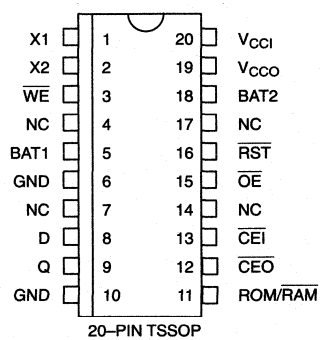
PIN ASSIGNMENT



16–PIN DIP (300 MIL)



16–PIN SOIC (300 MIL)



20–PIN TSSOP

PIN DESCRIPTION

X1, X2	–	32.768 KHz Crystal Connection
$\overline{WE}$	–	Write Enable
BAT1	–	Battery 1 Input
GND	–	Ground
D	–	Data Input
Q	–	Data Output
ROM/$\overline{RAM}$	–	ROM/RAM Mode Select
$\overline{CEO}$	–	Chip Enable Output
$\overline{CEI}$	–	Chip Enable Input
$\overline{OE}$	–	Output Enable
$\overline{RST}$	–	Reset
BAT2	–	Battery 2 Input
V_{CCO}	–	Switched Supply Output
V_{CCI}	–	Power Supply Input

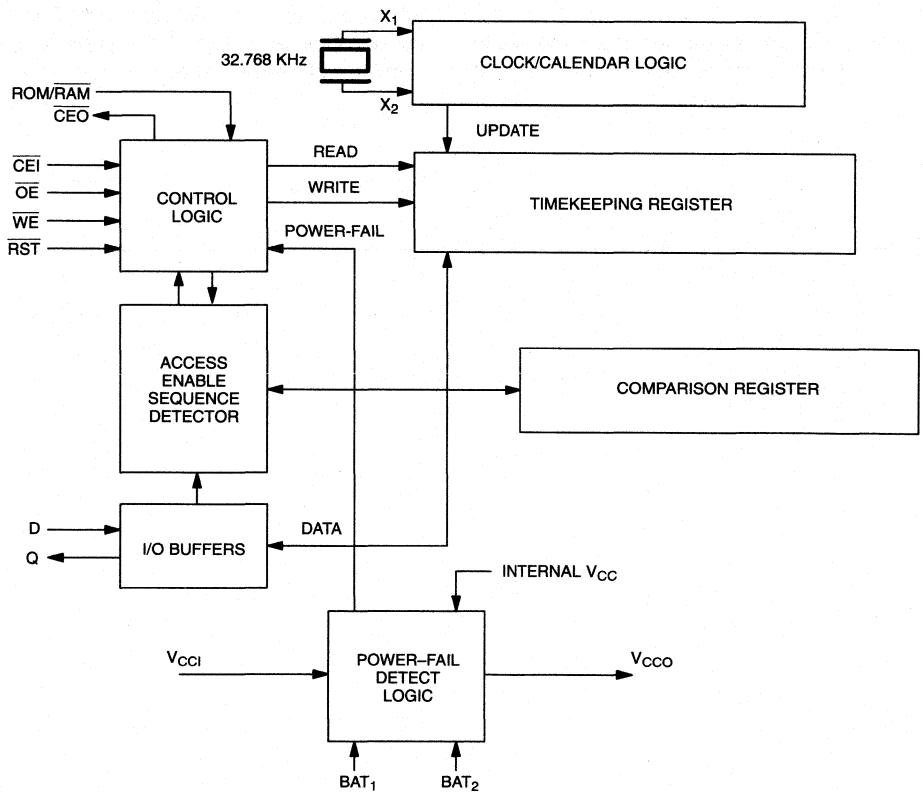
DESCRIPTION

The DS1315 Phantom Time Chip is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch keeps track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including leap year correction. The watch operates in one of two formats: a 12-hour mode with an AM/PM indicator or a 24–hour mode. The nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can be interfaced with either RAM or ROM without leaving gaps in memory.

OPERATION

The block diagram of Figure 1 illustrates the main elements of the Time Chip. The following paragraphs describe the signals and functions.

TIMING BLOCK DIAGRAM Figure 1



Communication with the Time Chip is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on data in (D). All accesses which occur prior to recognition of the 64–bit pattern are directed to memory via the chip enable output pin ($\overline{CEO}$).

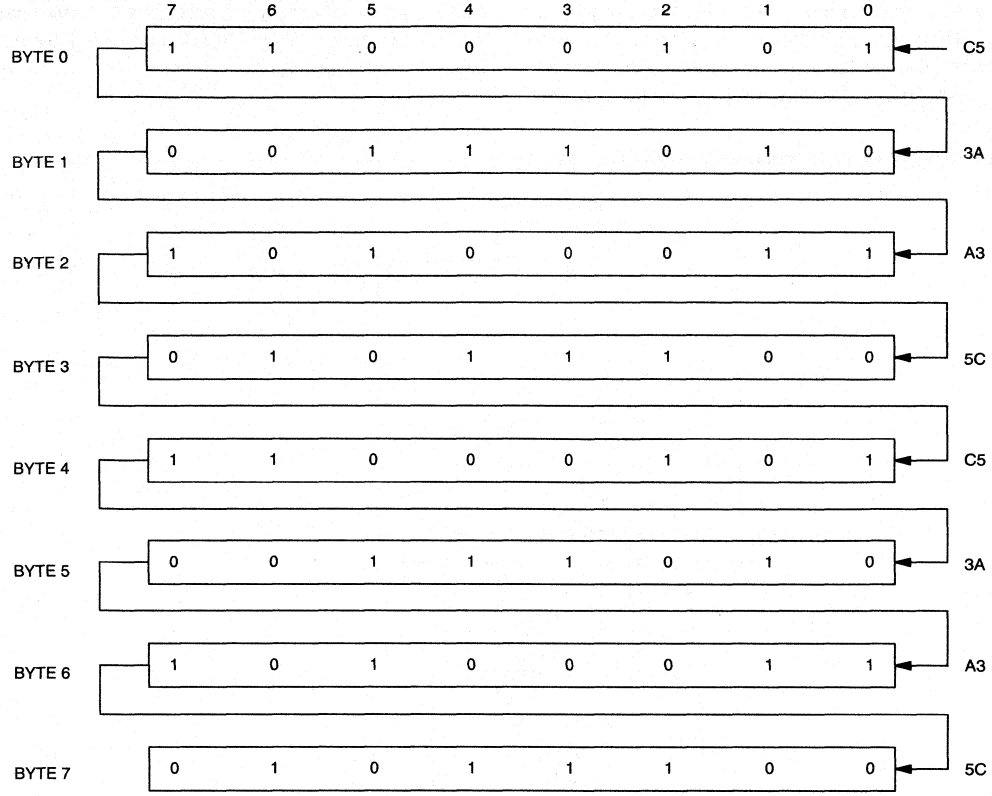
After recognition is established, the next 64 read or write cycles either extract or update data in the Time Chip and $\overline{CEO}$ remains high during this time, disabling the connected memory.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable input ($\overline{CEI}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle using the $\overline{CEI}$ and $\overline{OE}$ control of the Time Chip starts the pattern recognition sequence by moving pointer to the first bit of the 64 bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CEI}$ and $\overline{WE}$ control of the Time Chip. These 64 write cycles are used only to gain access to the Time Chip.

When the first write cycle is executed, it is compared to bit 1 of the 64–bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched. (This bit pattern is shown in Figure 2.) With a correct match for 64 bits, the Time Chip is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the Time Chip to either receive data on D, or transmit data on Q, depending on the level of $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CEI}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Time Chip.

A standard 32,768 KHz quartz crystal can be directly connected to the DS1315 via pins 1 and 2 (X1, X2). The crystal selected for use should have a specified load capacitance (C_L) of 12.5 pF. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks".

TIME CHIP COMPARISON REGISTER DEFINITION Figure 2



NOTE:
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Time Chip are less than 1 in 10^{19}.

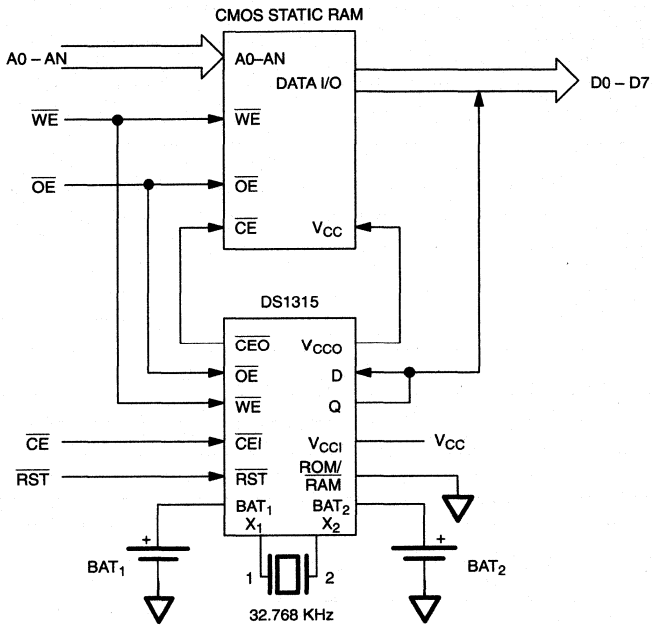
NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the Time Chip is determined by the level of the ROM/$\overline{\text{RAM}}$ select pin. When ROM/$\overline{\text{RAM}}$ is connected to ground, the controller is set in the RAM mode and performs the circuit functions required to make CMOS RAM and the timekeeping function nonvolatile. A switch is provided to direct power from the battery inputs or V_{CCI} to V_{CCO} with a maximum voltage drop of 0.3 volts. The V_{CCO} output pin is used to supply uninterrupted power to CMOS SRAM. The DS1315 also performs redundant battery control for high reliability. On power-fail, the battery with the highest voltage is automatically switched to V_{CCO}. If only one battery is used in the system, the unused battery input should be connected to ground.

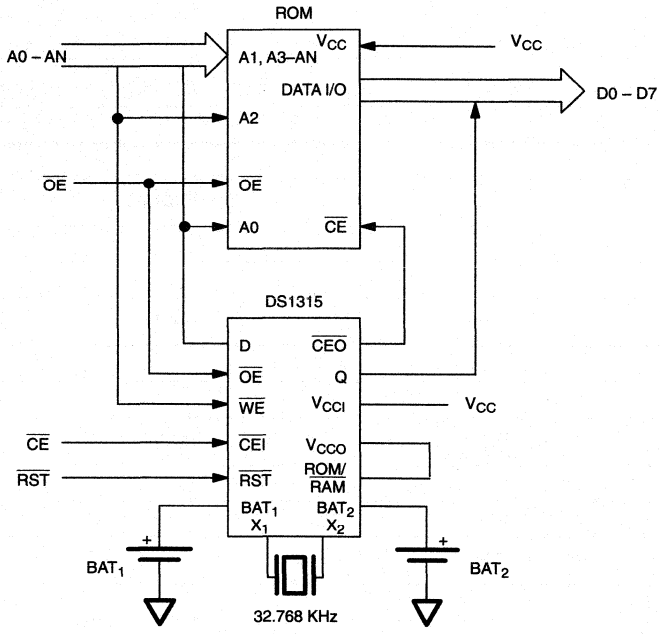
The DS1315 safeguards the Time Chip and RAM data by power-fail detection and write protection. Power-fail detection occurs when V_{CCI} falls below V_{PF} which is set by an internal bandgap reference. The DS1315 constantly monitors the V_{CCI} supply pin. When V_{CCI} is less than V_{PF}, power-fail circuitry forces the chip enable output ($\overline{\text{CEO}}$) to V_{CCI} or V_{BAT}–0.2 volts for external RAM write protection. During nominal supply conditions, $\overline{\text{CEO}}$ will track $\overline{\text{CEI}}$ with a maximum propagation delay of 5 ns. Internally, the DS1315 aborts any data transfer in progress without changing any of the Time Chip registers and prevents future access until V_{CCI} exceeds V_{PF}. A typical RAM/Time Chip interface is illustrated in Figure 3.

When the ROM/$\overline{RAM}$ pin is connected to V_{CCO}, the controller is set in the ROM mode. Since ROM is a read-only device that retains data in the absence of power, battery backup and write protection is not required. As a result, the chip enable logic will force $\overline{CEO}$ low when power fails. However, the Time Chip does retain the same internal nonvolatility and write protection as described in the RAM mode. A typical ROM/Time Chip interface is illustrated in Figure 4.

DS1315 TO RAM/TIME CHIP INTERFACE Figure 3



ROM/TIME CHIP INTERFACE Figure 4



TIME CHIP REGISTER INFORMATION

Time Chip information is contained in eight registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64–bit pattern recognition sequence has been completed. When updating the Time Chip registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 5.

Data contained in the Time Chip registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping though all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12– or 24–hour mode select bit. When high, the 12–hour mode is selected. In the 12–hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24–hour mode, bit 5 is the second 10–hour bit (20 –23 hours).

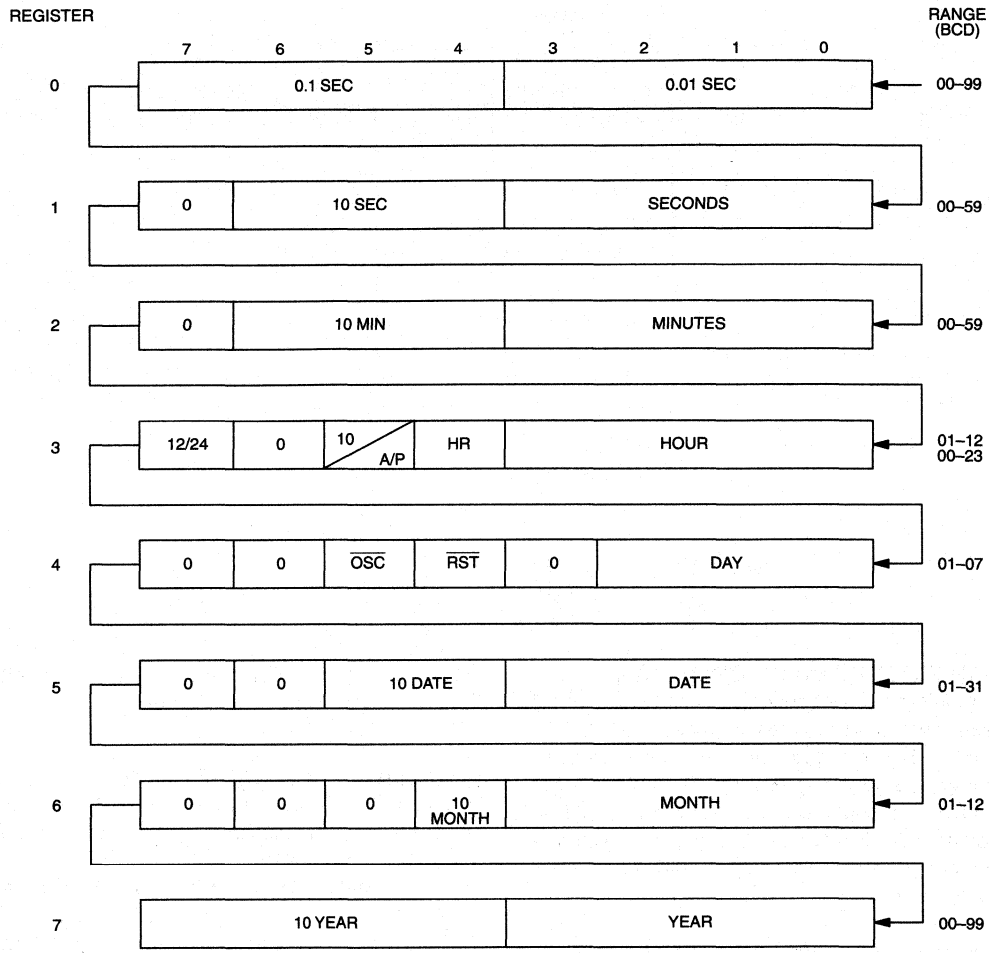
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin input. When the reset bit is set to logic 1, the reset input pin is ignored. When the reset bit is set to logic 0, a low input on the reset pin will cause the Time Chip to abort data transfer without changing data in the timekeeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to logic 0, the oscillator turns on and the real time clock/calendar begins to increment.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits that will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

TIME CHIP REGISTER DEFINITION Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature, commercial range	0°C to 70°C
Operating Temperature, industrial range	–45°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage 5 Volt Operation	V_{CC}	4.5	5.0	5.5	V	1
Power Supply Voltage 3 Volt Operation	V_{CC}	2.7	3.0	3.3	V	1
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	1
Input Logic 0	V_{IL}	–0.3		+0.6	V	1
Battery Voltage V_{BAT1} or V_{BAT2}	V_{BAT1}, V_{BAT2}	2.5		3.7	V	

DC OPERATING ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}			5	mA	6
V_{CC} Power Supply Current, ($V_{CCO} = V_{CCI}$–0.3)	I_{CC01}			150	mA	7
TTL Standby Current ($\overline{CEI} = V_{IH}$)	I_{CC2}			3	mA	6
CMOS Standby Current ($\overline{CEI} = V_{CCI}$–0.2)	I_{CC3}			1	mA	6
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	10
Output Leakage Current (any output)	I_{OL}	–1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = –1.0 mA)	V_{OH}	2.4			V	2
Output Logic 0 Voltage (I_{OUT} = 4.0 mA)	V_{OL}			0.4	V	2
Power Fail Trip Point	V_{PF}	4.25		4.5	V	
Battery Switch Voltage	V_{SW}		V_{BAT1}, V_{BAT2}			

DC POWER DOWN ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} < 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEO}$ Output Voltage	V_{CEO}	V_{CCI}–0.2 or $V_{BAT1,2}$ –0.2			V	8
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			0.5	µA	6
Battery Backup Current @ V_{CCO} = V_{BAT}–0.2V	I_{CCO2}			10	µA	9

AC ELECTRICAL OPERATING CHARACTERISTICS

ROM/$\overline{RAM}$ = GND

(0°C to 70°C; V_{CC} = 5.0 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	65			ns	
$\overline{CEI}$ Access Time	t_{CO}			55	ns	
$\overline{OE}$ Access Time	t_{OE}			55	ns	
$\overline{CEI}$ to Output Low Z	t_{COE}	5			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	5			ns	
$\overline{CEI}$ to Output High Z	t_{OD}			25	ns	
$\overline{OE}$ to Output High Z	t_{ODO}			25	ns	
Read Recovery	t_{RR}	10			ns	
Write Cycle	t_{WC}	65			ns	
Write Pulse Width	t_{WP}	55			ns	
Write Recovery	t_{WR}	10			ns	4
Data Setup	t_{DS}	30			ns	5
Data Hold Time	t_{DH}	0			ns	5
$\overline{CEI}$ Pulse Width	t_{CW}	60			ns	
$\overline{OE}$ Pulse Width	t_{OW}	55			ns	
$\overline{RST}$ Pulse Width	t_{RST}	65			ns	
$\overline{CEI}$ Propagation Delay	t_{PD}			5	ns	2, 3, 11
$\overline{CEI}$ High to Power-Fail	t_{PF}			0	ns	11

AC ELECTRICAL OPERATING CHARACTERISTICS

ROM/$\overline{RAM}$ = V_{CCO} (0°C to 70°C; V_{CC} = 5.0 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	65			ns	
$\overline{CEI}$ Access Time	t_{CO}			55	ns	
$\overline{OE}$ Access Time	t_{OE}			55	ns	
$\overline{CEI}$ to Output Low Z	t_{COE}	5			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	5			ns	
$\overline{CEI}$ to Output High Z	t_{OD}			25	ns	
$\overline{OE}$ to Output High Z	t_{ODO}			25	ns	
Address Setup Time	t_{AS}	5			ns	
Address Hold Time	t_{AH}	5			ns	
Read Recovery	t_{RR}	10			ns	
Write Cycle	t_{WC}	65			ns	
$\overline{CEI}$ Pulse Width	t_{CW}	55			ns	
$\overline{OE}$ Pulse Width	t_{OW}	55			ns	
Write Recovery	t_{WR}	10			ns	4
Data Setup	t_{DS}	30			ns	5
Data Hold Time	t_{DH}	0			ns	5
$\overline{RST}$ Pulse Width	t_{RST}	65			ns	
$\overline{CEI}$ Propagation Delay	t_{PD}			5	ns	2, 3, 11
$\overline{CEI}$ High to Power-Fail	t_{PF}			0	ns	11

3VOLT DEVICE OPERATING RANGE CHARACTERISTICS

DC OPERATING ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 3.0 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}			3	mA	6
Average V_{CC} Power Supply Current, (V_{CCO} = V_{CCI}–0.3)	I_{CC01}			100	mA	7
TTL Standby Current ($\overline{CEI}$ = V_{IH})	I_{CC2}			2	mA	6
CMOS Standby Current ($\overline{CEI}$ = V_{CCI}–0.2)	I_{CC3}			1	mA	6
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
Output Leakage Current (any output)	I_{LO}	–1		+1	µA	

DC OPERATING ELECTRICAL CHARACTERISTICS (cont'd) (0°C to 70°C; V_{CC} = 3.0 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Logic 1 Voltage (I_{OUT} = 0.4 mA)	V_{OH}	2.4			V	2
Output Logic 0 Voltage (I_{OUT} = 1.6 mA)	V_{OL}			0.4	V	2
Power Fail Trip Point	V_{PF}	2.5		2.7	V	
Battery Switch Voltage	V_{SW}		V_{BAT1}, V_{BAT2}			

DC POWER DOWN ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} > 2.7V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEO}$ Output Voltage	V_{CEO}	V_{CCI} or $V_{BAT1,2}$ –0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			0.3	µA	
Battery Backup Current @ $V_{CCO} = V_{BAT}$ –0.2	I_{CCO2}			10	µA	

AC ELECTRICAL OPERATING CHARACTERISTICS

ROM/$\overline{\text{RAM}}$ = GND (0°C to 70°C; V_{CC} = 5.0 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{\text{CEI}}$ Access Time	t_{CO}			100	ns	
$\overline{\text{OE}}$ Access Time	t_{OE}			100	ns	
$\overline{\text{CEI}}$ to Output Low Z	t_{COE}	5			ns	
$\overline{\text{OE}}$ to Output Low Z	t_{OEE}	5			ns	
$\overline{\text{CEI}}$ to Output High Z	t_{OD}			40	ns	
$\overline{\text{OE}}$ to Output High Z	t_{ODO}			40	ns	
Read Recovery	t_{RR}	20			ns	
Write Cycle	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	
Write Recovery	t_{WR}	20			ns	4
Data Setup	t_{DS}	45			ns	5
Data Hold Time	t_{DH}	0			ns	5
$\overline{\text{CEI}}$ Pulse Width	t_{CW}	105			ns	
$\overline{\text{OE}}$ Pulse Width	t_{OW}	100			ns	
$\overline{\text{RST}}$ Pulse Width	t_{RST}	120			ns	
$\overline{\text{CEI}}$ Propagation Delay	t_{PD}			10	ns	2, 3, 12
$\overline{\text{CEI}}$ High to Power-Fail	t_{PF}			0	ns	12

AC ELECTRICAL OPERATING CHARACTERISTICS

ROM/$\overline{\text{RAM}}$ = V_{CCO} (0°C to 70°C; V_{CC} = 3.0 ± 10%)

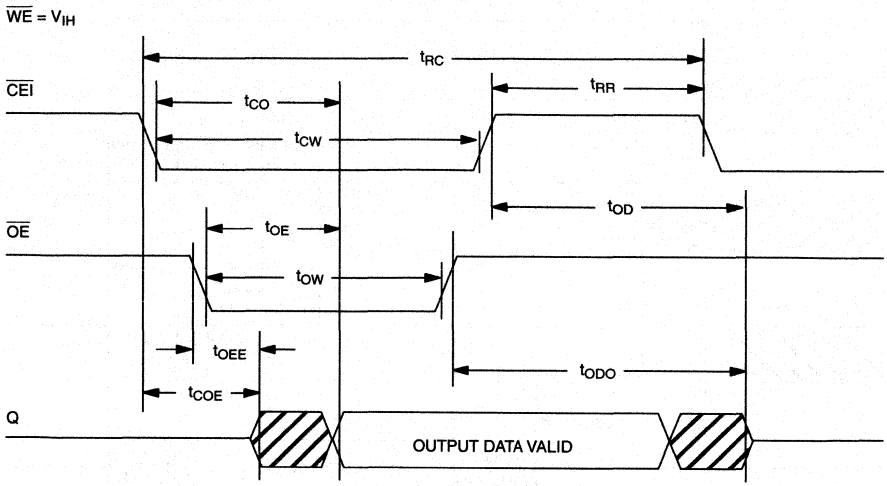
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{\text{CEI}}$ Access Time	t_{CO}			100	ns	
$\overline{\text{OE}}$ Access Time	t_{OE}			100	ns	
$\overline{\text{CEI}}$ to Output Low Z	t_{COE}	5			ns	
$\overline{\text{OE}}$ to Output Low Z	t_{OEE}	5			ns	
$\overline{\text{CEI}}$ to Output High Z	t_{OD}			40	ns	
$\overline{\text{OE}}$ to Output High Z	t_{ODO}			40	ns	
Address Setup Time	t_{AS}	10			ns	
Address Hold Time	t_{AH}	10			ns	
Read Recovery	t_{RR}	20			ns	
Write Cycle	t_{WC}	120			ns	
$\overline{\text{CEI}}$ Pulse Width	t_{CW}	100			ns	
$\overline{\text{OE}}$ Pulse Width	t_{OW}	100			ns	
Write Recovery	t_{WR}	20			ns	4
Data Setup	t_{DS}	45			ns	5
Data Hold Time	t_{DH}	0			ns	5
$\overline{\text{RST}}$ Pulse Width	t_{RST}	120			ns	
$\overline{\text{CEI}}$ Propagation Delay	t_{PD}			5	ns	2, 3, 12

CAPACITANCE

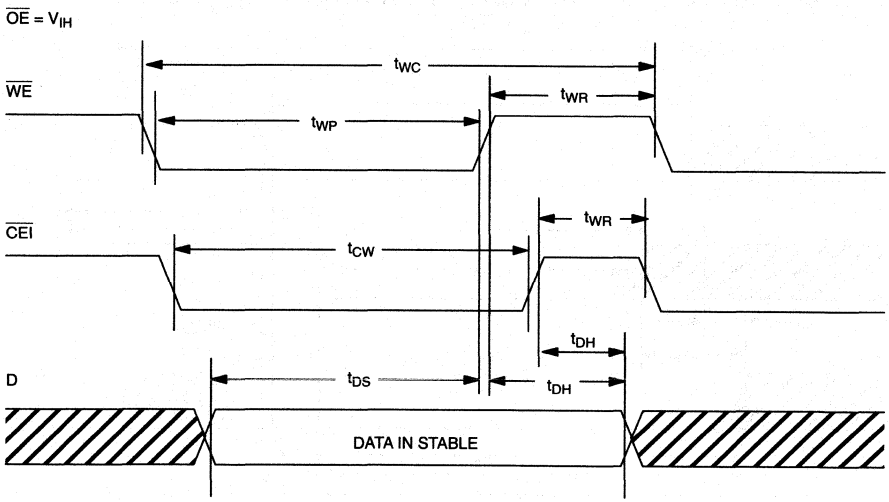
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			10	pF	

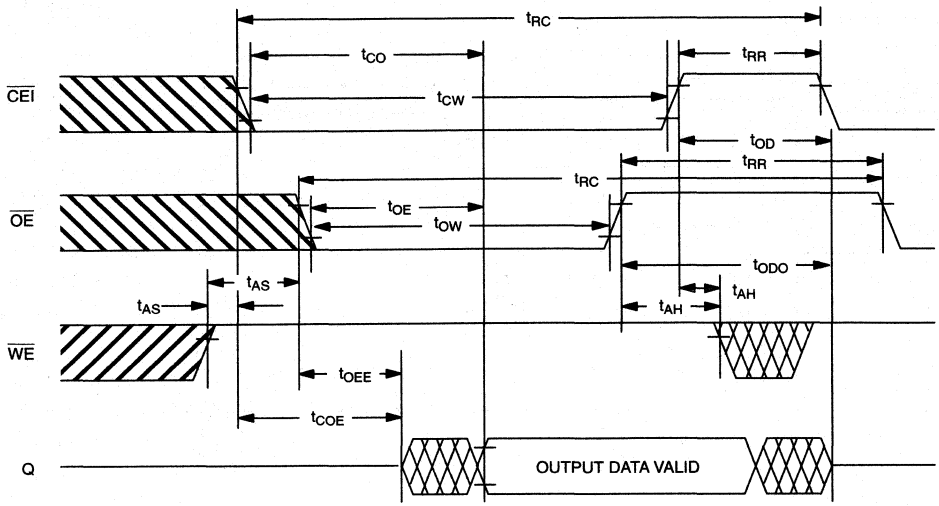
TIMING DIAGRAM: READ CYCLE TO TIME CHIP ROM/$\overline{\text{RAM}}$ = GND Figure 6



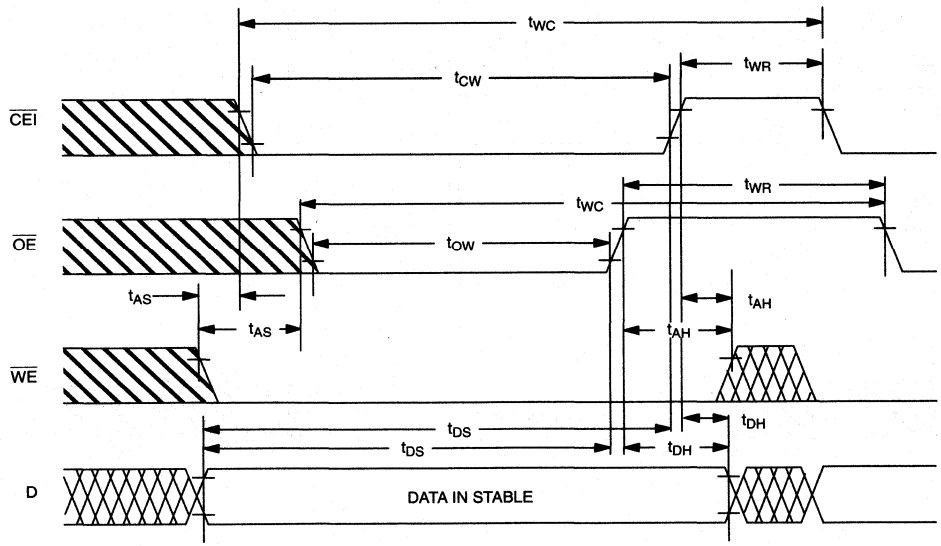
TIMING DIAGRAM: WRITE CYCLE TO TIME CHIP ROM/$\overline{\text{RAM}}$ = GND Figure 7



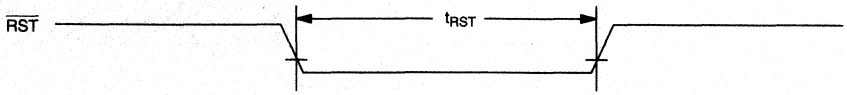
TIMING DIAGRAM: READ CYCLE TO TIME CHIP ROM/$\overline{\text{RAM}}$ = V_{CCO} Figure 8



TIMING DIAGRAM: WRITE CYCLE TO TIME CHIP ROM/$\overline{\text{RAM}}$ = V_{CCO} Figure 9



TIMING DIAGRAM: RESET PULSE Figure 10

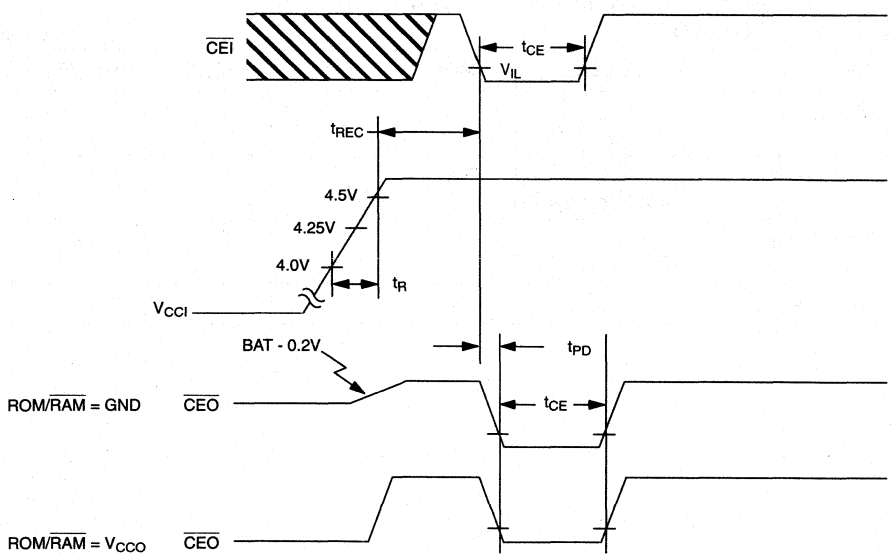


5V DEVICE POWER–UP POWER–DOWN CHARACTERISTICS, ROM/RAM = V_{CCO} OR GND

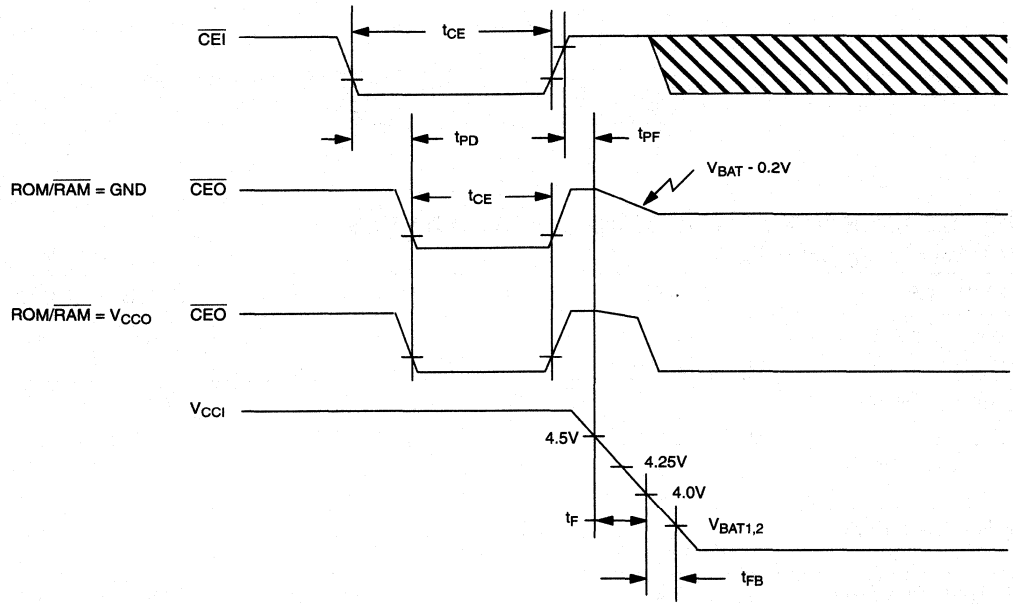
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery Time at Power–Up	t_{REC} V_{CC}>4.5			2	mS	11
V_{CC} Slew Rate Power Down	t_F 4.0≤ V_{CC} ≤ 4.5	300			mS	11
V_{CC} Slew Rate Power Down	t_{FB} 3.0≤ V_{CC} ≤ 4.0	10			mS	11
V_{CC} Slew Rate Power UP	t_R 4.5≤ V_{CC} ≤ 4.0	0			mS	11
$\overline{CEI}$ High to Power–Fail	t_{PF}			0	mS	11

5V DEVICE POWER–UP CONDITION Figure 11



5V DEVICE POWER–DOWN CONDITION Figure 12

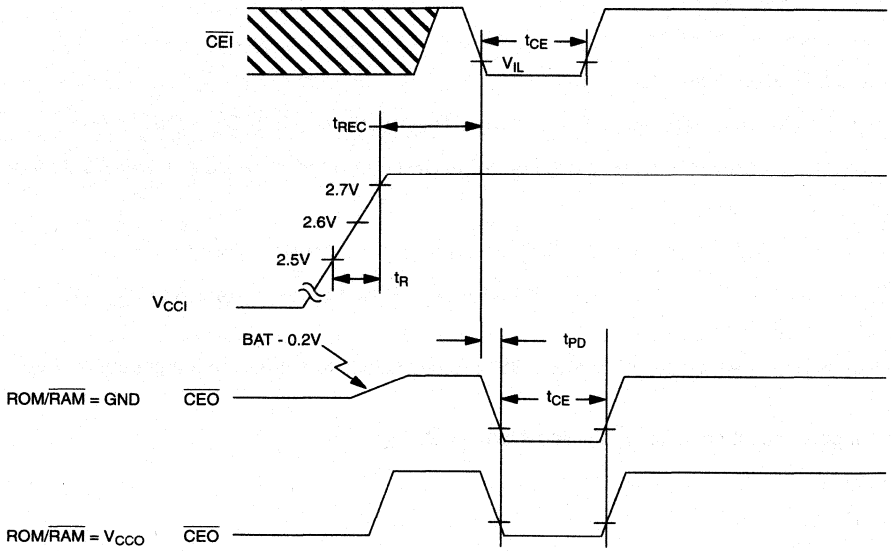


3V DEVICE POWER–UP POWER–DOWN CHARACTERISTICS, ROM/RAM = V_{CCO} OR GND

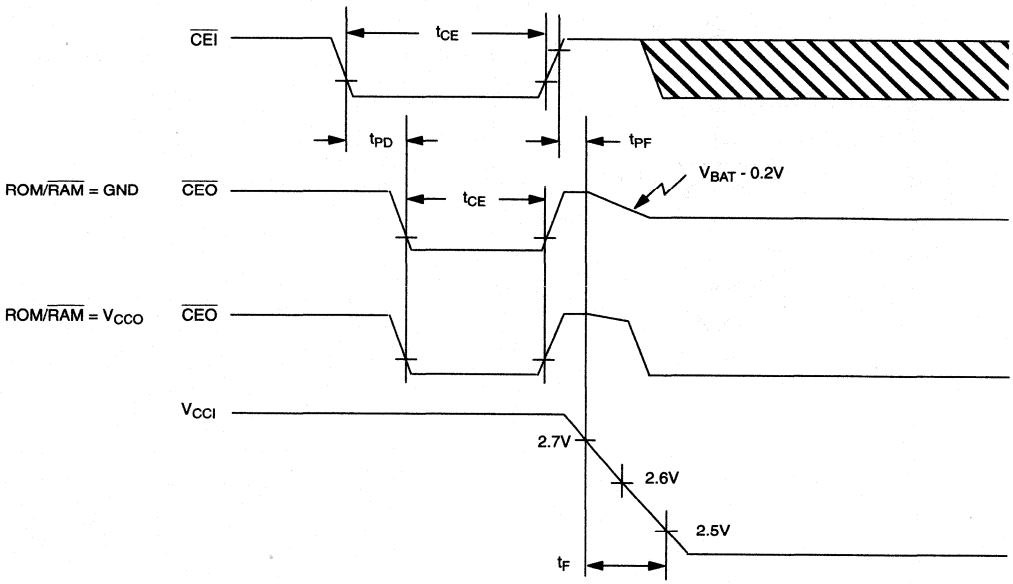
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery Time at Power–Up	t_{REC} V_{CC}>2.7			2	ms	12
V_{CC} Slew Rate Power Down	t_F 2.6≤ V_{CC} ≤ 2.7	300			ms	12
V_{CC} Slew Rate Power UP	t_R 2.7≤ V_{CC} ≤ 2.6	0			ms	12
$\overline{CEI}$ High to Power–Fail	t_{PF}	0			ms	12

3V DEVICE POWER–UP CONDITION Figure 13



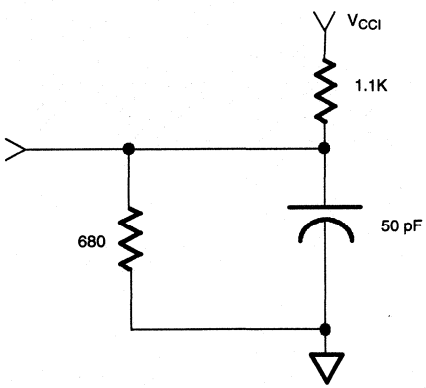
3V DEVICE POWER–DOWN CONDITION Figure 14



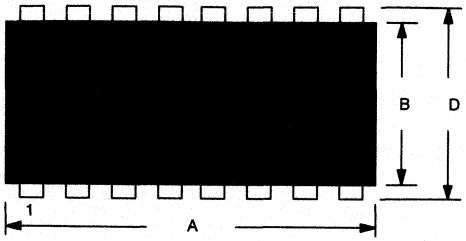
NOTES:

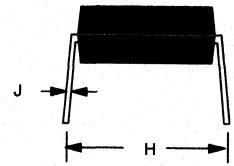
1. All voltages are referenced to ground.
2. Measured with load shown in Figure 15.
3. Input pulse rise and fall times equal 10 ns.
4. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode, or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
5. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode, or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
6. Measured without RAM connected.
7. I_{CC01} is the maximum average load current the DS1315 can supply to external memory.
8. Applies to $\overline{CEO}$ with the ROM/$\overline{RAM}$ pin grounded. When the ROM/$\overline{RAM}$ pin is connected to V_{CCO}, $\overline{CEO}$ will go to a low level as V_{CCI} falls below V_{BAT}.
9. I_{CC02} is the maximum average load current that the DS1315 can supply to memory in the battery backup mode.
10. Applies to all input pins except $\overline{RST}$. $\overline{RST}$ is pulled internally to V_{CCI}.
11. See Figures 11 and 12.
12. See Figures 13 and 14.

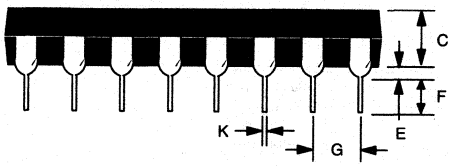
OUTPUT LOAD Figure 15



DS1315 TIME CHIP 16–PIN DIP

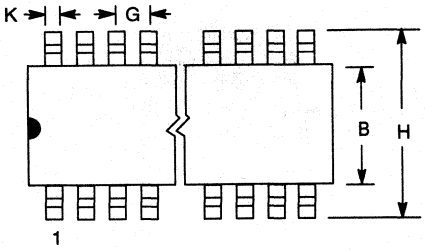


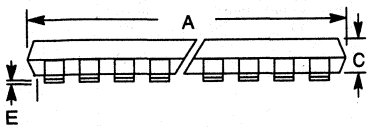


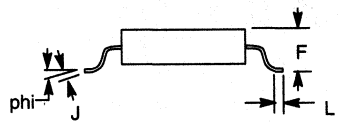


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.740	0.780
B IN. MM	0.240	0.260
C IN. MM	0.120	0.140
D IN. MM	0.300	0.325
E IN. MM	0.015	0.040
F IN. MM	0.110	0.140
G IN. MM	0.090	0.110
H IN. MM	0.300	0.370
J IN. MM	0.008	0.012
K IN. MM	0.015	0.021

DS1315 TIME CHIP 16–PIN SOIC

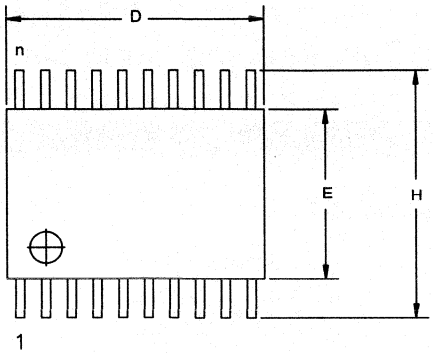


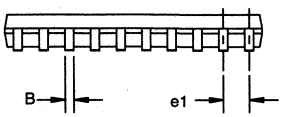


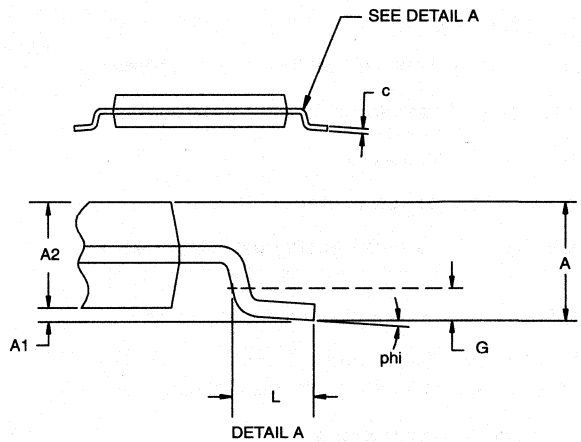


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN MM	0.398 10.11	0.416 10.57
J IN MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN MM	0.016 0.40	0.040 1.02
PHI	0°	8°

DS1315 TIME CHIP 20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

56–G2010–000

DALLAS SEMICONDUCTOR

DS1384
Watchdog Timekeeping Controller

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities
- Programmable interrupts and square wave outputs
- Bytewide RAM-like access
- 50 bytes of on board user RAM
- Greater than 10 years timekeeping and data retention in the absence of power with small lithium coin cells
- Supports up to 128K x 8 of external static RAM
- All timekeeping registers and on board RAM are individually addressable via the address and data bus

ORDERING INFORMATION

DS1384FP–XXX 44 pin quad flat pack

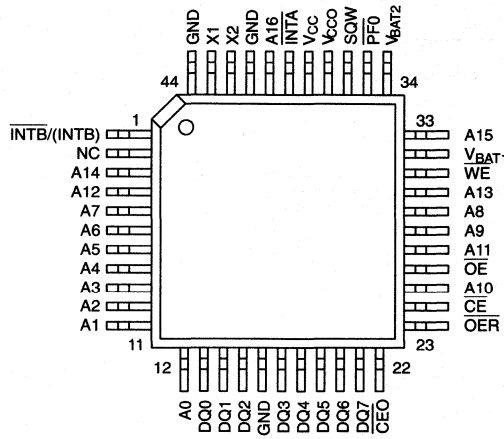
–120 120 ns access
–150 150 ns access

DS1384T–XXX 44 pin thin quad flat pack*

–120 120 ns access
–150 150 ns access

* Contact factory for availability.

PIN ASSIGNMENT



PIN DESCRIPTION

$\overline{INTA}$	-	Interrupt Output A
$\overline{INTB}$(INTB)	-	Interrupt Output B
A0-A16	-	Address Inputs
DQ0-DQ7	-	Data Input/Output
$\overline{CE}$	-	Chip Enable
$\overline{OE}$	-	Output Enable
$\overline{WE}$	-	Write Enable
V_{CC}	-	+5 Volt Input
GND	-	Ground
NC	-	No Connection
SQW	-	Square Wave Output
X1, X2	-	32.768 kHz Crystal Connections
$\overline{PFO}$	-	Power Fail Output
$\overline{CEO}$	-	Chip Enable RAM
$\overline{OER}$	-	Output Enable RAM
V_{CCO}	-	Voltage Out
V_{BAT1}	-	+3 Volt Battery Input
V_{BAT2}	-	+3 Volt Battery Input

DESCRIPTION

The DS1384 Watchdog Timekeeping Controller is a self-contained real time clock, alarm, watchdog timer, and interval timer which provides control of up to 128K x 8 of external low power CMOS static RAM in a 44–pin quad flat pack package. An external crystal and battery are the only components required to maintain time of day and RAM memory contents in the absence of power. Access to all RTC functions and the external RAM is the same as conventional bytewide SRAM. Data is maintained in the Watchdog Timekeeper by intelligent control circuitry which detects the status of V_{CC} and write protects both memory and timekeeping functions when V_{CC} is out of tolerance. Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The timekeeper operates in either 12- or 24-hour format with an AM/PM indicator. The watchdog internal timerprovides watchdog alarm windows and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week. All of the RTC functions and the internal 50 bytes of RAM reside in the lower 64 bytes of the attached RAM memory map. The externally attached static RAM is controlled by the DS1384 via the $\overline{OER}$ and $\overline{CEO}$ signals.

Automatic backup and write protection for an external SRAM is provided through the V_{CCO}, $\overline{CEO}$ and $\overline{OER}$ pins. The lithium energy source used to permanently power the real time clock is also used to retain RAM data in the absence of V_{CC} power through the V_{CCO} pin. The chip enable output to RAM ($\overline{CEO}$) and the output enable to RAM ($\overline{OER}$) are controlled during power transients to prevent data corruption. The DS1384 is a complete one–chip solution in that an external crystal and battery are the only components required to maintain time of day memory status in the absence of power.

SIGNAL DESCRIPTIONS

V_{CC}, GND – DC power inputs: DC operating voltage is provided to the device on these pins. V_{CC} is the +5V input.

V_{BAT1}, V_{BAT2} – Battery inputs for any standard 3–volt lithium cell or other energy source. Battery voltage must be held between 2.4 and 4 volts for proper operation. In the absence of power, the DS1384 will have a maximum load of 0.5 µA at 25°C. This should be added to the amount of current drawn from the external RAM in standby mode at 25°C to size the external energy source. The DS1384 samples V_{BAT1} and V_{BAT2} and always selects the battery with the higher voltage. If only one battery is used, the unused battery input must be grounded.

A16–A0 – Address Bus (inputs): The address bus inputs qualified by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, and V_{CC} voltage are used to select the on–chip 64 timekeeping/RAM registers within the memory map of the external SRAM controlled as nonvolatile storage. When the qualified address bus value is within the range of 00000H – 0003FH, one of the internal registers will be selected and $\overline{OER}$ will remain inactive. When the value is outside of the range, $\overline{OE}$ will be passed through to $\overline{OER}$.

D7–D0 – Data Bus (bi–directional): When a qualified address from 00000H through 0003FH is presented to the device, data is passed to or from the on–chip 64 timekeeping/RAM registers via the data bus lines. Data will be written on the rising edge of $\overline{WE}$ when $\overline{CE}$ is active. If $\overline{CE}$ is active without $\overline{WE}$, data is read from the device and driven onto the data bus pins when $\overline{OE}$ is low.

V_{CCO} – Switched DC power for SRAM (output): This pin will be connected to V_{CC} when V_{CC} voltage is above V_{SO} (the greater of V_{BAT1} or V_{BAT2}). When V_{CC} voltage falls below this level, V_{CCO} will be connected to the higher voltage battery pin.

$\overline{CEO}$ – RAM chip enable (output; active low): When power is good the $\overline{CE}$ input will be passed through to $\overline{CEO}$. If V_{CC} is below V_{PF}, $\overline{CEO}$ will remain at an inactive high level.

$\overline{OER}$ – RAM output enable (output; active low): When power is good and the address value is not within the range of 00000H and 0003FH, and $\overline{CE}$ is active, the $\overline{OE}$ input will be passed through to $\overline{OER}$. If these conditions are not met, $\overline{OER}$ will remain at an inactive high level.

$\overline{CE}$ – Chip enable (input; active low): The chip enable signal must be asserted low during a bus cycle to access the on–chip timekeeping RAM registers, or to access the external RAM via $\overline{CEO}$.

$\overline{OE}$ – Output enable (input; active low): The output enable signal identifies the time period when either the RTC or the external SRAM drives the bus with read data, provided that $\overline{CE}$ is valid with $\overline{WE}$ disabled. When one of the 64 on–chip registers is selected during a read

cycle, the $\overline{OE}$ is the enable signal for the DS1384 output buffers and the data bus will be driven with read data. When the external RAM is selected during a read cycle, the $\overline{OE}$ signal will be passed through to the $\overline{OER}$ pin so that read data will be driven by the external SRAM.

$\overline{WE}$ – Write enable (input; active low): The write enable signal identifies the time period during which data is written to either the on–chip registers or to an external SRAM location. When one of the on–chip 64 registers is addressed, data will be written to the selected register on the rising edge of $\overline{WE}$.

$\overline{INTA}$ – Interrupt Output A (output; active low): Interrupt output A can be programmed as a Time of Day Alarm or as a Watchdog Alarm (Interrupt output B becomes the alternate function). In addition, $\overline{INTA}$ can be programmed to output either a pulse or a level.

$\overline{INTB}$ – Interrupt Output B (output; active high or low): Interrupt output B outputs the alarm (Time of Day or Watchdog) that is not selected for $\overline{INTA}$. Interrupt output B is programmable high or low.

X1, X2 – Crystal inputs: Connections for a standard 32.768 KHz quartz crystal Daiwa part number DT–26S, Seiko part number DS–VT–200, of equivalent. When ordering, request a load capacitance or 6 pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6 pF.

For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks".

SQW – Square Wave (output): This pin can be programmed to output a 1024 Hz square wave signal. When the signal is turned off, the pin is high Z.

$\overline{PFO}$ – Power Fail Signal (output; active low when V_{WP} occurs): High state occurs t_{REC} after power–up and $V_{CC} \geq 4.5$ volts.

ADDRESS DECODING

The DS1384 accommodates 17 address lines which allows direct connection of up to 128K bytes of static RAM. The lower 14 bytes of RAM, regardless of the density used, will always contain the timekeeping, alarm, and watchdog registers. The 14 clock registers reside in the lower 14 RAM locations without conflict by inhibiting the $\overline{OER}$ (output enable RAM) signal during clock access. Since the watchdog timekeeping chip actually contains 64 registers (14 RTC and 50 user RAM), the lower 64 bytes of any attached memory resides within the DS1384. However, the RAM's physical location is transparent to the user and the memory map looks continuous from the first clock address to the upper most attached RAM address.

OPERATION – READ CYCLE

The DS1384 executes a read cycle whenever $\overline{WE}$ is inactive (high) and $\overline{CE}$ and $\overline{OE}$ are active (low). The unique address specified by the address inputs (A0–A16) defines which of the on–chip 64 RTC/RAM or external SRAM locations is to be accessed.

When the address value presented to the DS1384 is in the range of 00000H through 0003FH, one of the 64 on–chip registers will be selected and valid data will be available to the eight data output drivers within t_{ACC} (access time) after the address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If they are not, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than the address access time. When one of the on–chip registers is selected for read, the $\overline{OER}$ signal will remain inactive throughout the read cycle.

When the address value presented to the DS1384 is in the range of 00040H through 1FFFFH, an external SRAM location will be selected. In this case the $\overline{OE}$ signal will be passed to the $\overline{OER}$ pin, with the specified delay times of t_{AOEL} or t_{OERL}.

OPERATION – WRITE CYCLE

The DS1384 is in the write mode whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active (low) state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been

enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{WEZ} from its falling edge.

When the address value presented to the DS1384 during the write is in the range of 00000H through 0003FH, one of the 64 on–chip registers will be selected and data will be written into the device.

When the address value presented to the DS1384 during the write is in the range of 00040H through 1FFFFH, an external SRAM location will be selected.

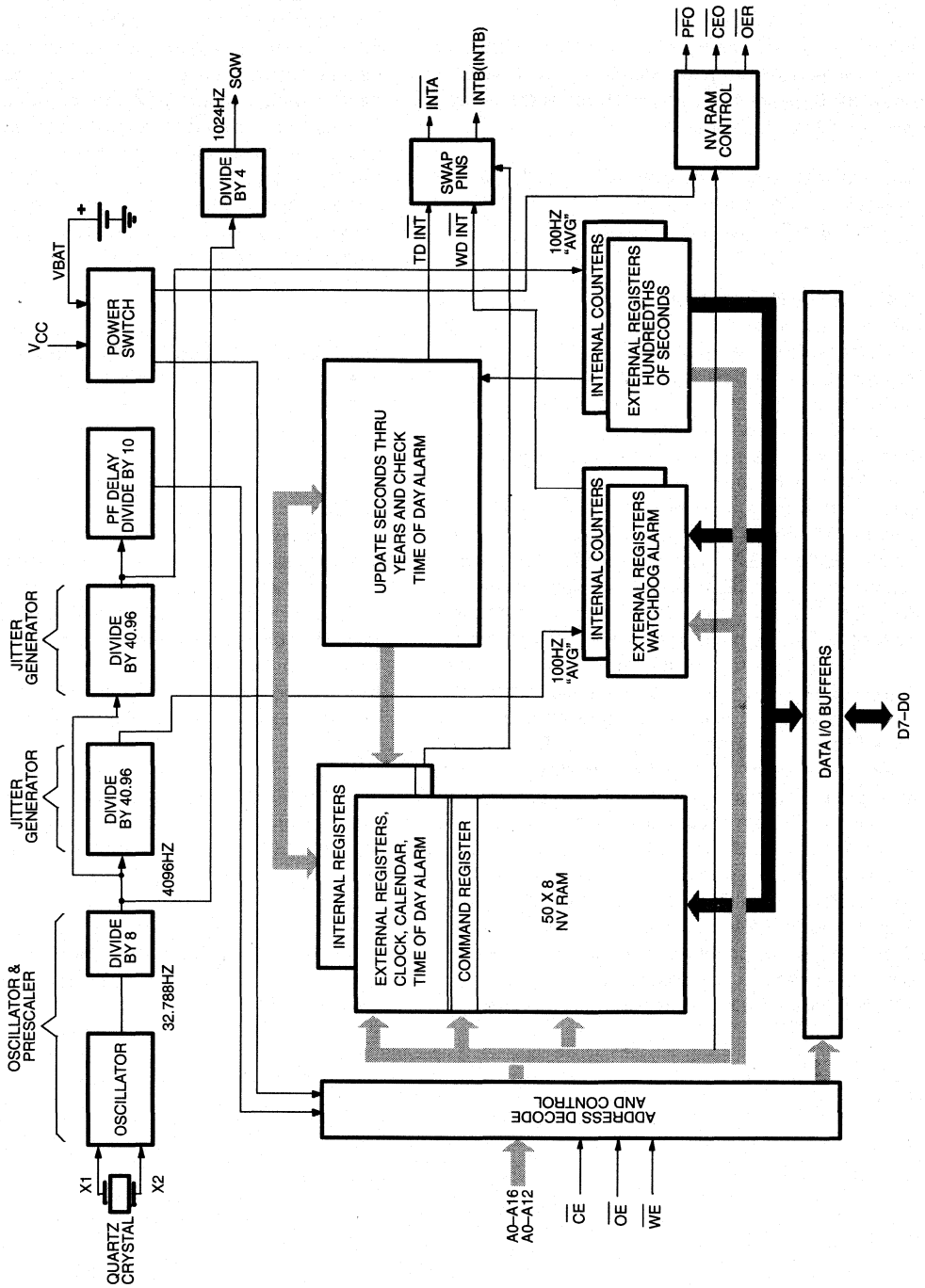
DATA RETENTION MODE

When V_{CCI} is within nominal limits (V_{CC} > 4.5 volts) the DS1384 can be accessed as described above with read or write cycles. However, when V_{CC} is below the power fail point, V_{PF}, (point at which write protection occurs) the internal clock registers and external RAM is blocked from access. This is accomplished internally by inhibiting access to the clock registers via the $\overline{CE}$ signal. At this time the power fail output signal ($\overline{PFO}$) is driven active and will remain active until V_{CC} returns to nominal levels. External RAM access is inhibited in a similar manner by forcing $\overline{CEO}$ to high level. This level is within 0.2 volts of the V_{CCI} input. $\overline{CEO}$ will remain at this level as long as V_{CCI} remains at an out–of–tolerance condition. When V_{CCI} falls below the level of the battery (V_{BAT1} or V_{BAT2}), power input is switched from the V_{CCI} pin to the V_{BAT} pin and the clock registers are maintained from the attached battery supply. External RAM is also powered by the V_{BAT} input when V_{CCI} is below V_{BAT} pin through the V_{CCO} pin. The V_{CCO} pin is capable of supplying 100 µA of current to the attached memory with less than 0.3 volts drop under this condition. On power up, when V_{CCI} returns to in–tolerance conditions, write protection continues for 150 ms by inhibiting $\overline{CEO}$. The $\overline{PFO}$ signal also remains active during this time. The DS1384 is capable of supporting two batteries which are used in a redundant fashion for applications which require added reliability or increased battery capacity. When two batteries are used, the higher of the two is selected for use. A selected battery will remain as backup supply until it is significantly below the other. When the selected battery voltage falls below the alternate battery by about 0.6 volts, the alternate battery is selected and then becomes the backup supply. This switching occurs transparent to the user and continues until both batteries are exhausted. When only a single battery is required, both battery inputs can be connected together. However, a more effective method of using a single battery supply is to ground the unused battery input. When using a single battery, V_{BAT1} is the prefered input.

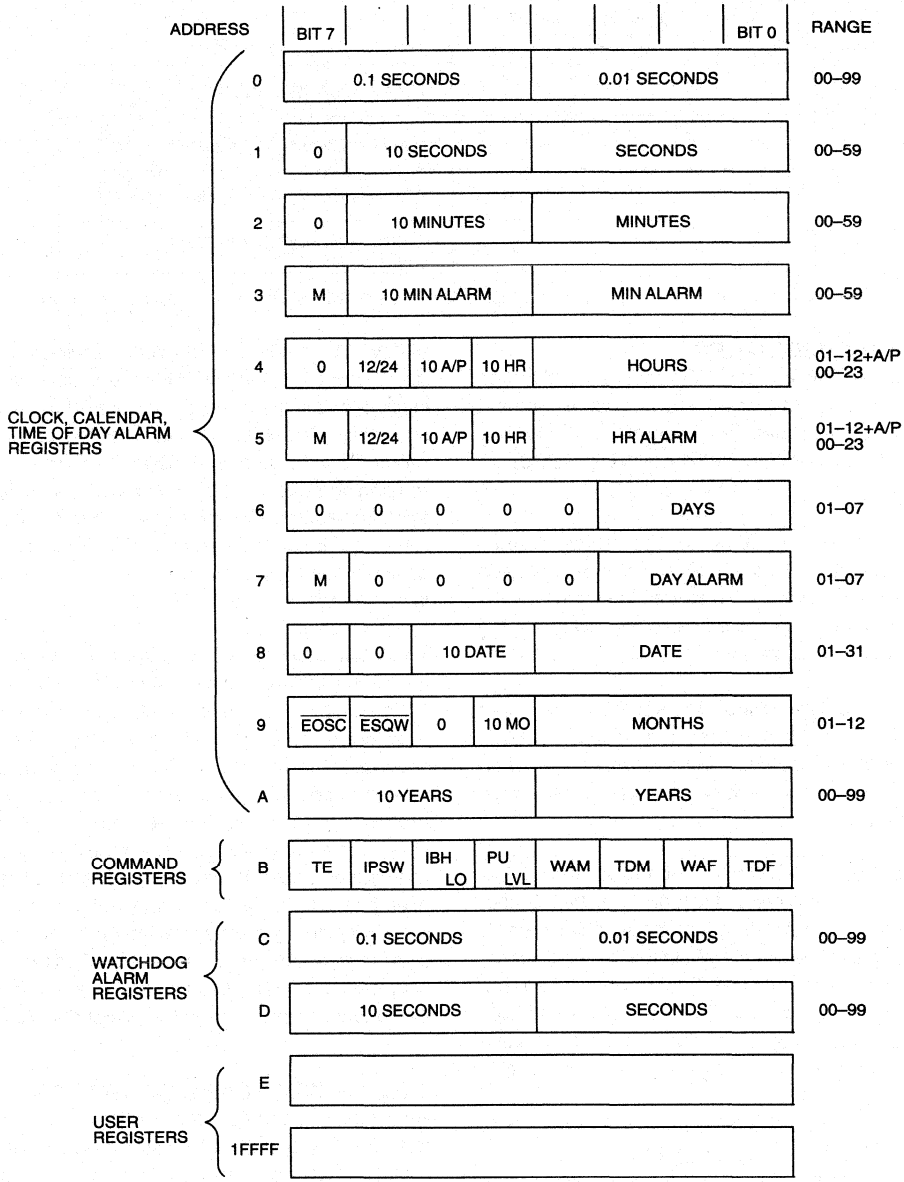
WATCHDOG TIMEKEEPER REGISTERS

The DS1384 Watchdog Timekeeper Controller has 14 internal registers which are eight bits wide and contain all of the Timekeeping, Alarm, Watchdog, Control, and Data information. The Clock, Calendar, Alarm and Watchdog Registers are memory locations which contain external (user accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 50 bytes of RAM registers are accessed from the external address and data bus and reside or overlay external static RAM. Registers 0, 1, 2, 4, 6, 8, 9 and A contain time of day and date information (see Figure 2). Time of day information is stored in BCD. Registers 3, 5, and 7 contain the time of day alarm information. Time of day alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Register C and D are the Watchdog Alarm Registers and information which is stored in these two registers is in BCD. Register 0000EH through register 0003FH are on–chip user bytes and can be used to contain data at the user's discretion.

DS1384 BLOCK DIAGRAM Figure 1



DS1384 WATCHDOG TIMEKEEPER REGISTERS Figure 2



TIME OF DAY ALARM MASK BITS Figure 3

REGISTER			
MINUTES	HOURS	DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

NOTE: ANY OTHER BIT COMBINATIONS OF MASK BIT SETTINGS PRODUCE ILLOGICAL OPERATION.

TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9 and A contain time of day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits.

When set to logical zero, $\overline{EOSC}$ (bit 7) enables the real–time clock oscillator. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level.

Bit 6 of this same byte controls the square wave output (pin 24). When set to logical zero, the square wave output pin will output a 1024 Hz square wave signal. When set to logic one the square wave output pin is in a high impedance state.

Bit 6 of the Hours Register is defined as the 12– or 24–Hour Select Bit. When set to logic one, the 12–hour format is selected. In the 12–hour format, bit 5 is the AM/PM bit with logical one being PM. In the 24–hour mode, bit 5 is the second 10–hour bit (20-23 hours). The time of day registers are updated every 0.01 seconds from the real time clock, except when the TE bit (bit 7 of register B) is set low or the clock oscillator is not running.

The preferred method of synchronizing data access to and from the Watchdog Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable bit) to a logic zero. This will freeze the external time of day registers at the present recorded time allowing access to occur without danger of simultaneous update. When the watch registers have been read or written a second write cycle to location 0B, setting the TE bit to a logic one, will put the time of day registers back to being updated every 0.01 second. No time is lost in the real time clock because the internal copy of the time of day register buffers are continually incremented while the external memory registers are frozen. An alternate method of reading and writing the time of day registers is to ignore synchronization. However, any single read may give erroneous data as the real time clock may be in the process of updating the external memory registers as data is being read.

The internal copies of seconds through years are incremented and Time of Day Alarm is checked during the period that hundreths of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the Watchdog Timekeeper.

TIME OF DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the time of day alarm registers. Bits 3, 4, 5, and 6 of register 7 will always read zero regardless of how they are written. Bit 7 of registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logical zero, a time of day alarm will only occur when registers 2, 4, and 6 match the values stored in registers 3, 5, and 7. An alarm will be generated every day when bit 7 of register 7 is set to a logical one. Similarly, an alarm is generated every hour when bit 7 of registers 7

and 5 is set to a logical 1. When bit 7 of registers 7, 5, and 3 is set to a logical 1, an alarm will occur every minute when register 1 (seconds) rolls from 59 to 00.

Time of day alarm registers are written and read in the same format as the time of day registers. The time of day alarm flag and interrupt is always cleared when alarm registers are read or written.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer Countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from ever going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual count down register is internal and is not readable. Writing registers C and D to zero will disable the Watchdog Alarm feature.

COMMAND REGISTER

Address location 0Bh is the Command Register where mask bits, control bits and flag bits reside. The operation of each bit is as follows:

TE - Bit 7 Transfer enable - This bit when set to a logic 0 will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and reads or writes will not be affected with updates. This bit must be set to a logic 1 to allow updates.

IPSW - Bit 6 Interrupt switch - When set to a logic 1, $\overline{\text{INTA}}$ is the Time of Day Alarm and INTB/($\overline{\text{INTB}}$) is the Watchdog Alarm. When set to logic 0, this bit reverses the output pins. $\overline{\text{INTA}}$ is now the Watchdog Alarm output and INTB/($\overline{\text{INTB}}$) is the Time of Day Alarm output.

IBH/LO - Bit 5 Interrupt B Sink or Source Current - When this bit is set to a logic 1 and V_{CC} is applied, INTB/($\overline{\text{INTB}}$) will source current (see DC characteristics I_{OH}). When this bit is set to a logic 0, INTB will sink current (see DC characteristics I_{OL}).

PU/LVL - Bit 4 Interrupt pulse mode or level mode - This bit determines whether both interrupts will output a pulse or level signal. When set to a logic 0, $\overline{\text{INTA}}$ and INTB/($\overline{\text{INTB}}$) will be in the level mode. When this bit is set to a logic 1, the pulse mode is selected and $\overline{\text{INTA}}$ will sink current for a minimum of 3 ms and then release. INTB/($\overline{\text{INTB}}$) will either sink or source current, depending on the condition of bit 5, for a minimum of 3 ms and then release.

WAM - Bit 3 Watchdog Alarm Mask - When this bit is set to a logic 0, the Watchdog Interrupt output will be activated. The activated state is determined by bits 1,4,5, and 6 of the Command Register. When this bit is set to a logic 1, the Watchdog interrupt output is deactivated.

TDM - Bit 2 Time of Day Alarm Mask - When this bit is set to a logic 0, the Time of Day Alarm Interrupt output will be activated. The activated state is determined by bits 0,4,5, and 6 of the Command Register. When this bit is set to a logic 1 , the Time of Day Alarm interrupt output is deactivated.

WAF - Bit 1 Watchdog Alarm Flag - This bit is set to a logic 1 when a watchdog alarm interrupt occurs. This bit is read only.

The bit is reset when any of the Watchdog Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

TDF - Bit 0 Time of Day Flag - This is a read only bit. This bit is set to a logic 1 when a time of day alarm has occurred. The time the alarm occurred can be determined by reading the Time of Day Alarm registers. This bit is reset to a logic 0 state when any of the Time of Day Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–20°C to +70°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC}+0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	
Battery Input Voltage	V_{BAT}	2.4		4.0	V	

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ tA ≤ 70°C; V_{CC} (max) ≤ V_{CC} ≤ V_{CC} (min))

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		7	15	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH}, CE2 = V_{IL})	I_{CC2}		2	5	mA	2, 3
CMOS Standby Current (CE=V_{CC}-0.2V, CE2=GND+0.2V)	I_{CC3}		1	3	mA	2, 3
Input Leakage Current (any input)	I_{IL}	1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Output Voltage	V_{CCO1}	V_{CC}-0.3			V	4
Output Current	I_{CCO1}			85	mA	4
Write Protection Voltage	V_{PF}	4.0	4.25	4.5	V	5
Output Voltage	V_{CCO2}	V_{BAT}-0.3			V	6
Output Current	I_{CCO2}			100	µA	6
Battery Leakage OSC ON	I_{BAT1}			500	nA	
Battery Leakage OSC OFF	I_{BAT2}			100	nA	
Switch Over Voltage	V_{SO}				V	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	-120		-150		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Address Access Time	t_{ACC}		120		150	ns	
$\overline{CE}$ Access Time	t_{CO}		120		150	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		40		50	ns	
Output Enable Access Time	t_{OE}		60		70	ns	
Output Enable Data Off Time	t_{OEZ}		40		50	ns	
Output Enable to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	10		10		ns	
Output Hold from Address	t_{OH}	5		5		ns	
$\overline{CE}$ to $\overline{CEO}$ Low or High	t_{CEPD}		25		30	ns	
$\overline{OE}$ Low to $\overline{OER}$ Low A0–A16 ≥ 00040h	t_{OERL}		20		25	ns	
$\overline{OE}$ High to $\overline{OER}$ High Time	t_{RO}		20		25	ns	
Address 00040h–1FFFFh to $\overline{OER}$ Low	t_{AOEL}		50		55	ns	
Address 00000h–0003Fh to $\overline{OER}$ High	t_{AOEH}		40		45	ns	
Write Cycle Time	t_{WC}	120		150		ns	
Address Setup Time	t_{AW}	0		0		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	120		150		ns	
Address Hold from End of Write	t_{AH}	10		10		ns	
Write Pulse Width	t_{WP}	80		90		ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		40		50	ns	
$\overline{WE}$ Data Off Time	t_{WEZ}		40		50	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10		10		ns	
Data Setup Time	t_{DS}	45		50		ns	
Data Hold Time High	t_{DH}	0		0		ns	
$\overline{INTA}$ and $\overline{INTB}$ Pulse Width	t_{IPW}	3		3		ms	

AC TEST CONDITIONS

Input Levels: 0V to 3V
Transition Times: 5 ns

CAPACITANCE

(t_A = 25°C)

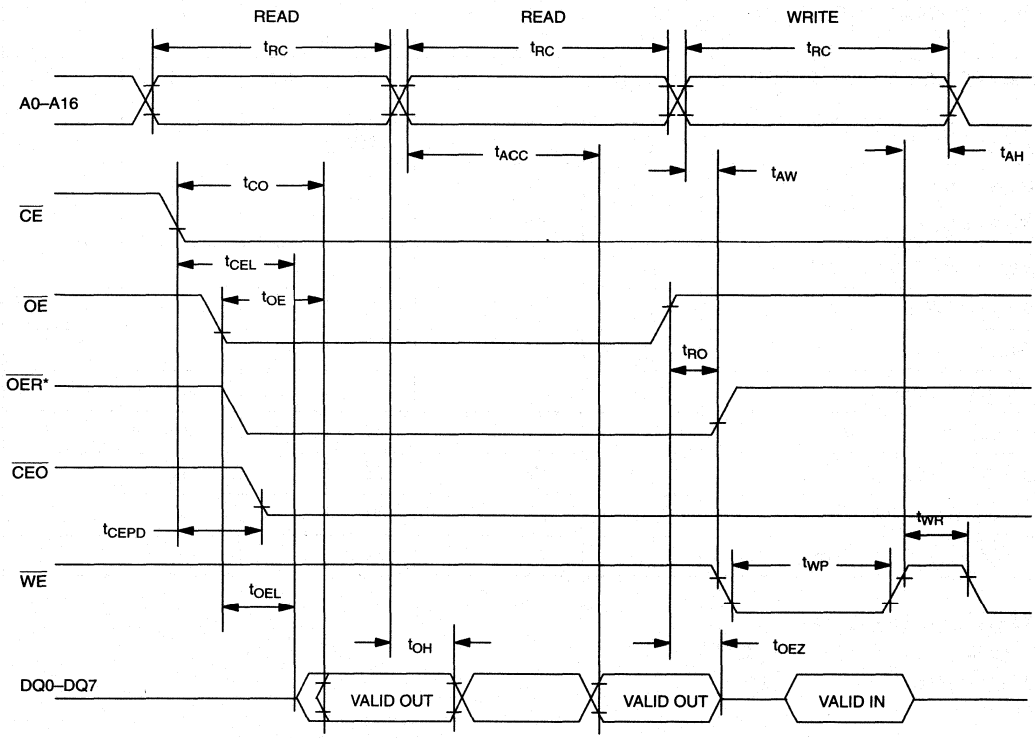
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	C_I		7	15	pF	
Capacitance on DQ pins	C_{DQ}		7	15	pF	

AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING)

(0°C to 70°C)

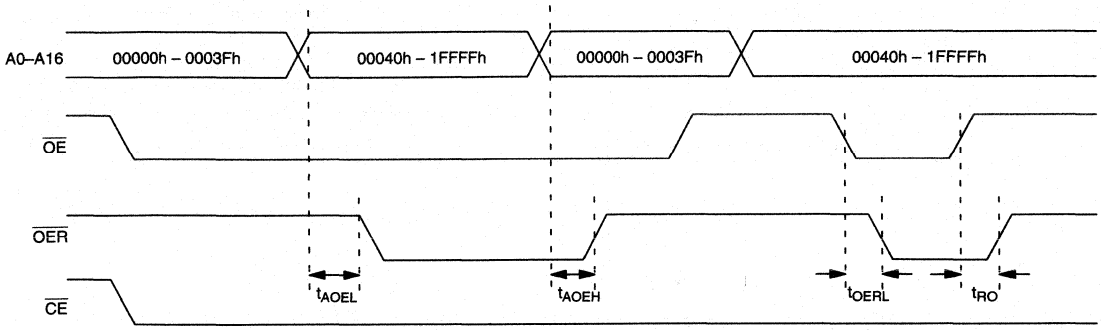
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power Down	t_{PD}	0			µs	
V_{PF} (Max) to V_{PF} (Min) V_{CC} Fall Time	t_F	300			µs	
V_{PF} (Min) to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{PF} (Min) to V_{PF} (Max) V_{CC} Rise Time	t_R	0			µs	
Power Up	t_{REC}	10		150	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	7

READ CYCLE TIMING: RTC AND EXTERNAL SRAM CONTROL SIGNALS



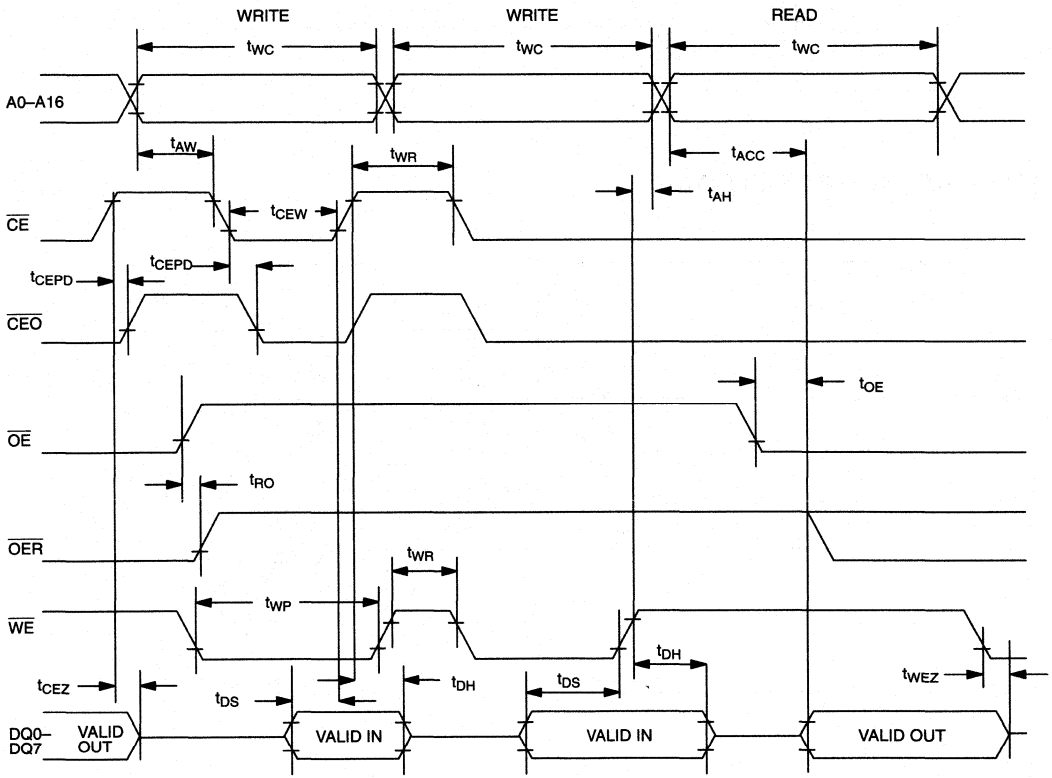
* See the following timing diagram for more specifics on $\overline{OER}$ timing.

$\overline{OER}$ TIMING WHEN SWITHCHING BETWEEN LOWER MEMORY (00000h–0003Fh) AND UPPER MEMORY (00040h–1FFFFh)

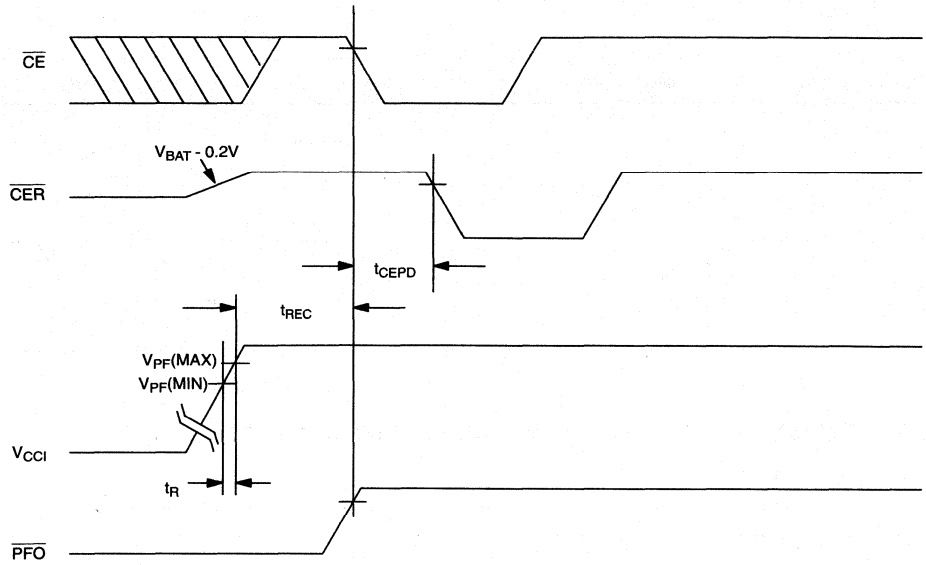


3

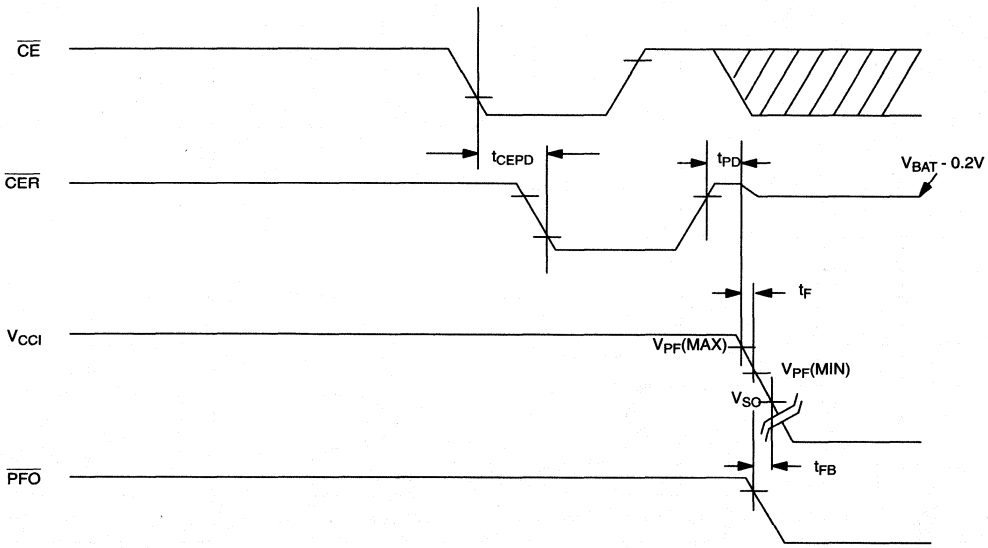
WRITE CYCLE TIMING: RTC AND EXTERNAL SRAM CONTROL SIGNALS



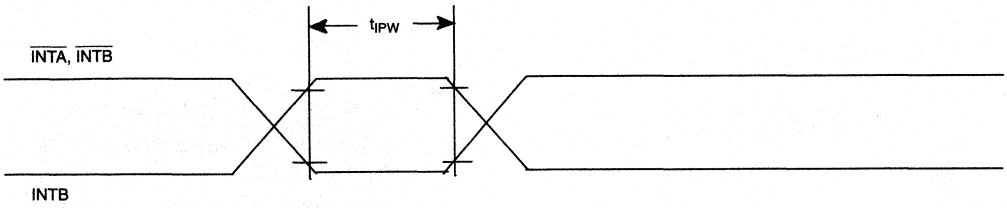
TIMING DIAGRAM: POWER UP



TIMING DIAGRAM: POWER DOWN



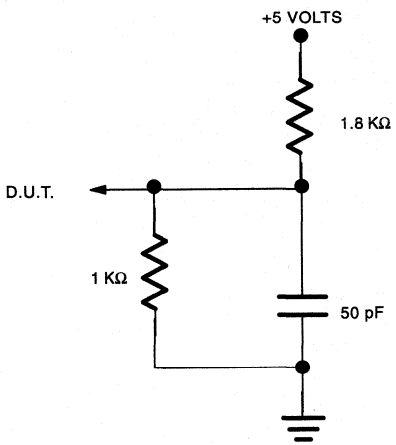
TIMING DIAGRAM: INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 8, 9)



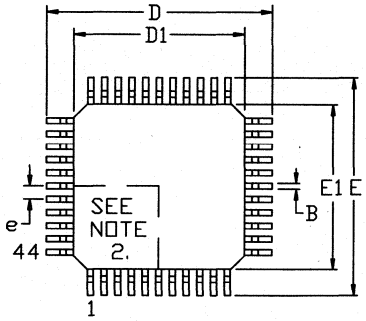
NOTES:

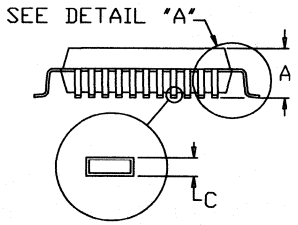
1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Value for voltage and currents is from the V_{CCI} input pin to the V_{CCO} pin.
5. Write protection trip point occurs during power fail prior to switchover from V_{CC} to V_{BAT}.
6. Value for voltage and currents is from the V_{BAT} input pin to the V_{CCO} pin.
7. Data retention time depends on the size of battery selected and the amount of current demanded by the static RAM in back-up mode. The battery capacity (mA • hr) to achieve a T_{DR} of 10 years is given by the formula: $C=(I_{BAT1} + I_{RAM}) \times 24 \times 365 \times 10$, where I_{RAM} is the standby current of the static RAM at the battery voltage. For the DS1384 chip alone, a standard 48 mAh lithium cell battery will provide greater than 10 years of data retention in the absence of power.
8. Applies to both interrupt pins when the alarms are set to pulse.
9. Interrupt output occurs within 100 ns of the alarm condition existing.

OUTPUT LOAD



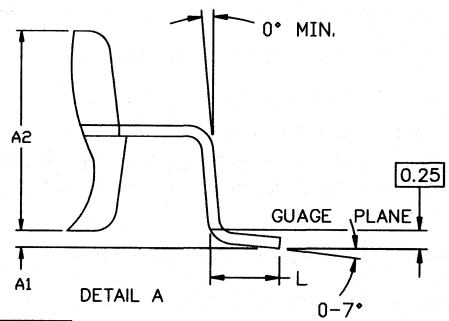
DS1384 AND DS1384T PACKAGE OUTLINES





NOTE:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; AT MAXIMUM MATERIAL CONDITION. PROTRUSIOI NOT TO BE LOCATED ON LOWER RADIUS OF FOOT OF LEAD.
4. CONTROLLING DIMENSIONS: MILLIMETERS.



PKG	DS1384FP		DS1384T	
DIM	MIN	MAX	MIN	MAX
A	–	2.45	–	1.20
A1	0.10	0.30	0.05	0.15
A2	1.95	2.10	0.95	1.05
D	13.65	14.30	11.80	12.20
D1	9.90	10.00	10.00 BSC	
E	13.65	14.30	11.80	12.20
E1	9.90	10.00	10.00 BSC	
L	0.63	1.03	0.45	0.75
e	0.80 BSC		0.80 BSC	
B	0.30	0.45	0.30	0.45
C	0.13	0.23	0.09	0.20

56–G3001–001, 56–G4012–001

DALLAS SEMICONDUCTOR

DS1385/DS1387
RAMified Real Time Clock 4K x 8

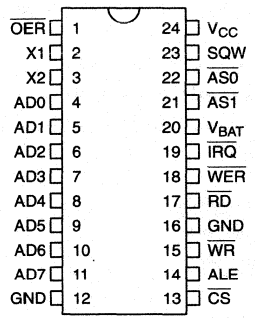
FEATURES

- Upgraded IBM AT computer clock/calendar with 4K x 8 extended RAM
- Totally nonvolatile with over 10 years of operation in the absence of power
- Counts seconds, minutes, hours, day of the week, date, month and year with leap year compensation
- Binary or BCD representations of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Multiplex bus for pin efficiency
- Interfaced with software as 64 user RAM locations plus 4K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
  - 4K x 8 SRAM accessible by using separate control pins
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End-of-clock update cycle
- Available as chip (DS1385 or DS1385S) or stand alone module with embedded lithium battery and crystal (DS1387)

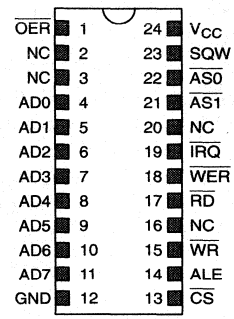
ORDERING INFORMATION

DS1385	RTC Chip; 24–pin DIP
DS1385S	RTC Chip; 28–pin SOIC
DS1387	RTC Module; 24–pin DIP

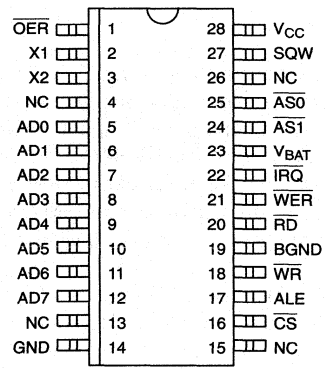
PIN ASSIGNMENT



DS1385 24–PIN DIP
(600 MIL)



DS1387 24–PIN
ENCAPSULATED PACKAGE
(740 MIL FLUSH)



DS1385S 28–PIN SOIC
(330 MIL)

PIN DESCRIPTION

$\overline{OER}$	-	RAM Output Enable
X1	-	Crystal Input
X2	-	Crystal Output
AD0-AD7	-	Mux'ed Address/Data Bus
$\overline{CS}$	-	RTC Chip Select Input
ALE	-	RTC Address Strobe
$\overline{WR}$	-	RTC Write Data Strobe
$\overline{RD}$	-	RTC Read Data Strobe
$\overline{WER}$	-	RAM Write Data Strobe
$\overline{IRQ}$	-	Interrupt Request Output (open drain)
$\overline{AS1}$	-	RAM Upper Address Strobe
$\overline{AS0}$	-	RAM Lower Address Strobe
SQW	-	Square Wave Output
V_{CC}	-	+5V Supply
GND	-	Ground
V_{BAT}	-	Battery + Supply
BGND	-	Battery Ground
NC	-	No Connection

DESCRIPTION

The DS1385/DS1387 RAMified Real Time Clocks (RTCs) are upward-compatible successors to the industry standard DS1285/DS1287 RTC's for PC applications. In addition to the basic DS1285/DS1287 RTC functions, 4K bytes of on-chip nonvolatile RAM have been added.

The RTC functions include a time-of-day clock, a one-hundred year calendar, time-of-day interrupt, periodic interrupts, and an end-of-clock update cycle interrupt. In addition, 50 bytes of user NV RAM are provided within this basic RTC function which can be used to store configuration data. The clock and user RAM are maintained in the absence of system V_{CC} by a lithium battery.

The 4K x 8 additional NV RAM is provided to store a much larger amount of system configuration data than is possible within the original 50 byte area. This RAM is accessed via control signals separate from the RTC, and is also maintained as nonvolatile storage from the lithium battery.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1385/DS1387. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to the energy source connected to the V_{BAT} pin in the case of the DS1385, or to the internal battery in the case of the DS1387. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

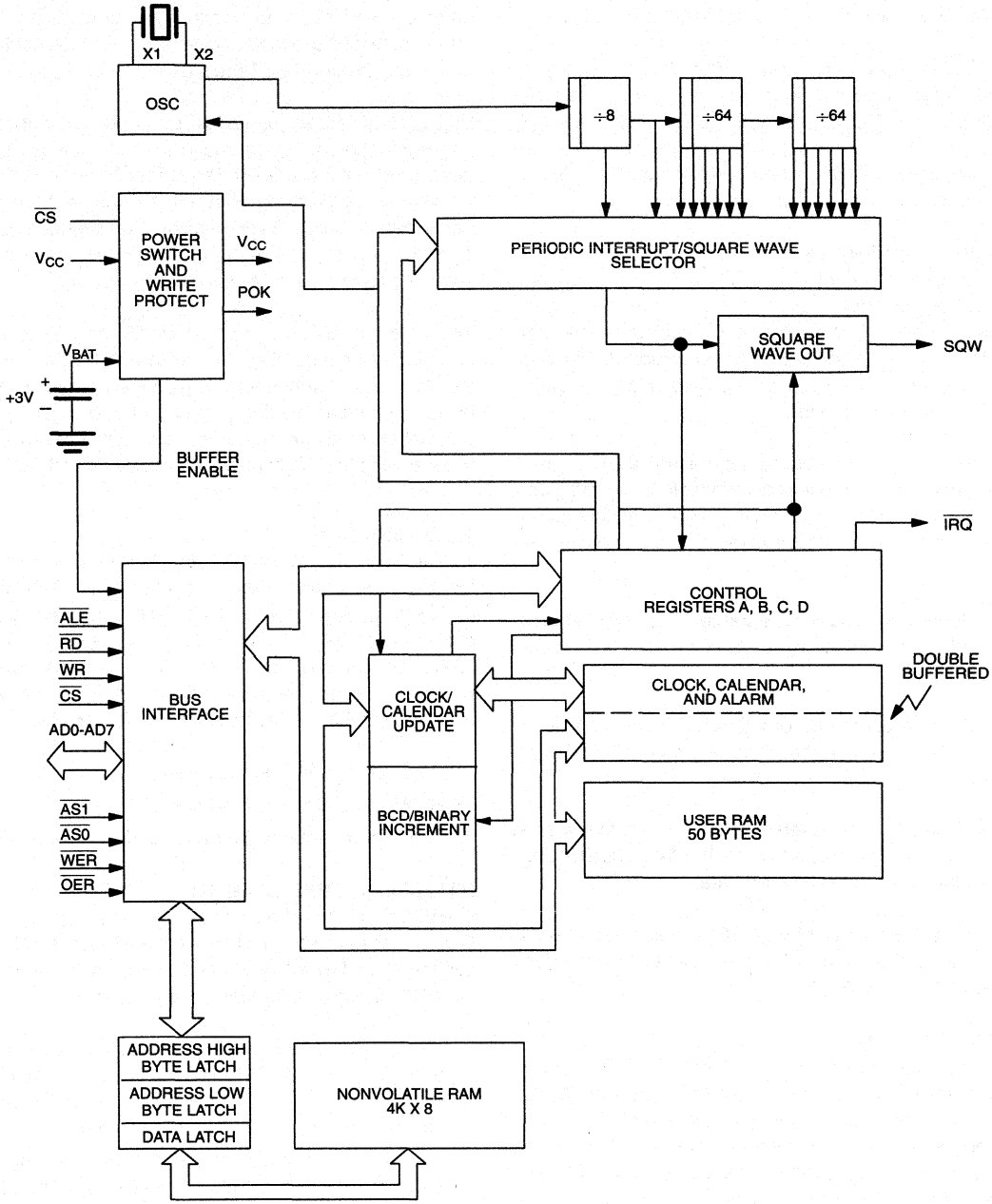
SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1385/DS1387 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, $\overline{AS0}$, or $\overline{AS1}$, at which time the DS1385/DS1387 latches the address from AD0 to AD7. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ or $\overline{WER}$ pulses. In a read cycle, the DS1385/DS1387 outputs 8 bits of data during the latter portion of the $\overline{RD}$ or $\overline{OER}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ or $\overline{OER}$ transitions high.

ALE (RTC Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1385/DS1387.

$\overline{RD}$ (RTC Read Input) - $\overline{RD}$ identifies the time period when the DS1385/DS1387 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

DS1385/DS1387 BLOCK DIAGRAM Figure 1



$\overline{WR}$ (RTC Write Input) -The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed clock register.

$\overline{CS}$ (RTC Chip Select Input) - The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1385/DS1387 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur.

$\overline{IRQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS1385/DS1387 that can be tied to an interrupt input on a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application program normally reads the C register.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

$\overline{AS0}$ (RAM Address Strobe Zero) - The rising edge of $\overline{AS0}$ latches the lower eight bits of the 4K x 8 RAM address.

$\overline{AS1}$ (RAM Address Strobe One) - The rising edge of $\overline{AS1}$ latches the upper four bits of the 4K x 8 RAM address.

$\overline{OER}$ (RAM Output Enable) - $\overline{OER}$ is active low and identifies the time period when the DS1385/DS1387 drives the bus with RAM read data.

$\overline{WER}$ (RAM Write Enable) - $\overline{WER}$ is an active low signal and is used to perform writes to the 4K x 8 RAM portion of the DS1385/DS1387.

(DS1385 ONLY)

X1, X2 - Connections for a standard 32.768 KHz quartz crystal, Daiwa part number DT-26S or equivalent. When ordering, request a load capacitance of 6 pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks".

V_{BAT}, BGND - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage is set by the internal circuitry and is 4.25 volts typical. A maximum load of 1 µA at 25°C and 3.0V on V_{BAT} should in the absence of power be used to size the external energy source.

The battery should be connected directly to the V_{BAT} pin. A diode must not be placed in series with the battery to the V_{BAT} pin. Furthermore, a diode is not necessary because reverse charging current protection circuitry is provided internal to the device and has passed the requirements of Underwriters Laboratories for UL listing.

ADDRESS MAP

The address map of the DS1385/DS1387 is shown in Figure 2. The address map consists of the RTC and the 4K X 8 NV SRAM section. The RTC section contains 50 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

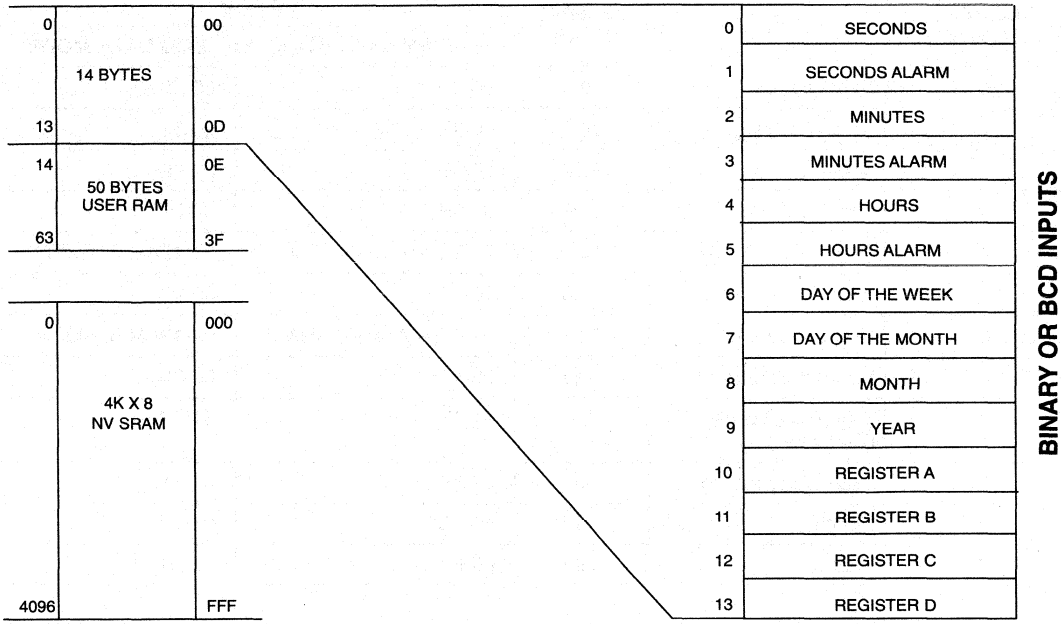
1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

RTC (REAL TIME CLOCK)

The RTC function is the same as the DS1287 Real Time Clock. Access to the RTC is accomplished with four controls: ALE, $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$. The RTC is the same in the DS1287 with the following exceptions:

1. The MOT pin on the DS1285/DS1287 is not present on the DS1385/DS1387. The bus selection capability of the DS1285/DS1287 has been eliminated. Only the Intel bus interface timing is applicable.
2. The $\overline{RESET}$ pin on the DS1285/DS1287 is not present on the DS1385/DS1387. The DS1385/DS1387 will operate the same as the DS1285/DS1287 with $\overline{RESET}$ tied to V_{CC}.

ADDRESS MAP DS1385/DS1387 Figure 2



3

TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second method is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

USER NONVOLATILE RAM - RTC

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1385/DS1387. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1287. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS1385/DS1387 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 KHz
0	1	0	0	244.141 µs	4.096 KHz
0	1	0	1	488.281 µs	2.048 KHz
0	1	1	0	976.5625 µs	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

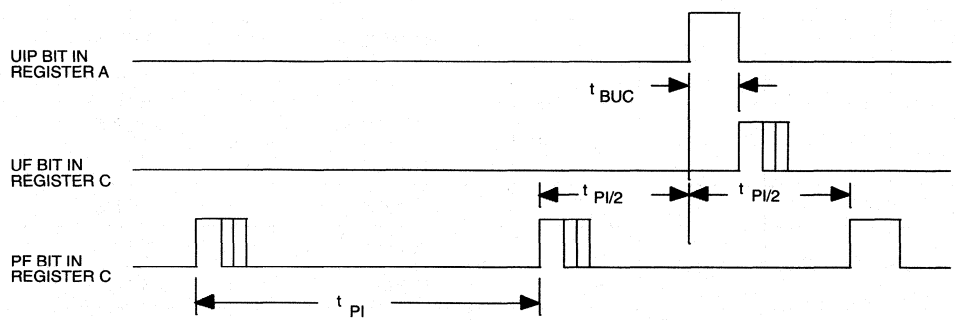
The DS1385/DS1387 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($t_{PI}/2+t_{BUC}$) to ensure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS1385/DS1387 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1385/DS1387.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1385/DS1387 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1385/DS1387 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do

not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1
i.e., IRQF = (PF • PIE) + (AF • ALE) + (UF • UIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 0 THROUGH BIT 3 - These are reserved bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.

4K X 8 RAM

The DS1385/DS1387 provides 4K x 8 of on-chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by the internal power OK signal (POK) generated from the write protect circuitry. The POK signal becomes active at 4.25 volts (typical).

The on-chip 4K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7-AD0. Access to the SRAM is controlled by three on-chip latch registers. Two registers are used to hold the SRAM address, and the third register is used to hold read/write data. The SRAM address space is from 000H to FFFH.

Four control signals, $\overline{AS0}$, $\overline{AS1}$, $\overline{OER}$, and $\overline{WER}$, are used to access the 4K x 8 SRAM. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ($\overline{AS0}$) and Address Strobe 1 (AS1) signals. $\overline{AS0}$ is used to latch the lower 8-bits of address, and $\overline{AS1}$ is used to latch the upper 4-bits of address. It is necessary to meet the setup and hold times given in the Electrical Specifications with valid address information in order to properly latch the address. If the upper or lower order address is correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation requires valid data to be placed on the bus (AD7-AD0) followed by the activation of the Write Enable RAM ($\overline{WER}$) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Output Enable RAM ($\overline{OER}$) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met. The $\overline{WER}$ and $\overline{OER}$ signals should never be active at the same time. In addition, access to the clock/calendar registers and user RAM (via $\overline{CS}$) must not be attempted when the 4K x 8 RAM is being accessed. The RAM is enabled when either $\overline{WER}$ or $\overline{OER}$ is active. $\overline{CS}$ is only used for the access of the clock calendar registers (including the extended Dallas registers) and the 50 bytes of user RAM.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	DS1387: -40°C to +70°C DS1385: –55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	9

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

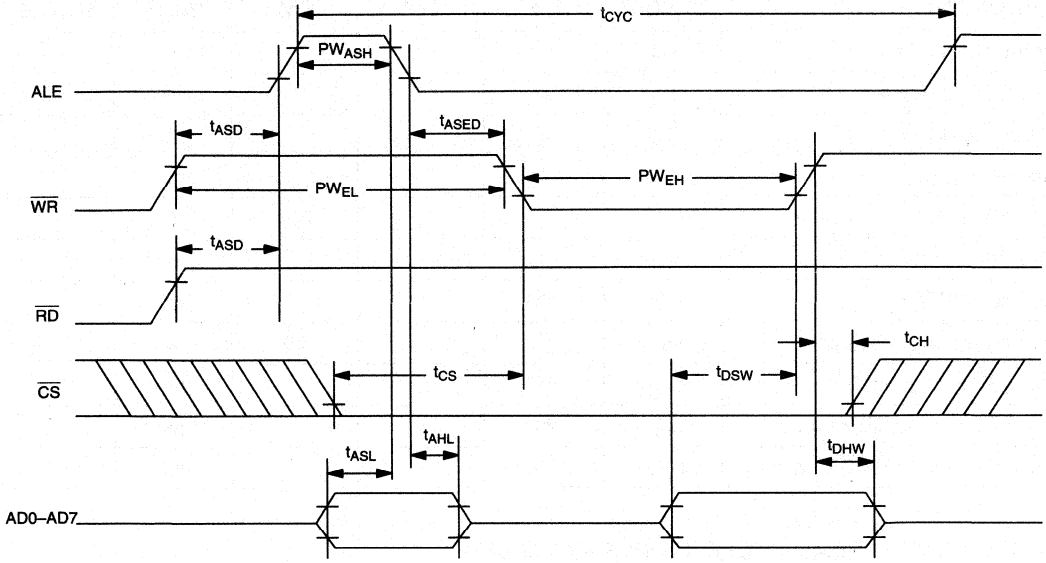
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		35	50	mA	2
Standby Current $\overline{CS}$, $\overline{OER}$, and $\overline{WER}$ = V_{CC} -0.3V	I_{CC2}		1	5.0	mA	6
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	3
Output @ 2.4V	I_{OH}	-1.0			mA	1,4
Output @ 0.4V	I_{OL}			2.0	mA	1

RTC AC TIMING CHARACTERISTICS

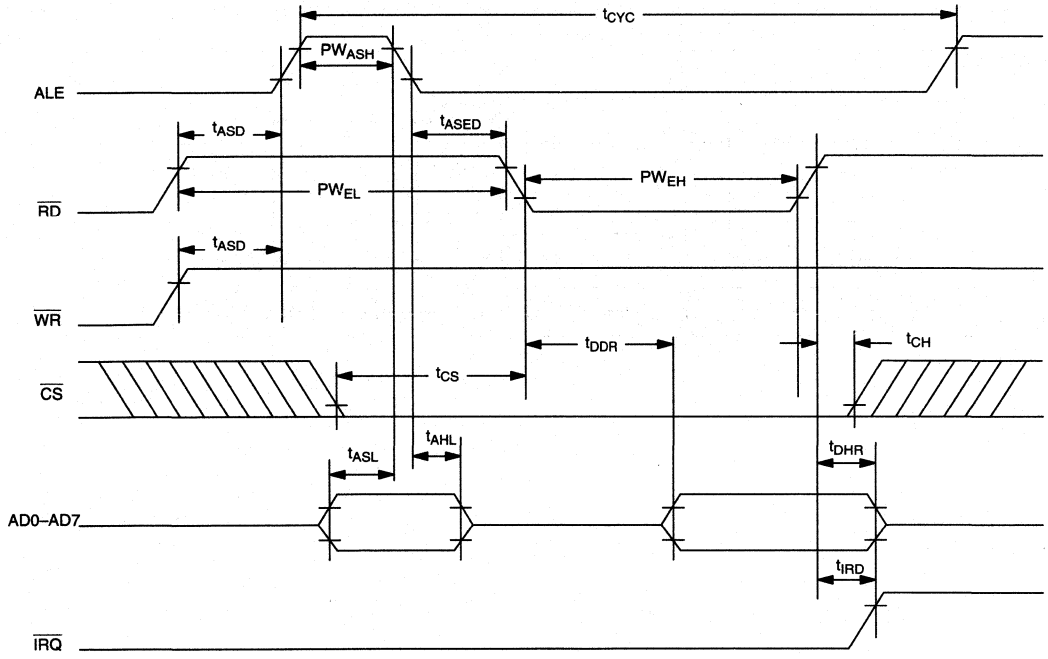
(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}/\overline{WR}$ Low	PW_{EH}	125			ns	
Pulse Width, $\overline{RD}/\overline{WR}$ High	PW_{EL}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	5
Data Setup Time to Write	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

DS1385/DS1387 BUS TIMING FOR WRITE CYCLE TO RTC



DS1385/DS1387 BUS TIMING FOR READ CYCLE TO RTC

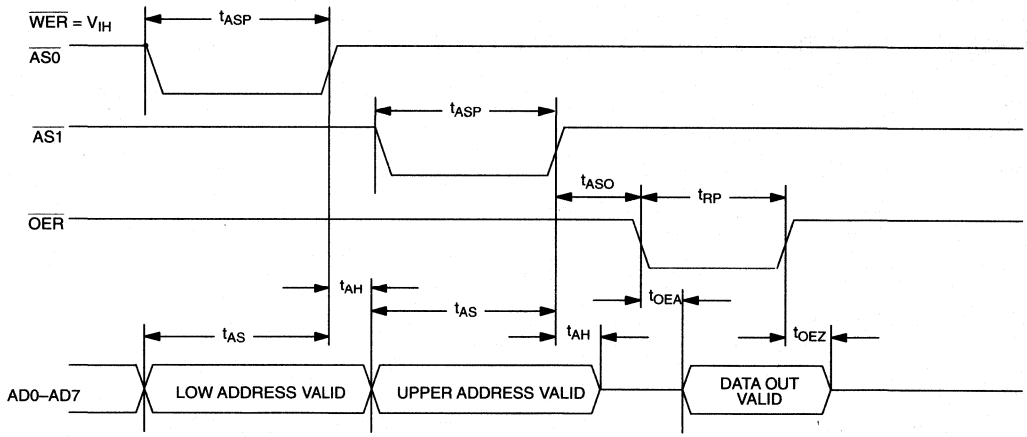


4K X 8 AC TIMING CHARACTERISTICS

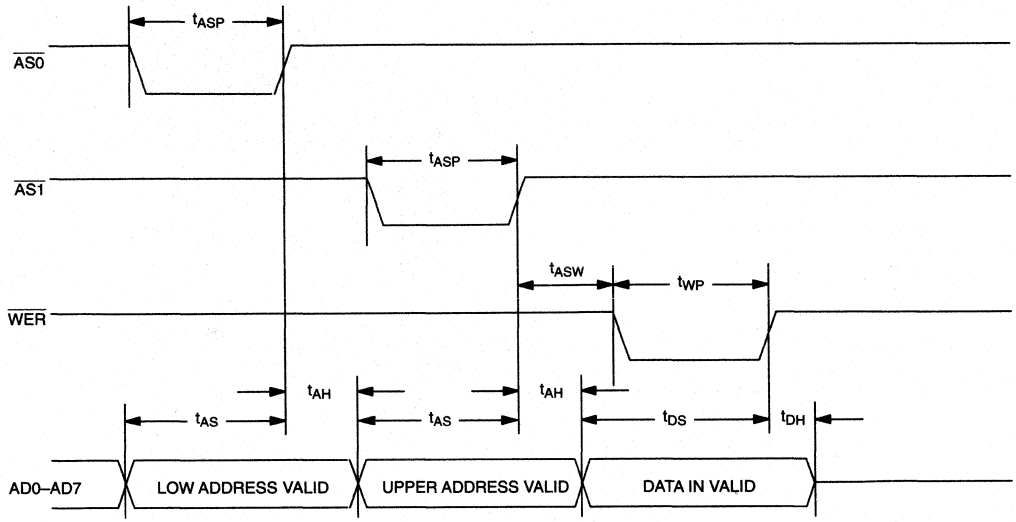
(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	50			ns	
Address Hold Time	t_{AH}	0			ns	
Data Setup Time	t_{DS}	75			ns	
Data Hold Time	t_{DH}	0			ns	
Output Enable Access Time	t_{OEA}			200	ns	7
Write Pulse Width	t_{WP}	200			ns	
$\overline{OER}$ Pulse Width	t_{RP}	200			ns	
$\overline{OER}$ to Output in High Z	t_{OEZ}			50	ns	
$\overline{AS0}$, $\overline{AS1}$ Pulse Width	t_{ASP}	75			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{OER}$ Low	t_{ASO}	20			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{WER}$ Low	t_{ASW}	20			ns	

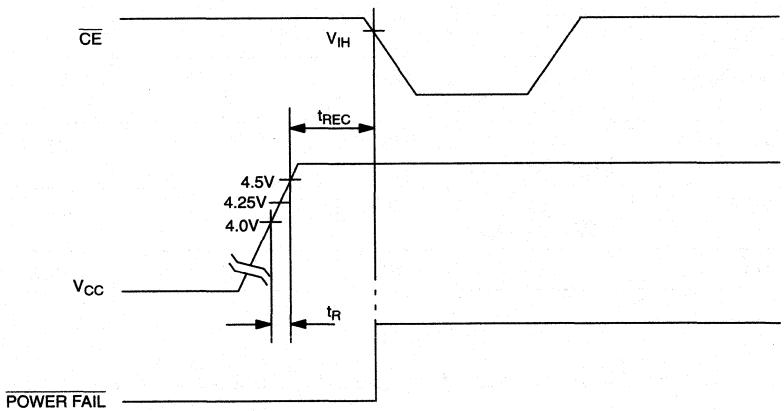
BUS TIMING FOR READ CYCLE TO 4K X 8 NV SRAM



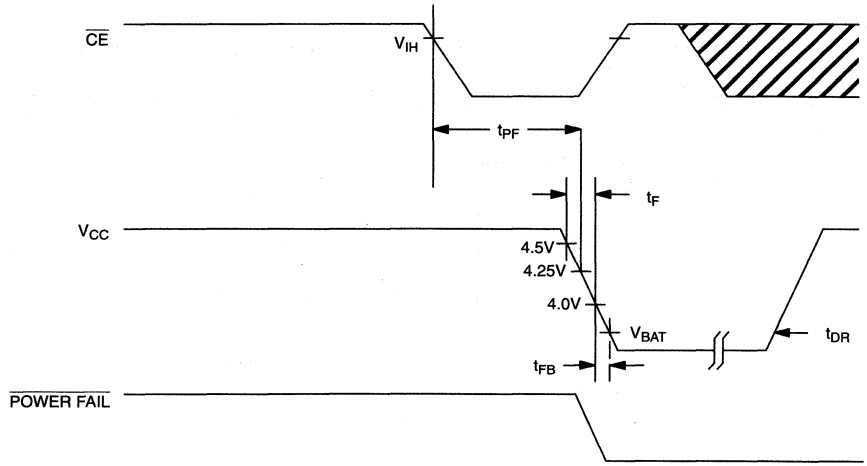
BUS TIMING FOR WRITE CYCLE TO 4K X 8 SRAM



POWER-UP CONDITION



POWER-DOWN CONDITION



POWER-UP POWER-DOWN TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	8

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

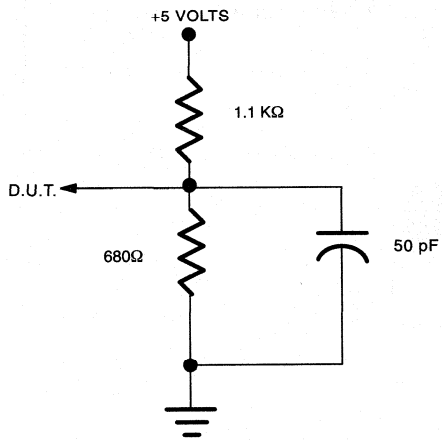
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

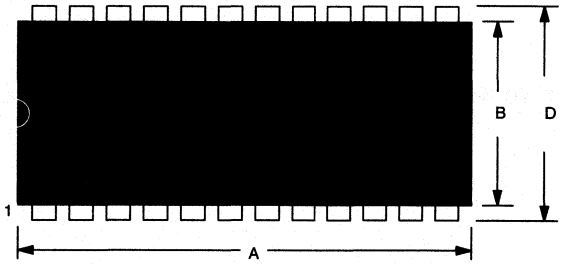
NOTES:

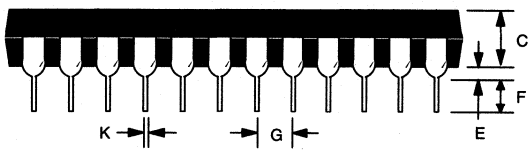
1. All voltages are referenced to ground.
2. All outputs are open.
3. Applies to the AD0-AD7 pins, and the SQW pin when each is in the high impedance state.
4. The $\overline{IRQ}$ pin is open drain.
5. Measured with a load as shown in Figure 4.
6. All other inputs at CMOS levels.
7. Measured with a load as shown in Figure 4.
8. The real-time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
9. Applies to DS1385 and DS1385S only.

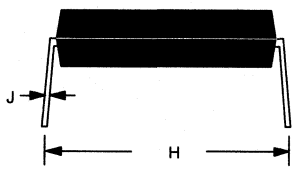
OUTPUT LOAD Figure 4



DS1385 24–PIN DIP

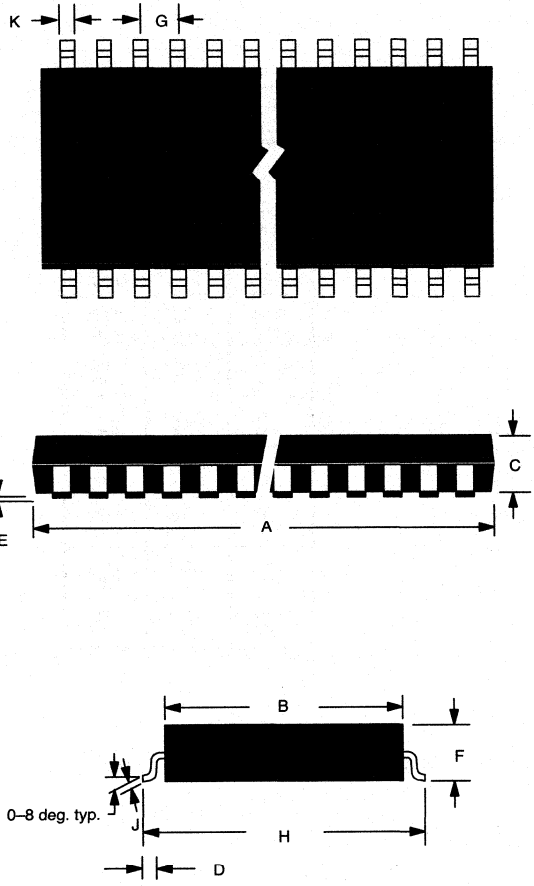






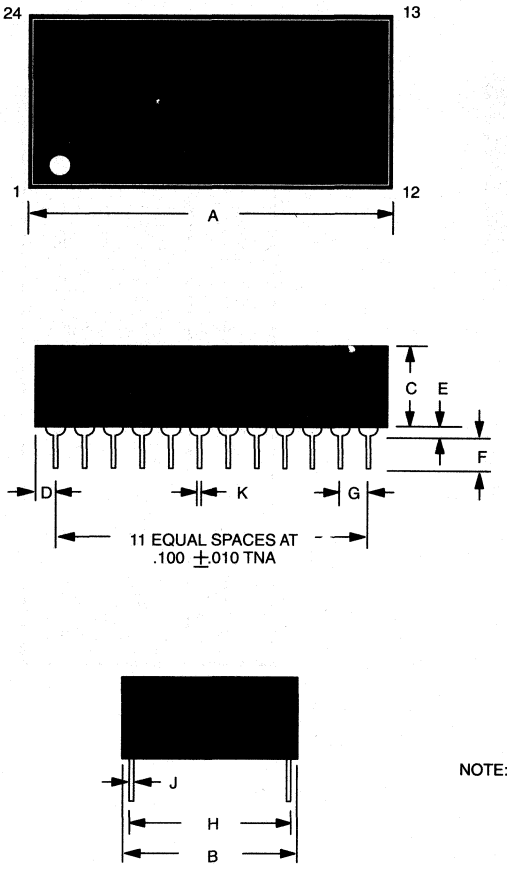
PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.245 31.62	1.270 32.26
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.38	0.050 1.27
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.625 15.88	0.675 17.15
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

DS1385S 28–PIN SOIC



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480 12.19
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51

DS1387 24–PIN 740 MIL FLUSH ENCAPSULATED



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN.	1.320	1.335
MM	33.53	33.91
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.345	0.370
MM	8.76	9.40
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.89
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

DS1386
RAMified Watchdog Timekeeper

3

FEATURES

- 8K or 32K bytes of user NV RAM
- Real time quartz clock/calendar keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Will operate in 28-pin JEDEC footprint when lower justified
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities such as system wakeup
- Embedded lithium energy cell maintains time, watchdog, user RAM, and alarm information
- Programmable interrupts and square wave output
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25°C
- Greater than 10 years of timekeeping in the absence of V_{CC}
- Interrupt signals are active in power-down mode

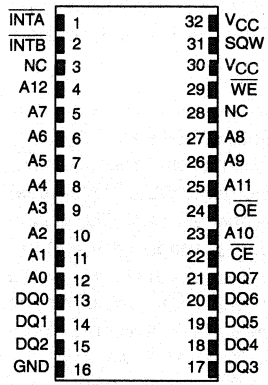
ORDERING INFORMATION

DS1386 XX–XX RTC and NVSRAM; 32 pin DIP

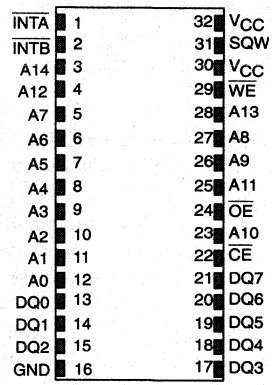
–15 150 ns access
–12 120 ns access

08 8K x 8 NVSRAM
32 32K x 8 NVSRAM

PIN ASSIGNMENT



DS1386 8K x 8
32-Pin Encapsulated Package



DS1386 32K x 8
32-Pin Encapsulated Package

PIN DESCRIPTION

$\overline{INTA}$	-	Interrupt Output A (open drain)
$\overline{INTB}$(INTB)	-	Interrupt Output B (open drain)
A0-A14	-	Address Inputs
DQ0-DQ7	-	Data Input/Output
$\overline{CE}$	-	Chip Enable
$\overline{OE}$	-	Output Enable
$\overline{WE}$	-	Write Enable
V_{CC}	-	+5 Volts
GND	-	Ground
SQW	-	Square Wave Output
NC	-	No Connection

DESCRIPTION

The DS1386 RAMified Watchdog Timekeeper is a self-contained real time clock (RTC), alarm, watchdog timer, and interval timer in a 32-pin JEDEC DIP package. The DS1386 contains an embedded lithium energy source and a quartz crystal which eliminates the need for any external circuitry. Data contained within 8K or 32K by 8-bit memory and the timekeeping registers can be read or written in the same manner as bytewide static RAM. The timekeeping registers are located in the first 14 bytes of memory space. Data is maintained in the RAMified Timekeeper by intelligent control circuitry which detects the status of V_{CC} and write protects memory when V_{CC} is out of tolerance. The lithium energy source can maintain data and real time for over ten

years in the absence of V_{CC}. Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The RAMified Timekeeper operates in either 24 hour or 12 hour format with an AM/PM indicator. The watchdog timer provides alarm interrupts and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week. Interrupts for both watchdog and RTC will operate when system is powered down. Either can provide system "wake-up" signals.

OPERATION - READ REGISTERS

The DS1386 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (High) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (Low). The unique address specified by the address inputs (A0-A14) defines which of the registers is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE REGISTERS

The DS1386 is in the write mode whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set-Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (High) during write cycles to avoid bus contention . However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

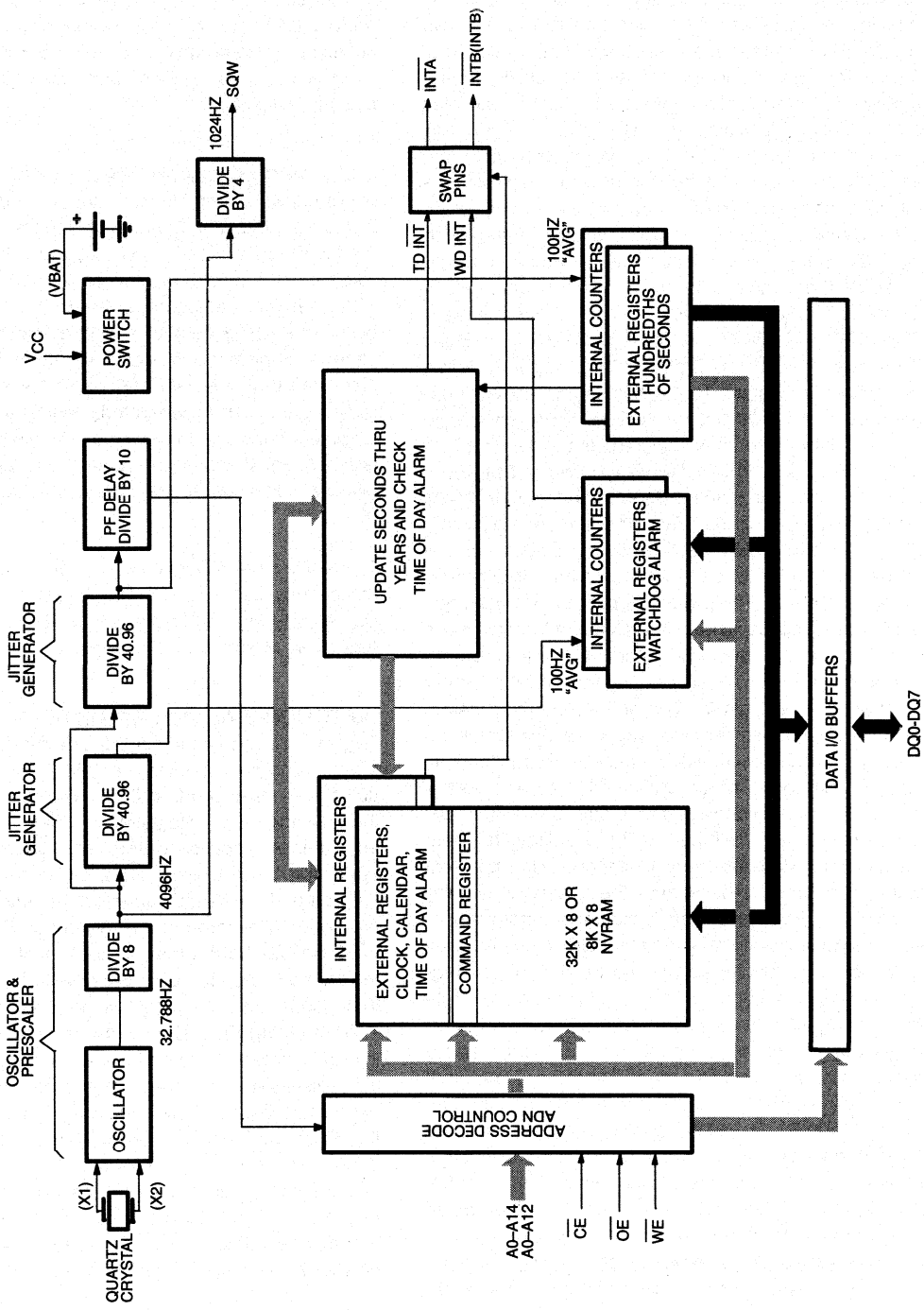
DATA RETENTION

The RAMified Timekeeper provides full functional capability when V_{CC} is greater than 4.5 volts and write-protects the register contents at 4.25 volts typical. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1386 constantly monitors V_{CC}. Should the supply voltage decay, the RAMified Timekeeper will automatically write-protect itself and all inputs to the registers become "don't care". The two interrupts $\overline{INTA}$ and $\overline{INTB}$ (INTB) and the internal clock and timers continue to run regardless of the level of V_{CC}. However, it is important to insure that the pull–up resistors used with the interrupt pins are never pulled up to a value that is greater than V_{CC} + 0.3V. As V_{CC} falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} and disconnects the internal lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for a period of 200 ms.

RAMIFIED TIMEKEEPER REGISTERS

The RAMified Timekeeper has 14 registers which are eight bits wide that contain all of the timekeeping, alarm, watchdog and control information. The clock, calendar, alarm, and watchdog registers are memory locations which contain external (user-accessible) copies of the timekeeping data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 8K or 32K bytes of RAM and the 14 external timekeeping registers are accessed from the external address and data bus. Register 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm Registers and information which is stored in these two registers is in BCD. Registers E through 1FFF or 7FFF are user bytes and can be used to maintain data at the user's discretion.

BLOCK DIAGRAM Figure 1



TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic 0, $\overline{EOSC}$ (Bit 7) enables the Real Time Clock oscillator. This bit is set to logic 1 as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the Square Wave Output (pin 31). When set to logic 0, the Square Wave Output Pin will output a 1024 Hz Square Wave Signal. When set to logic 1 the Square Wave Output Pin is in a high impedance state. Bit 6 of the Hours Register is defined as the 12 or 24 Hour Select Bit. When set to logic 1, the 12 Hour Format is selected. In the 12 Hour Format, bit 5 is the AM/PM bit with logic 1 being PM. In the 24 Hour Mode, bit 5 is the Second 10 Hour bit (20-23 hours). The Time of Day Registers are updated every .01 seconds from the Real Time Clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the RAMified Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable bit) to a logic 0. This will freeze the External Time of Day Registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic 1, will put the Time of Day Registers back to being updated every .01 second. No time is lost in the Real Time Clock because the internal copy of the Time of Day Register buffers is continually incremented while the external memory registers are frozen. An alternate method of reading and writing the Time of Day Registers is to ignore synchronization. However, any single read may give erroneous data as the Real Time Clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented, and the Time of Day Alarm is checked during the period that hundreds of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the RAMified Timekeeper.

TIME OF DAY ALARM REGISTERS

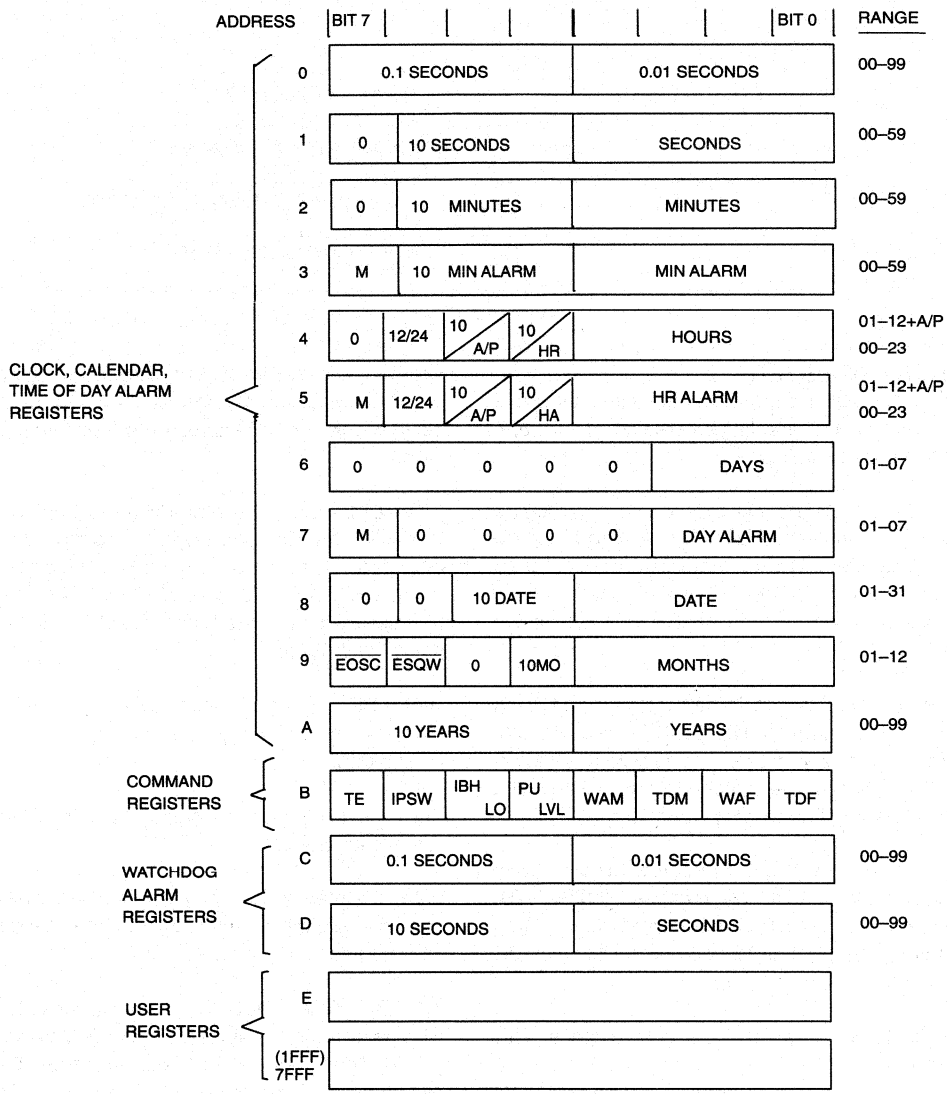
Registers 3, 5, and 7 contain the Time of Day Alarm Registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logic 0, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic 1. Similarly, an alarm is generated every hour when bit 7 of Registers 7 and 5 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm Registers are written and read in the same format as the Time of Day Registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm Registers are read or written.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer Countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual count- down register is internal and is not readable. Writing registers C and D to zero will disable the Watchdog Alarm feature.

DS1386 RAMIFIED WATCHDOG TIMEKEEPER REGISTERS Figure 2



TIME OF DAY ALARM MASK BITS Figure 3

REGISTER			
(3)MINUTES	(5)HOURS	(7)DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

NOTE: ANY OTHER BIT COMBINATIONS OF MASK BIT SETTINGS PRODUCE ILLOGICAL OPERATION.

COMMAND REGISTER

Address location 0Bh is the Command Register where mask bits, control bits and flag bits reside. The operation of each bit is as follows:

TE - Bit 7 Transfer enable - This bit when set to a logic 0 will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and reads or writes will not be affected with updates. This bit must be set to a logic 1 to allow updates.

IPSW - Bit 6 Interrupt switch - When set to a logic 1, $\overline{INTA}$ is the Time of Day Alarm and INTB/($\overline{INTB}$) is the Watchdog Alarm. When set to logic 0, this bit reverses the output pins. $\overline{INTA}$ is now the Watchdog Alarm output and INTB/($\overline{INTB}$) is the Time of Day Alarm output.

IBH/LO - Bit 5 Interrupt B Sink or Source Current - When this bit is set to a logic 1 and V_{CC} is applied, INTB/($\overline{INTB}$) will source current (see DC characteristics IOH). When this bit is set to a logic 0, INTB will sink current (see DC characteristics IOL).

PU/LVL - Bit 4 Interrupt pulse mode or level mode - This bit determines whether both interrupts will output a pulse or level signal. When set to a logic 0, $\overline{INTA}$ and INTB/($\overline{INTB}$) will be in the level mode. When this bit is set to a logic 1, the pulse mode is selected and $\overline{INTA}$ will sink current for a minimum of 3 ms and then release. INTB/($\overline{INTB}$) will either sink or source current, depending on the condition of Bit 5, for a minimum of 3 ms and then release.

WAM - Bit 3 Watchdog Alarm Mask - When this bit is set to a logic 0, the Watchdog Interrupt output will be activated. The activated state is determined by bits 1,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Watchdog interrupt output is deactivated.

TDM - Bit 2 Time of Day Alarm Mask - When this bit is set to a logic 0, the Time of Day Alarm Interrupt output will be activated. The activated state is determined by bits 0,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1 , the Time of Day Alarm interrupt output is deactivated.

WAF - Bit 1 Watchdog Alarm Flag - This bit is set to a logic 1 when a watchdog alarm interrupt occurs. This bit is read only.

The bit is reset when any of the Watchdog Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

TDF - Bit 0 Time of Day Flag - This is a read only bit. This bit is set to a logic 1 when a Time of Day alarm has occurred. The time the alarm occurred can be determined by reading the Time of Day Alarm registers. This bit is reset to a logic 0 state when any of the Time of Day Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	10
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	10
Input Logic 0	V_{IL}	-0.3		+0.8	V	10

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
Output Leakage Current	I_{LO}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LIO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}			2.1	mA	13
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE}$ = V_{CC} -0.5	I_{CCS2}		2.0	4.0	mA	
Active Current	I_{CC}			85	mA	
Write Protection Voltage	V_{TP}		4.25		V	

CAPACITANCE

(t_A = 25°C)

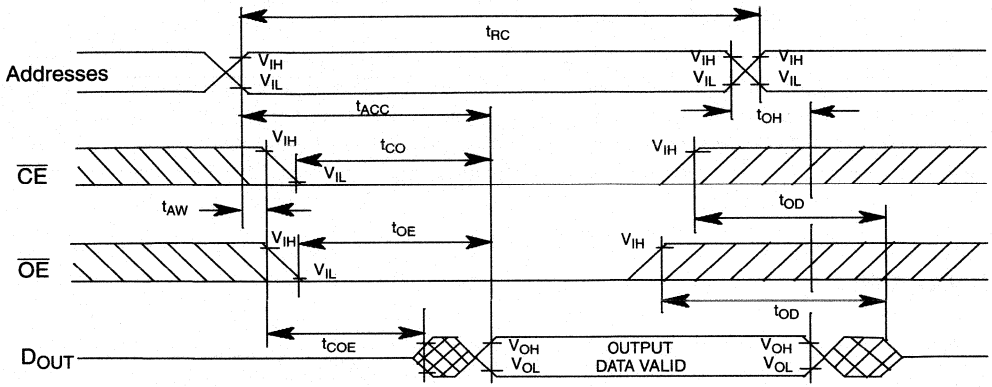
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		7	15	pF	
Output Capacitance	C_{OUT}		7	15	pF	
Input/Output Capacitance	$C_{I/O}$		7	15	pF	

AC ELECTRICAL CHARACTERISTICS

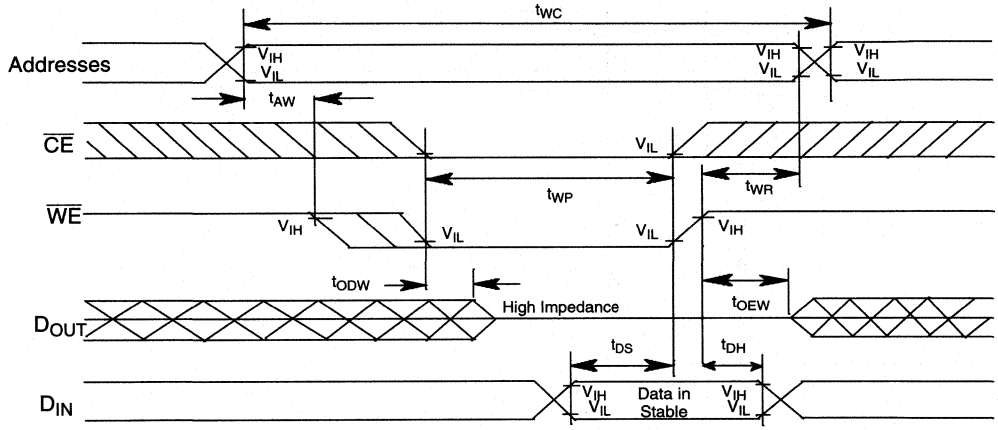
(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	DS1386XX–12		DS1386XX–15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	1
Address Access Time	t_{ACC}		120		150	ns	
$\overline{CE}$ Access Time	t_{CO}		120		150	ns	
$\overline{OE}$ Access Time	t_{OE}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10		10		ns	
Output High Z from Deselect	t_{OD}		40		50	ns	
Output Hold from Address Change	t_{OH}	10		10		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Write Pulse Width	t_{WP}	110		140		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	10		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		40		50	ns	
Output Active from $\overline{WE}$	t_{OEW}	10		10		ns	
Data Setup Time	t_{DS}	85		110		ns	4
Data Hold Time	t_{DH}	10		15		ns	4,5
$\overline{INTA}$, $\overline{INTB}$ Pulse Width	t_{IPW}	3		3		ms	11,12

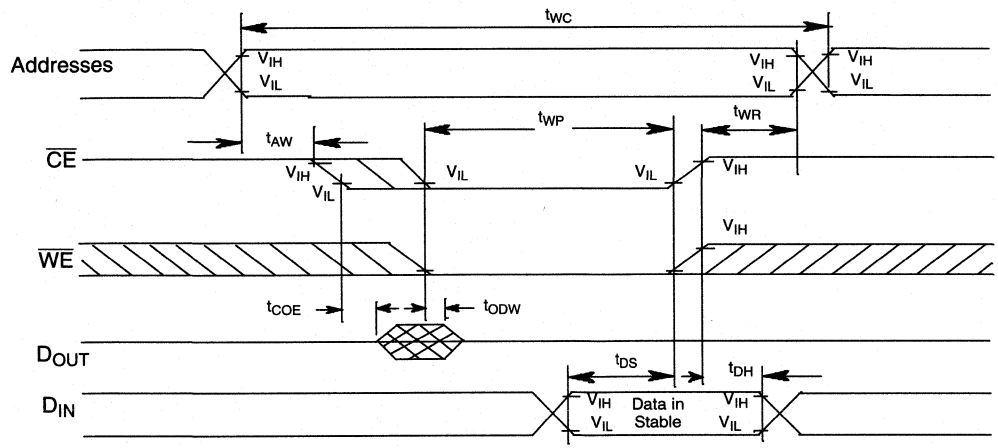
READ CYCLE (Note1)



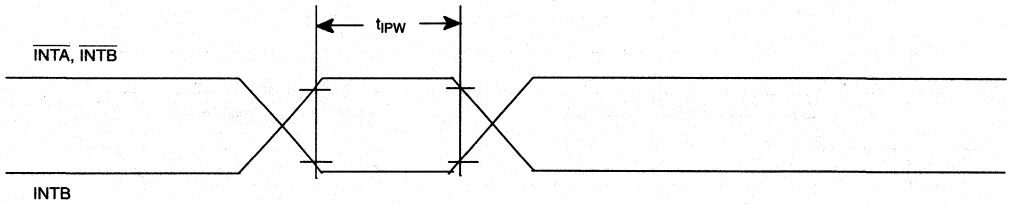
WRITE CYCLE 1 (Notes 2, 6, 7)



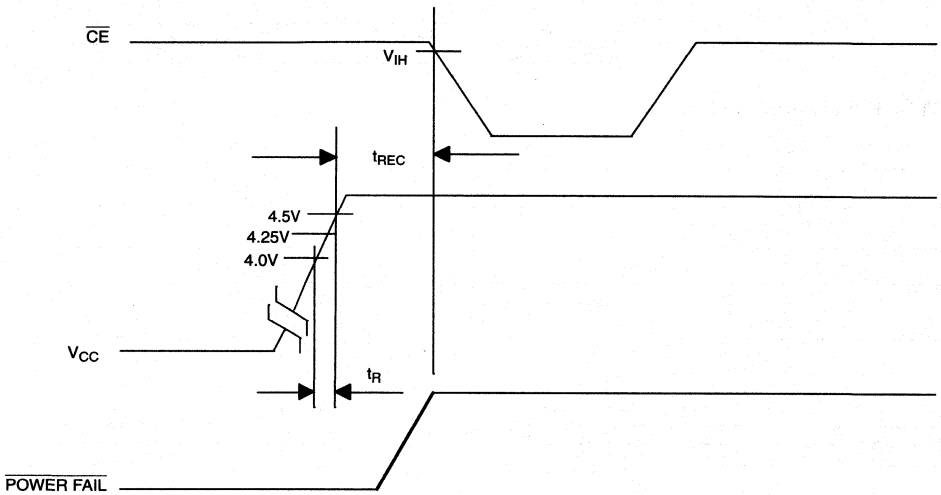
WRITE CYCLE 2 (Notes 2, 8)



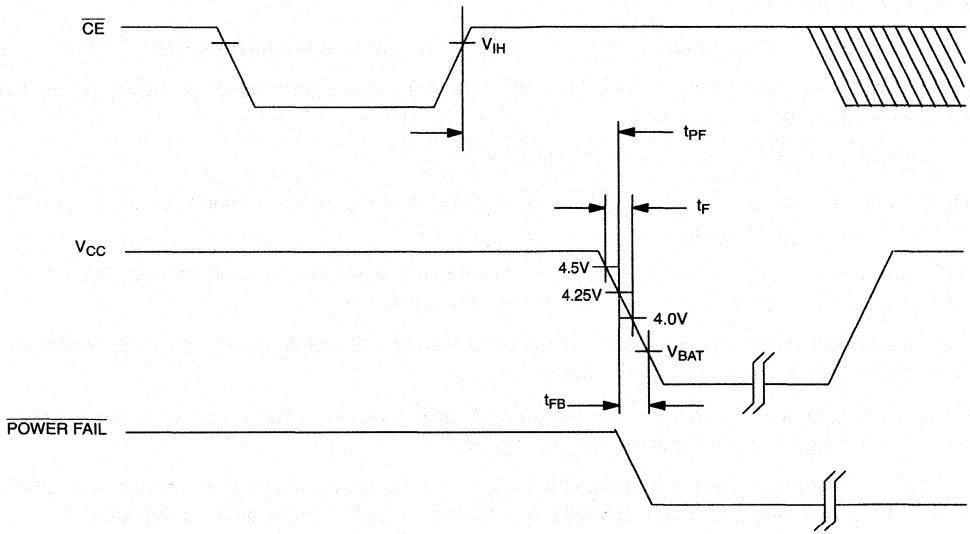
TIMING DIAGRAM: INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11 AND 12)



POWER-UP CONDITION



POWER-DOWN CONDITION



AC ELECTRICAL CHARACTERISTICS POWER-UP POWER-DOWN TIMING (0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}		0	ns	
Recovery at Power Up	t_{REC}		200	ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300		µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.25V$	10		µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0		µs	
Expected Data Retention	t_{DR}	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of the $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} or t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle, then t_{DH} = 20 ns for –12 parts and t_{DH} = 25 ns for –15 parts.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1386 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All voltages are referenced to ground.
11. Applies to both interrupt pins when the alarms are set to pulse.
12. Interrupt output occurs within 100 ns on the alarm condition existing.
13. Both $\overline{INTA}$ and $\overline{INTB}$(INTB) are open drain outputs.

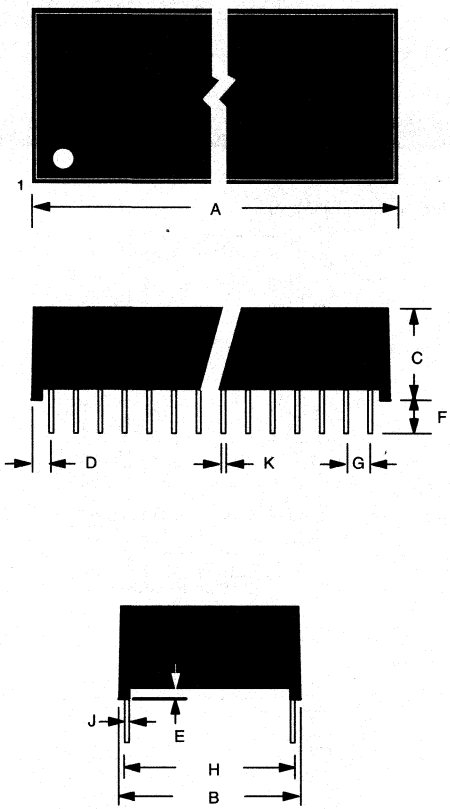
AC TEST CONDITIONS

Input Levels:	0V to 3V
Transition Times:	5 ns

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns.

DS1386 32 PIN 740 MIL MODULE



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.720	1.740
MM	43.69	44.20
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.090	0.120
MM	2.29	3.05
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

3

DALLAS SEMICONDUCTOR

DS14285/DS14287
Real Time Clock with NVRAM Control

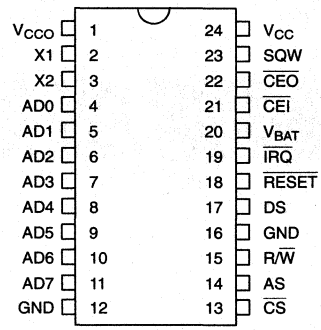
FEATURES

- Direct replacement for IBM AT computer clock/calendar
- Functionally compatible with the DS1285/DS1287
- Available as chip (DS14285, DS14285S, or DS14285Q) or stand–alone module with embedded lithium battery and cyrstal (DS14287)
- Automatic backup supply and write protection to make external SRAM nonvolatile
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End of clock update cycle

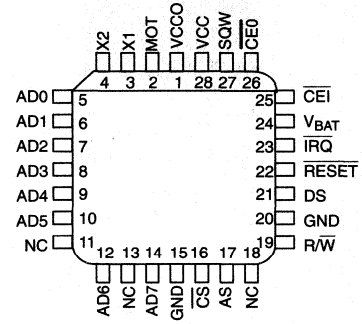
ORDERING INFORMATION

DS14285	RTC Chip; 24–pin DIP
DS14285S	RTC Chip; 24–pin SOIC
DS14285Q	RTC Chip; 28–pin PLCC
DS14287	RTC Module; 24–pin DIP

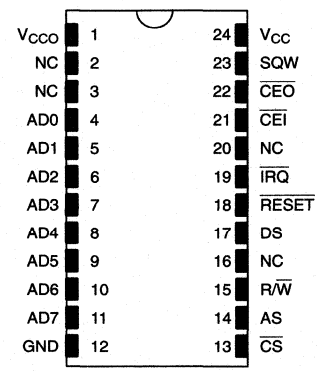
PIN ASSIGNMENT



DS14285 24–PIN DIP
DS14285S 24–PIN SOIC



DS14285Q 28–PIN PLCC



DS14287 24–PIN ENCAPSULATED PACKAGE

PIN DESCRIPTION

AD0-AD7	–	Multiplexed Address/Data Bus
NC	–	No Connection
MOT	–	Bus Type Select (DS14285Q only)
$\overline{CS}$	–	Chip Select
AS	–	Address Strobe
R/$\overline{W}$	–	Read/Write Input
DS	–	Data Strobe
$\overline{RESET}$	–	Reset Input
$\overline{IRQ}$	–	Interrupt Request Output
SQW	–	Square Wave Output
V_{CC}	–	+5 Volt Supply
GND	–	Ground
V_{CCO}	–	RAM Power Supply Output
$\overline{CEI}$	–	RAM Chip Enable In
$\overline{CEO}$	–	RAM Chip Enable Out
X1, X2	–	32.768 KHz Crystal Connections
V_{BAT}	–	+3 Volt Battery Input

DESCRIPTION

The DS14285/DS14287 Real Time Clock with NVRAM Control provides the industry standard DS1287 clock function with the additional feature of providing nonvolatile control for an external SRAM. Functions include a nonvolatile time–of–day clock, alarm, one–hundred year calendar, programmable interrupt, square wave generator, and 114 bytes of nonvolatile static RAM. For the DS14287 a lithium energy source, quartz crystal, and write–protection circuitry are contained within a 24–pin dual in–line package. The DS14285 requires an external quartz crystal connected to the X1 and X2 pins as well as an external energy source connected to the V_{BAT} pin.

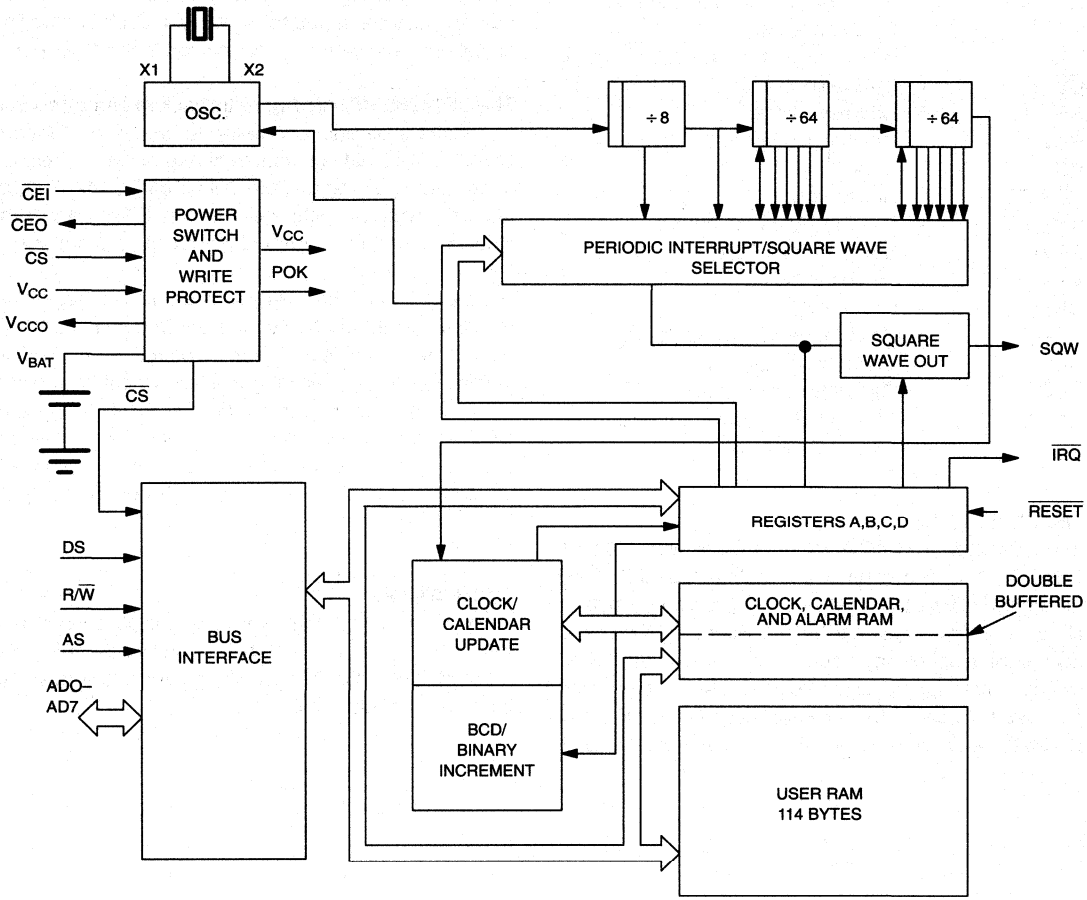
The DS14285/DS14287 uses its backup energy source and battery–backup controller to make a standard CMOS static RAM nonvolatile during power–fail conditions. During power fail, the DS14285/DS14287 automatically write protects the external SRAM and provides a V_{CC} output sourced from its internal battery.

For the DS14287 the internal lithium cell is electrically isolated from the clock and memory when shipped from the factory. This isolation is removed after the first application of V_{CC} allowing the lithium cell to provide data retention to the clock, internal RAM, V_{CCO} and $\overline{CEO}$ on subsequent power–downs. Care must be taken after this isolation has been broken to avoid inadvertently discharging the lithium cell through the V_{CCO} and $\overline{CEO}$ pins.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS14285/DS14287. The following paragraphs describe the function of each pin.

DS14285/DS14287 BLOCK DIAGRAM Figure 1



POWER-DOWN/POWER-UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS14285/DS14287 and reaches a level of greater than 4.25 volts (typical), the device becomes accessible after 200 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts (typical), the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin. The DS14285/DS14287 is, therefore, write-protected. When the DS14285/DS14287 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When V_{CC} falls below a level of approximately 3 volts, the external V_{CC} supply is switched off and an internal lithium energy source supplies power to the Real Time Clock and the RAM memory.

An external SRAM can be made nonvolatile by using the V_{CCO} and SRAM chip enable pins (see Figure 2). Nonvolatile control of the external SRAM is analogous to that of the real–time clock registers. When V_{CC} slews down during a power fail, $\overline{CEO}$ is driven to an inactive level regardless $\overline{CEI}$. This write protection occurs when V_{CC} is less than 4.25 volts (typical).

During power up, when V_{CC} reaches a level of greater than 4.25 volts (typical), $\overline{CEO}$ will reflect $\overline{CEI}$ after 200 ms. During power–valid operation, the $\overline{CEI}$ input is passed to the $\overline{CEO}$ output with a propagation delay of less than 10 ns.

When V_{CC} is above a level of approximately 3V, the external SRAM will be powered by V_{CC} through the V_{CCO} pin. When V_{CC} is below a level of approximately 3V, the external SRAM will be powered by the internal lithium cell through the V_{CCO} pin. An internal comparator and switch determine whether V_{CCO} is powered by V_{CC} or the internal lithium cell.

When the device is in battery backup mode, the energy source connected to the V_{BAT} pin in the case of the DS14285, or the internal lithium cell in the case of the DS14287 can power an external SRAM for an extended period of time. The amount of time that the lithium cell can supply power to the external SRAM is a function of the data retention current of the SRAM. The capacity of the lithium cell that is encapsulated within the DS14287 module is 130 mAh. If a SRAM with a data retention current of less than 1 µA is used and the oscillator current is 300 nA (typical), the cumulative data retention time is calculated at more than 11 years.

SIGNAL DESCRIPTIONS

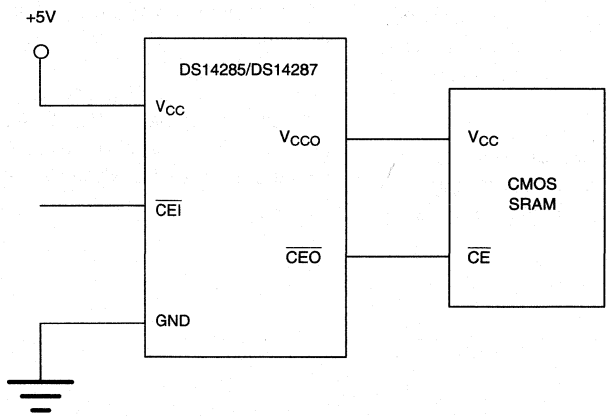
GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to an internal lithium energy source. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 1

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz
0	1	1	0	976.5625 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

EXTERNAL SRAM INTERFACE TO THE DS14285/DS14287 RTC Figure 2



AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS14285/DS14287 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the DS14285/DS14287 latches the address from AD0 to AD6. Valid write data must be present and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle the DS14285/DS14287 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as $\overline{RD}$ transitions high in the case of Intel timing.

MOT (Mode Select) – The MOT pin offers the flexibility to choose between to bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull–down resistance of approximately 20 KΩ. This pin is on the DS14285Q only.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS14285/DS14287.

DS (Data Strobe or Read Input) - For the DS14285Q the DS/$\overline{RD}$ pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS14285Q is to drive the bidirectional bus. In write cycles the trailing edge of DS causes the DS14285Q to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read($\overline{RD}$). $\overline{RD}$ identifies the time period when the DS14285Q drives the bus with read data. The $\overline{RD}$ signal is the same definition as the Output Enable ($\overline{OE}$) signal on a typical memory.

The DS14285, DS14285S and DS14287 do not have a MOT pin and therefore operate only in Intel bus timing mode.

R/$\overline{W}$ (Read/Write Input)-The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/$\overline{W}$ is at a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active low signal called $\overline{WR}$. In this mode the R/$\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{WE}$) on generic RAMs.

$\overline{CS}$ (Chip Select Input) - The Chip Select signal must be asserted low for a bus cycle in the DS14285/DS14287 to be accessed. $\overline{CS}$ must be kept in the active state during DS for Motorola timing and during $\overline{RD}$ and $\overline{WR}$ for Intel timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur. When V_{CC} is below 4.25 volts, the DS14285/DS14287 internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the real time clock data and RAM data during power outages.

$\overline{IRQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS14285/DS14287 that can be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

$\overline{RESET}$ (Reset Input) - The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{RESET}$ pin can be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power-up, the time $\overline{RESET}$ is low should exceed 200 ms to make sure that the internal timer that controls the DS14285/DS14287 on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above 4.25 volts, the follow ing occurs:

A. Periodic Interrupt Enable (PEI) bit is cleared to zero.

B. Alarm Interrupt Enable (AIE) bit is cleared to zero.

C. Update Ended Interrupt Flag (UF) bit is cleared to zero.

D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.

E. Periodic Interrupt Flag (PF) bit is cleared to zero.

F. The device is not accessible until $\overline{RESET}$ is returned high.

G. Alarm Interrupt Flag (AF) bit is cleared to zero.

H. $\overline{IRQ}$ pin is in the high impedance state.

I. Square Wave Output Enable ($\overline{SQWE}$) bit is cleared to zero.

J. Update Ended Interrupt Enable (UIE) is cleared to zero.

K. $\overline{CEO}$ is driven high.

In a typical application $\overline{RESET}$ can be connected to V_{CC}. This connection will allow the DS14287 to go in and out of power fail without affecting any of the control registers.

$\overline{CEI}$ (External RAM Chip Enable Input, active low) – $\overline{CEI}$ should be driven low to enable the external RAM. $\overline{CEI}$ is internally pulled up with a 50kΩ resistor.

$\overline{CEO}$ (External RAM Chp Enable Output, active low) – When V_{CC} is greater than 4.25 volts (typical), $\overline{CEO}$ will reflect $\overline{CEI}$ provided the $\overline{RESET}$ is at a logic high. When V_{CC} is less than 4.25 volts (typical), $\overline{CEO}$ will be forced to an inactive level regardless of $\overline{CEI}$.

V_{CCO} (External RAM Power Supply Output) – V_{CCO} provides the higher of V_{CC} or V_{BAT} through an internal switch to power an external RAM.

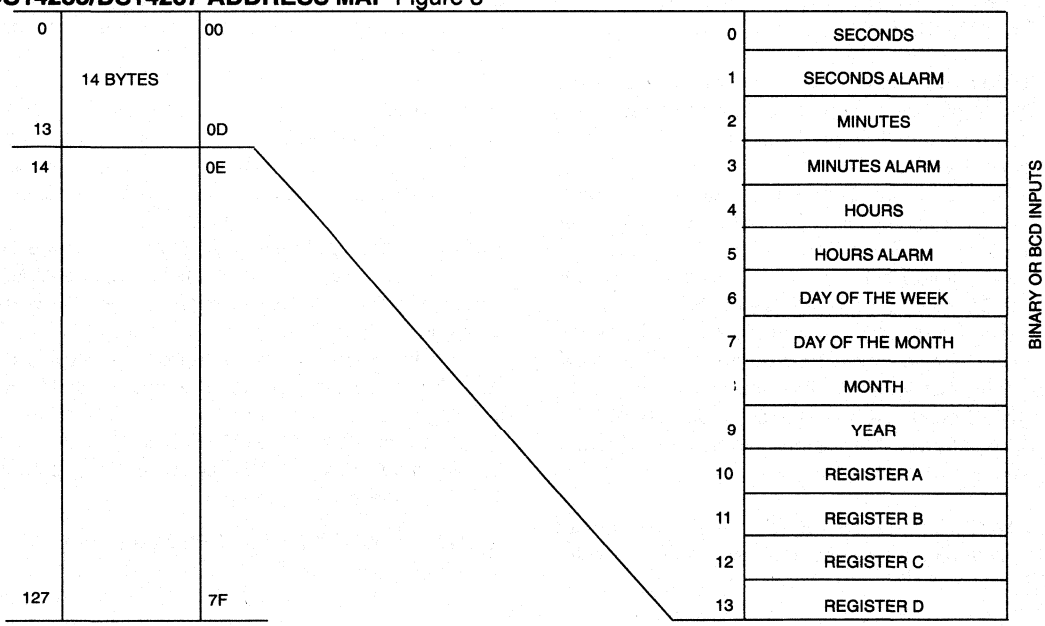
ADDRESS MAP

The address map of the DS14285/DS14287 is shown in Figure 3. The address map consists of 114 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 128 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

The contents of four registers (A,B,C, and D) are described in the "Registers" section.

DS14285/DS14287 ADDRESS MAP Figure 3



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar, and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The 24-12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one.

The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

TIME, CALENDAR AND ALARM DATA MODES Table 2

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

NONVOLATILE RAM

The 114 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS14285/DS14287. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

The DS14285/DS14287 can also provide additional nonvolatile RAM. This is accomplished through the use of its internal lithium cell in the case of the DS14287 (or the energy source connected to the V_{BAT} pin in the case of the DS14285) and battery–backup controller to make a standard CMOS SRAM nonvolatile during power–fail conditions. During power fail, the DS14285/DS14287 automatically write protects the external SRAM and provides a V_{CC} output sourced from the internal lithium cell. The interface between the DS14285/DS14287 and an external SRAM is illustrated in Figure 2.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A zero in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts a re lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS14285/DS14287. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS14287 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

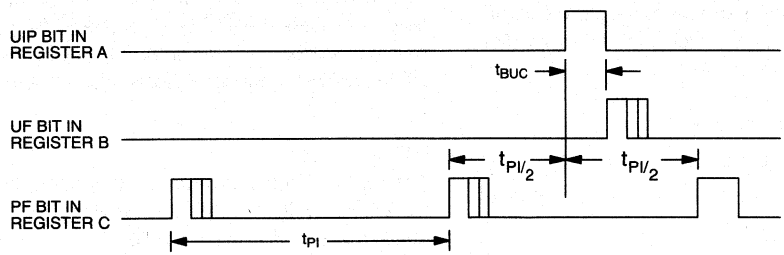
The DS14285/DS14287 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 4). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within 1 ($t_{PI/2} + t_{BUC}$) to ensure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 4



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS14285/DS14287 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2

These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1, and DV2.

RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by $\overline{\text{RESET}}$ or internal functions of the DS14285/DS14287.

PIE

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{\text{IRQ}}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS14285/DS14287 functions, but is cleared to zero on $\overline{\text{RESET}}$.

AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to zero. The internal functions of the DS14285/DS14287 do not affect the AIE bit.

UIE

The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears to UIE bit.

SQWE
When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

DM
The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{\text{RESET}}$. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12
The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write and is not affected by internal functions of $\overline{\text{RESET}}$.

DSE
The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or $\overline{\text{RESET}}$.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF
The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

That is, IRQF = PF • PIE + AF • AIE + UF • UIE.

Any time the IRQF bit is a one, the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

PF
The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{\text{IRQ}}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{\text{RESET}}$ or a software read of Register C.

AF
A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{\text{IRQ}}$ pin will go low and a one will appear in the IRQF bit. A $\overline{\text{RESET}}$ or a read of Register C will clear AF.

UF
The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{\text{IRQ}}$ pin. UF is cleared by reading Register C or a $\overline{\text{RESET}}$.

BIT 0 THROUGH BIT 3
These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT
The Valid RAM and Time (VRT) bit indicates the condition of the internal battery (the battery connected to the V_{BAT} pin in the case of the DS14285S, DS14285, and the DS14285Q). This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{\text{RESET}}$.

BIT 6 THROUGH BIT 0
The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to 7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–40°C to 70°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		7	15	mA	2
Oscillator Current	I_{OSC}		300	500	nA	
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	5
MOT Input Current	I_{MOT}	-1.0		+500	µA	3
$\overline{CEI}$ Input Current	$I_{\overline{CEI}}$	–1.0		200	µA	4
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			60	Ω	11
Output @ 2.4V	I_{OH}	-1.0			mA	1,6
Output @ 0.4V	I_{OL}			4.0	mA	1
Write Protect Voltage	V_{TP}	4.0	4.25	4.5	V	
V_{CCO} Voltage	V_{CCO1}	V_{CC}–0.3V			V	7
V_{CCO} Voltage	V_{CCO2}	V_{BAT}–0.3V			V	8

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

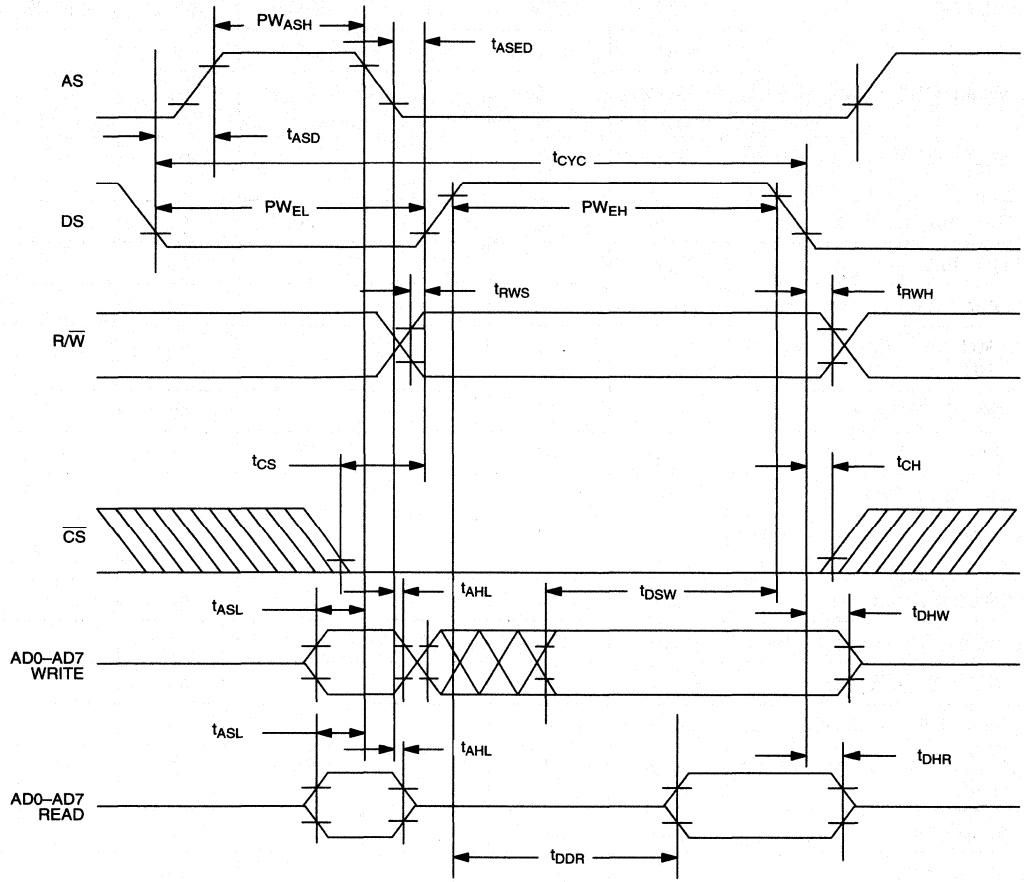
(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	225		DC	ns	
Pulse Width, DS/E Low or RD/$\overline{WR}$ High	PW_{EL}	115			ns	
Pulse Width, DS/E High or RD/$\overline{WR}$ Low	PW_{EH}	80			ns	
Input Rise and Fall Time	t_R,t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	10			ns	
Chip Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	20			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	35			ns	
Output Data Delay Time From DS/E or $\overline{RD}$	t_{DDR}	10		75	ns	9
Data Setup Time	t_{DSW}	60			ns	
Reset Pulse Width	t_{RWL}	5			µs	
$\overline{IRQ}$ Release from DS	t_{IRDS}			2	µs	
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}			2	µs	

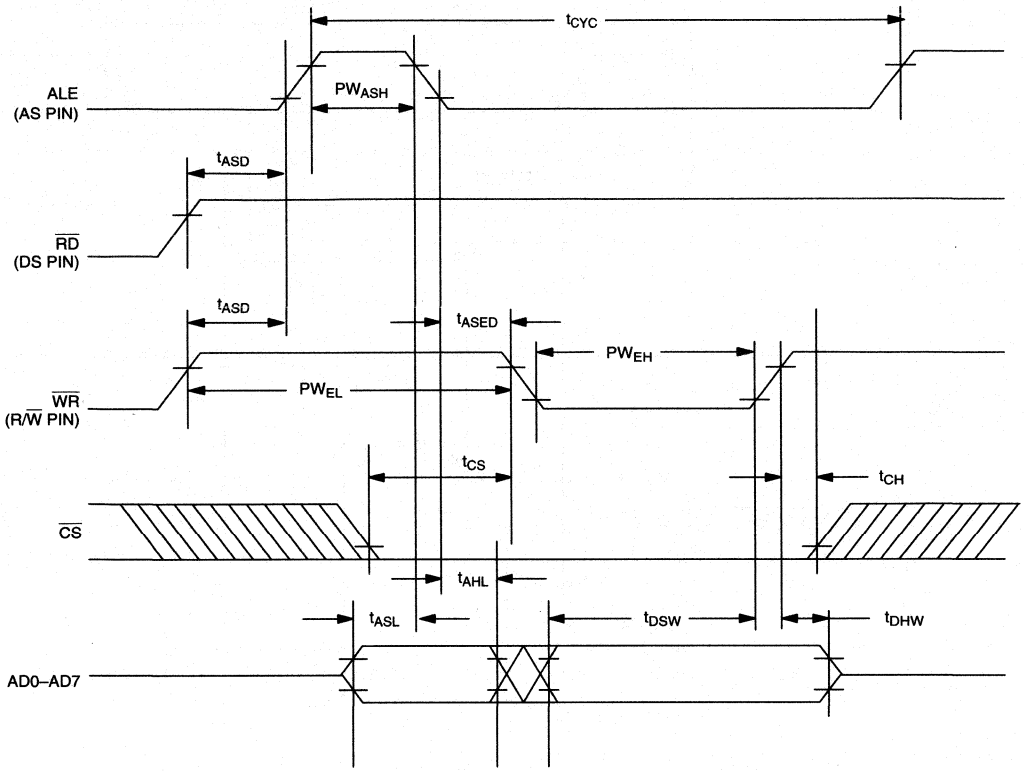
AC TEST CONDITIONS

Input Pulse Level: 0 to 3.0V
Input Rise/Fall Times: 5 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: Figure 5

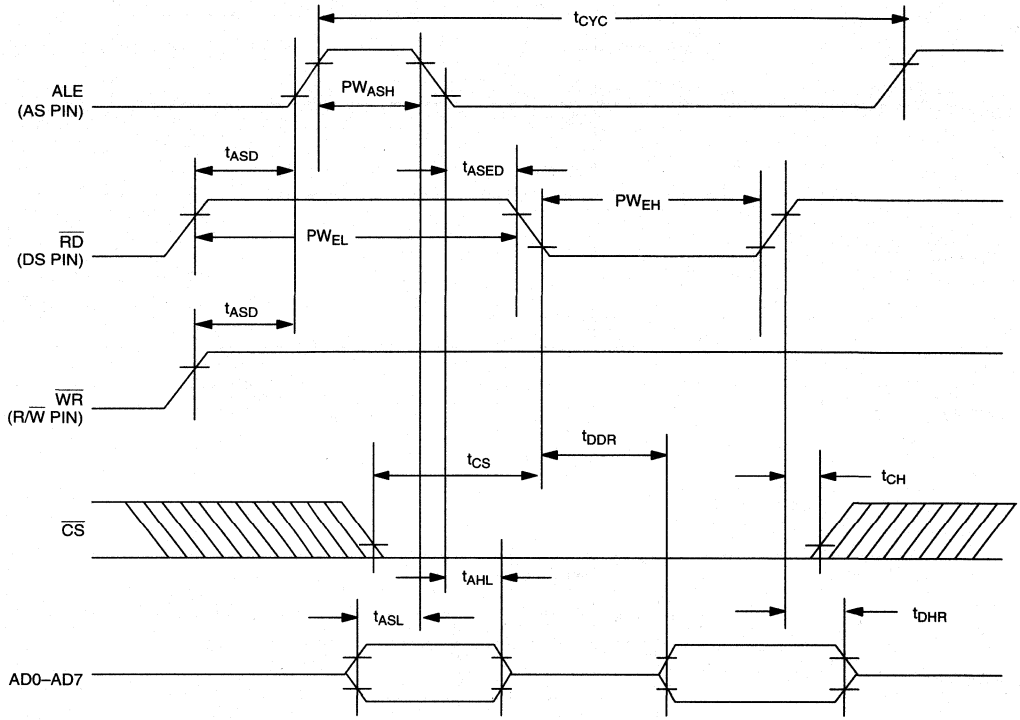
DS14285 BUS TIMING FOR MOTOROLA INTERFACE



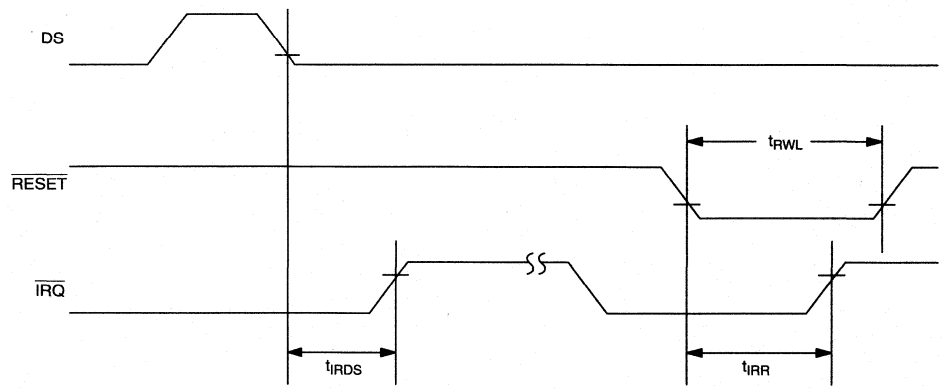
DS14285/DS14287 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



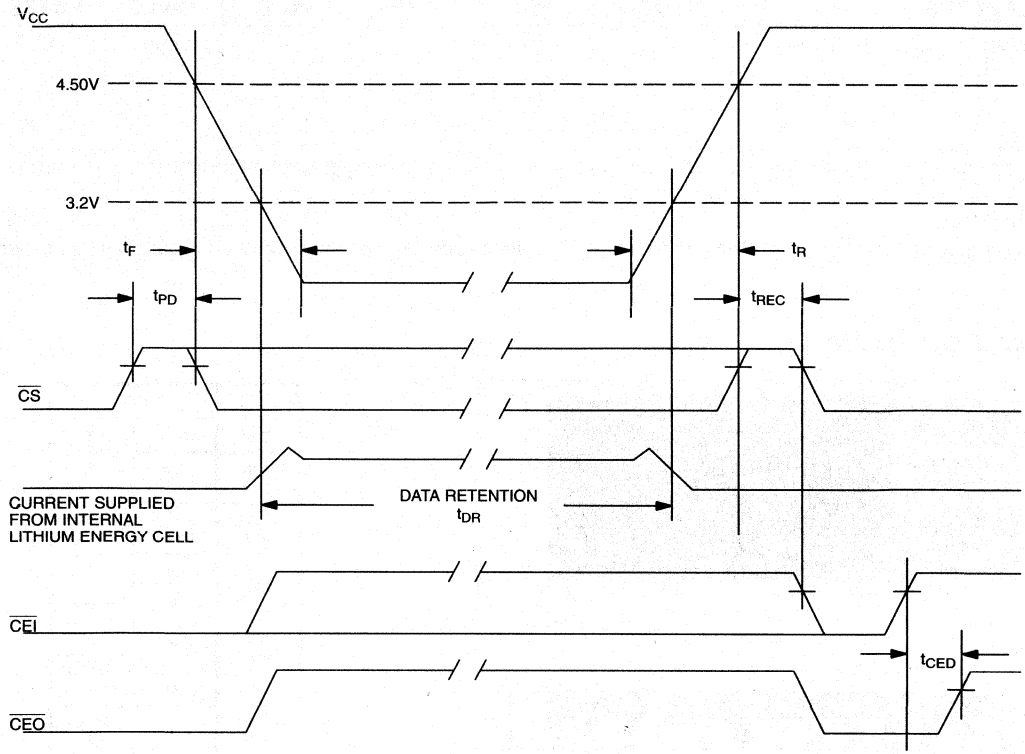
DS14285/DS14287 BUS TIMING FOR INTEL INTERFACE READ CYCLE



DS14285/DS14287 IRQ RELEASE DELAY TIMING



POWER DOWN/POWER UP TIMING



POWER DOWN/POWER UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} slew from 4.5V to 0V ($\overline{CS}$ at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to 4.5V ($\overline{CS}$ at V_{IH})	t_R	100			µs	
$\overline{CS}$ at V_{IH} after Power-Up	t_{REC}	20		200	ms	
Chip Enable Propagation Delay to External SRAM	t_{CED}			10	ns	

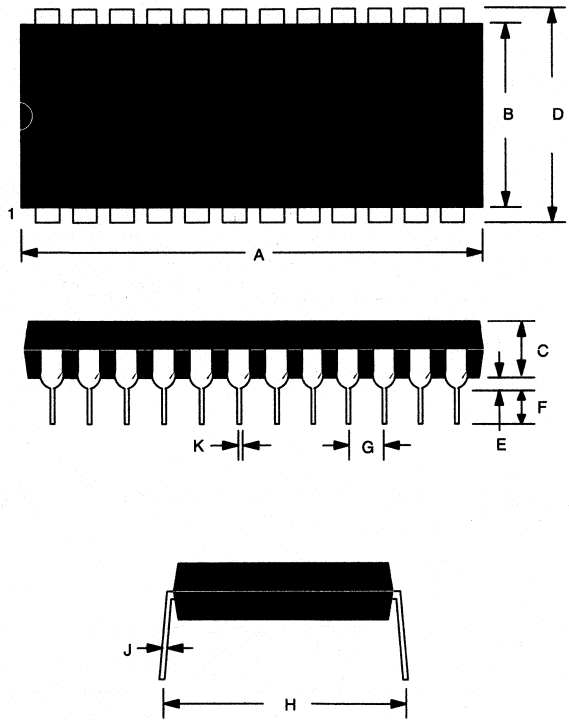
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention for DS14287	t_{DR}	10			years	10

NOTE:
The real time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.

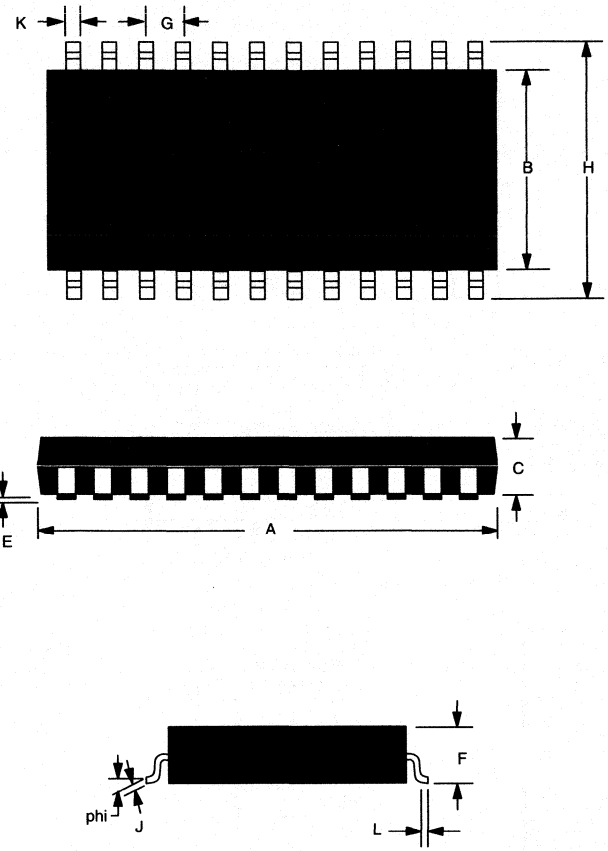
WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

DS14285 24–PIN DIP



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.245	1.270
MM	31.62	32.25
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.050
MM	0.380	1.27
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.559

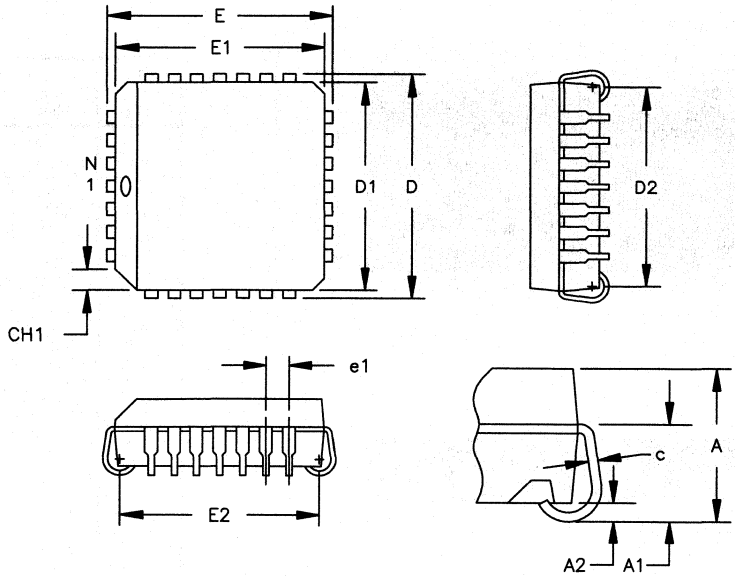
DS14285 24–PIN SOIC



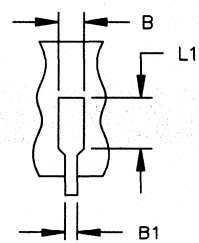
PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.602 15.29	0.612 15.54
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN. MM	0.016 0.406	0.040 1.02
phi	0°	8°

3

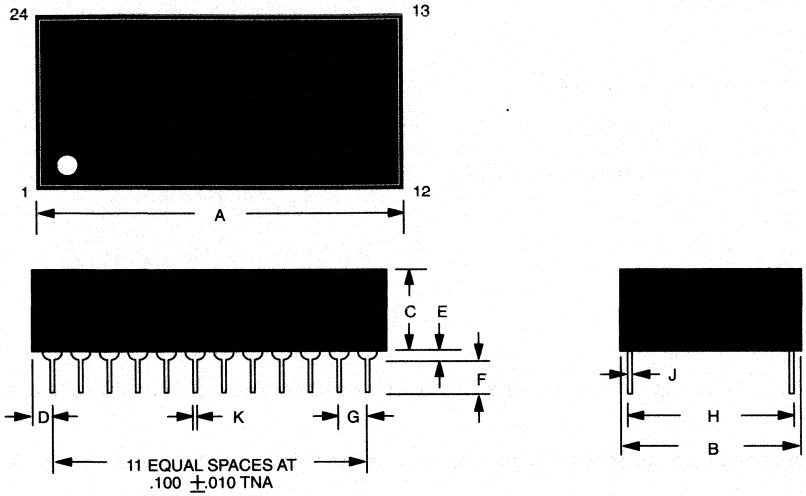
DS14285Q 28–PIN PLCC



PKG	28-PIN	
DIM	**MIN**	**MAX**
A	0.165	0.180
A1	0.090	0.120
A2	0.020	——
B	0.026	0.033
B1	0.013	0.021
c	0.009	0.012
D	0.485	0.495
D1	0.450	0.456
D2	0.390	0.430
E	0.485	0.495
E1	0.450	0.456
E2	0.390	0.430
L1	0.060	——
N	28	——
e1	0.050 BSC	
CH1	0.042	0.048



DS14287 REAL TIME CLOCK PLUS RAM



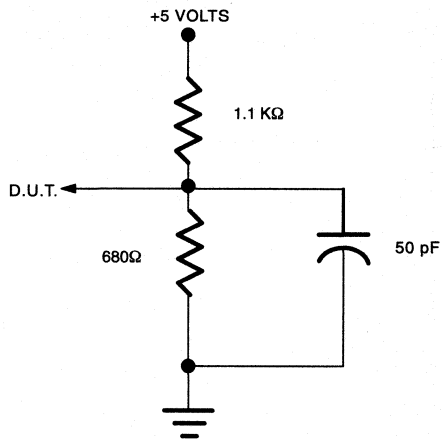
PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.720 18.29	0.740 18.80
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.

NOTES:

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pulldown of 20 KΩ.
4. The $\overline{CEI}$ pin has an internal pull–up of 50KΩ.
5. Applies to the AD0-AD7 pins, the $\overline{IRQ}$ pin,and the SQW pin when each is in the high impedance state.
6. The $\overline{IRQ}$ pin is open drain.
7. I_{CCO}=100 mA, $V_{CC} > V_{BAT}$.
8. I_{CCO}=100 µA, $V_{CC} < V_{BAT}$.
9. Measured with a load as shown in Figure 5.
10. Expected data retention is based on using an external SRAM with a data retention current of less than 1 µA at 25°C.
11. Z_{CE} is an average input–to–output impedance as the input is swept from ground to V_{CCI} and less than 4 mA is forced through Z_{CE}.

OUTPUT LOAD Figure 5



DALLAS SEMICONDUCTOR

DS1485/DS1488
RAMified Real Time Clock 8K x 8

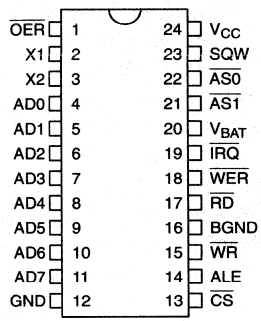
FEATURES

- Upgraded IBM AT computer clock/calendar with 8K x 8 extended RAM
- Totally nonvolatile with over 10 years of operation in the absence of power
- Counts seconds, minutes, hours, day of the week, date, month and year with leap year compensation
- Binary or BCD representations of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Multiplex bus for pin efficiency
- Interfaced with software as 64 user RAM locations plus 8K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
  - 8K x 8 SRAM accessible by using separate control pins
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End-of-clock update cycle
- Available as chip (DS1485) or stand alone module with embedded lithium battery and crystal (DS1488)

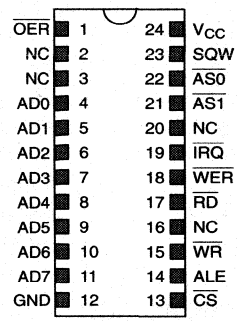
ORDERING INFORMATION

DS1485	RTC Chip; 24–pin DIP
DS1485S	RTC Chip; 28–pin SOIC
DS1488	RTC Module; 24–pin DIP

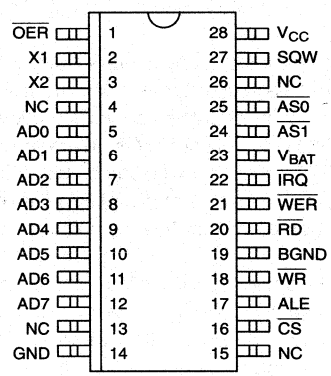
PIN ASSIGNMENT



DS1485 24–PIN DIP
(600 MIL)



DS1488 24–PIN
ENCAPSULATED PACKAGE
(740 MIL FLUSH)



DS1485S 28–PIN SOIC
(330 MIL)

PIN DESCRIPTION

$\overline{OER}$	-	RAM Output Enable
X1	-	Crystal Input
X2	-	Crystal Output
AD0-AD7	-	Mux'ed Address/Data Bus
$\overline{CS}$	-	RTC Chip Select Input
ALE	-	RTC Address Strobe
$\overline{WR}$	-	RTC Write Data Strobe
$\overline{RD}$	-	RTC Read Data Strobe
$\overline{WER}$	-	RAM Write Data Strobe
$\overline{IRQ}$	-	Interrupt Request Output (open drain)
$\overline{AS1}$	-	RAM Upper Address Strobe
$\overline{AS0}$	-	RAM Lower Address Strobe
SQW	-	Square Wave Output
V_{CC}	-	+5V Supply
GND	-	Ground
V_{BAT}	-	Battery + Supply
BGND	-	Battery Ground
NC	-	No Connection

DESCRIPTION

The DS1485/DS1488 RAMified Real Time Clocks (RTCs) are upward-compatible successors to the industry standard DS1285/DS1287 and the DS1385/DS1387 RTC's for PC applications. In addition to the basic DS1285/DS1287 RTC functions, 8K bytes of on-chip nonvolatile RAM have been added.

The RTC functions include a time-of-day clock, a one-hundred year calendar, time-of-day interrupt, periodic interrupts, and an end-of-clock update cycle interrupt. In addition, 50 bytes of user NV RAM are provided within this basic RTC function which can be used to store configuration data. The clock and user RAM are maintained in the absence of system V_{CC} by a lithium battery.

The 8K x 8 additional NV RAM is provided to store a much larger amount of system configuration data than is possible within the original 50 byte area. This RAM is accessed via control signals separate from the RTC, and is also maintained as nonvolatile storage from the lithium battery.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1485/DS1488. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to the energy source connected to the V_{BAT} pin in the case of the DS1485, or to the internal battery in the case of the DS1488. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

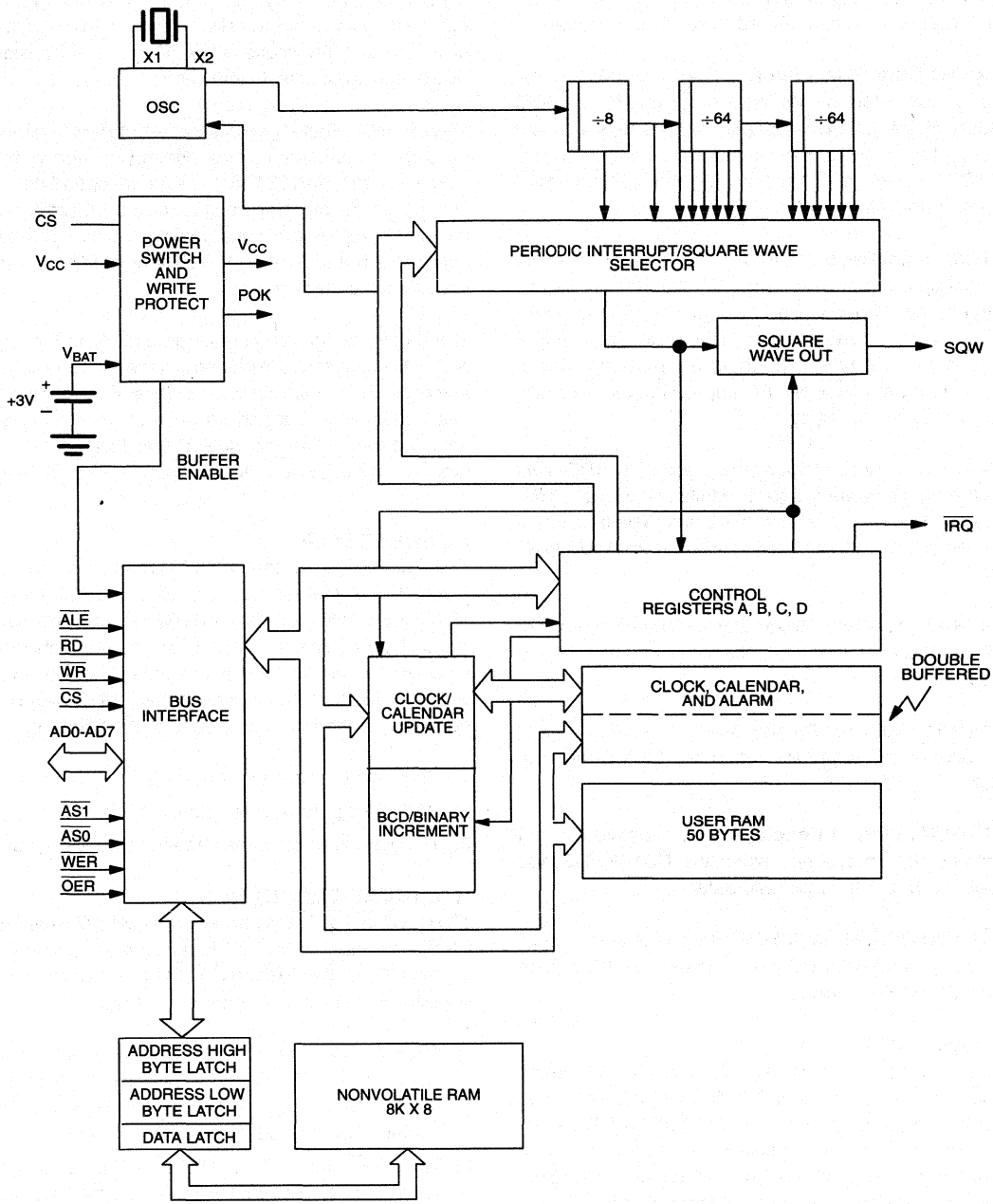
SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1485/DS1488 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, $\overline{AS0}$, or $\overline{AS1}$, at which time the DS1485/DS1488 latches the address from AD0 to AD7. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ or $\overline{WER}$ pulses. In a read cycle, the DS1485/DS1488 outputs 8 bits of data during the latter portion of the $\overline{RD}$ or $\overline{OER}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ or $\overline{OER}$ transitions high.

ALE (RTC Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1485/DS1488.

$\overline{RD}$ (RTC Read Input) - $\overline{RD}$ identifies the time period when the DS1485/DS1488 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

DS1485/DS1488 BLOCK DIAGRAM Figure 1



$\overline{WR}$ (RTC Write Input) -The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed clock register.

$\overline{CS}$ (RTC Chip Select Input) - The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1485/DS1488 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur.

$\overline{IRQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS1485/DS1488 that can be tied to an interrupt input on a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application program normally reads the C register.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

$\overline{AS0}$ (RAM Address Strobe Zero) - The rising edge of $\overline{AS0}$ latches the lower eight bits of the 8K x 8 RAM address.

$\overline{AS1}$ (RAM Address Strobe One) - The rising edge of $\overline{AS1}$ latches the upper five bits of the 8K x 8 RAM address.

$\overline{OER}$ (RAM Output Enable) - $\overline{OER}$ is active low and identifies the time period when the DS1485/DS1488 drives the bus with RAM read data.

$\overline{WER}$ (RAM Write Enable) - $\overline{WER}$ is an active low signal and is used to perform writes to the 8K x 8 RAM portion of the DS1485/DS1488.

(DS1485 ONLY)

X1, X2 - Connections for a standard 32.768 KHz quartz crystal, Daiwa part number DT-26S or equivalent. When ordering, request a load capacitance of 6 pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks".

V_{BAT}, BGND - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage is set by the internal circuitry and is 4.25 volts typical. A maximum load of 1 µA at 25°C and 3.0V on V_{BAT} should be used to size the external energy source.

The battery should be connected directly to the V_{BAT} pin. A diode must not be placed in series with the battery to the V_{BAT} pin. Furthermore, a diode is not necessary because reverse charging current protection circuitry is provided internal to the device and has passed the requirements of Underwriters Laboratories for UL listing.

ADDRESS MAP

The address map of the DS1485/DS1488 is shown in Figure 2. The address map consists of the RTC and the 8K X 8 NV SRAM section. The RTC section contains 50 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

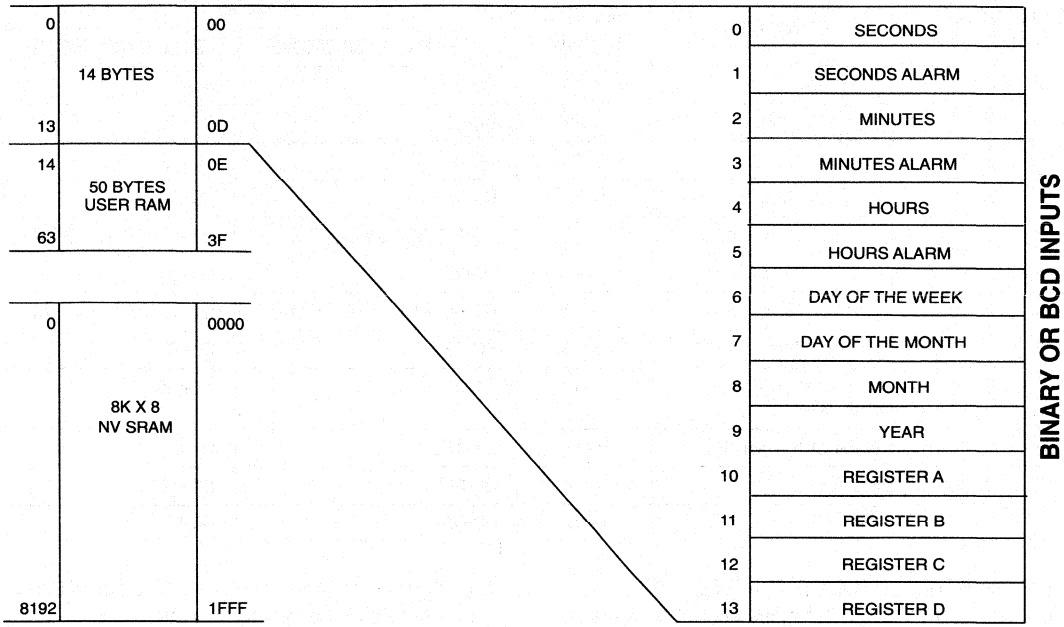
1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

RTC (REAL TIME CLOCK)

The RTC function is the same as the DS1287 Real Time Clock. Access to the RTC is accomplished with four controls: ALE, $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$. The RTC is the same in the DS1287 with the following exceptions:

1. The MOT pin on the DS1285/DS1287 is not present on the DS1485/DS1488. The bus selection capability of the DS1285/DS1287 has been eliminated. Only the Intel bus interface timing is applicable.
2. The $\overline{RESET}$ pin on the DS1285/DS1287 is not present on the DS1485/DS1488. The DS1485/DS1488 will operate the same as the DS1285/DS1287 with $\overline{RESET}$ tied to V_{CC}.

ADDRESS MAP DS1485/DS1488 Figure 2



3

TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second method is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

USER NONVOLATILE RAM - RTC

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1485/DS1488. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that

the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1485/DS1488. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS1485/DS1488 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

3

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 KHz
0	1	0	0	244.141 µs	4.096 KHz
0	1	0	1	488.281 µs	2.048 KHz
0	1	1	0	976.5625 µs	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

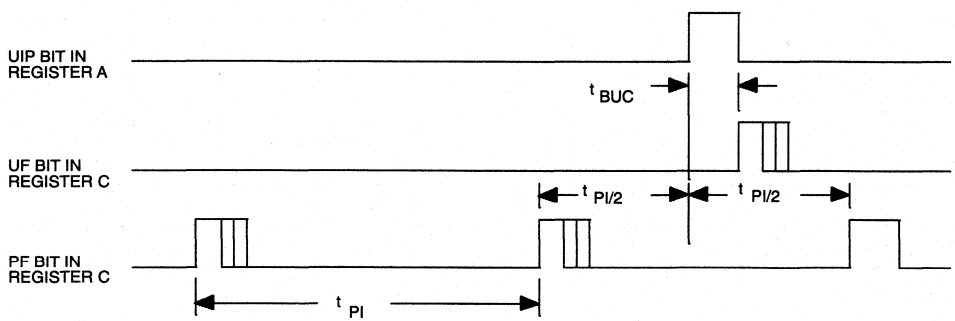
The DS1485/DS1488 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($t_{PI}/2+t_{BUC}$) to ensure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS1485/DS1488 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1485/DS1488.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1485/DS1488 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1485/DS1488 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update Ended Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1
i.e., IRQF = (PF • PIE) + (AF • ALE) + (UF • UIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 0 THROUGH BIT 3 - These are reserved bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.

8K X 8 RAM

The DS1485/DS1488 provides 8K x 8 of on-chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by the internal power OK signal (POK) generated from the write protect circuitry. The POK signal becomes active at 4.25 volts (typical).

The on-chip 8K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7-AD0. Access to the SRAM is controlled by three on-chip latch registers. Two registers are used to hold the SRAM address, and the third register is used to hold read/write data. The SRAM address space is from 0000H to 1FFFH. A direct hardware interface to the SRAM is supported.

Four control signals, $\overline{AS0}$, $\overline{AS1}$, $\overline{OER}$, and $\overline{WER}$, are used to access the 8K x 8 SRAM. This access mode is identical to that supported by the DS1385/DS1387. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ($\overline{AS0}$) and Address Strobe 1 ($\overline{AS1}$) signals. $\overline{AS0}$ is used to latch the lower 8-bits of address, and $\overline{AS1}$ is used to latch the upper 5-bits of address. It is necessary to meet the setup and hold times given in the Electrical Specifications with valid address information in order to properly latch the address. If the upper or lower order address is correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation requires valid data to placed on the bus (AD7-AD0) followed by the activation of the Write Enable RAM ($\overline{WER}$) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Output Enable RAM ($\overline{OER}$) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met. The $\overline{WER}$ and $\overline{OER}$ signals should never be active at the same time. In addition, access to the clock/calendar registers and user RAM (via $\overline{CS}$) must not be attempted when the 8K x 8 RAM is being accessed. The RAM is enabled when either $\overline{WER}$ or $\overline{OER}$ is active. $\overline{CS}$ is only used for the access of the clock calendar registers and the 50 bytes of user RAM.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	DS1488: -40°C to +70°C DS1485: –55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	9

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C)

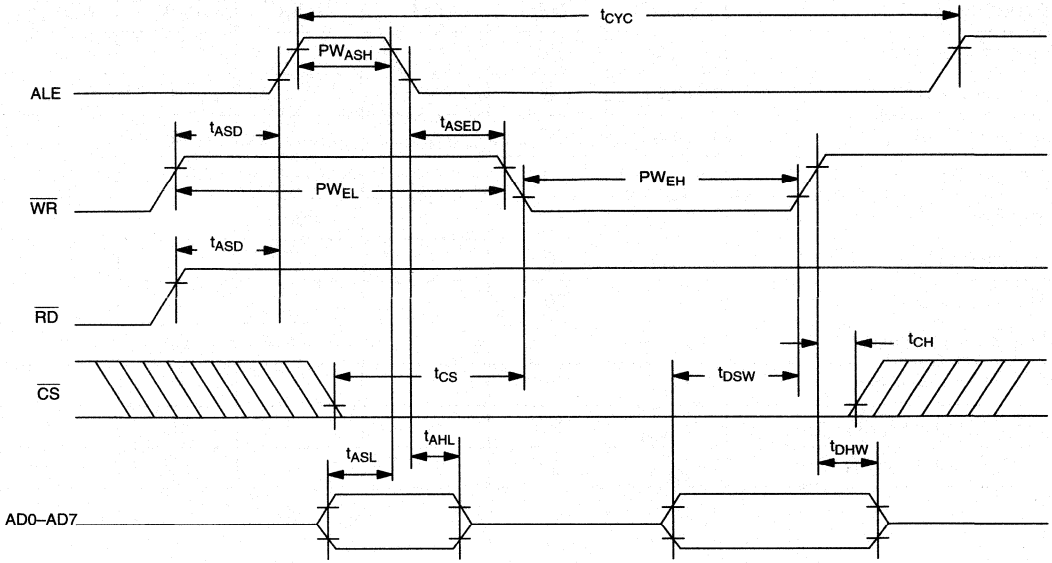
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		35	50	mA	2
Standby Current $\overline{CS}$, $\overline{OER}$, and $\overline{WER}$ = V_{CC} -0.3V	I_{CC2}		1	5.0	mA	6
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	3
Output @ 2.4V	I_{OH}	-1.0			mA	1,4
Output @ 0.4V	I_{OL}			2.0	mA	1

RTC AC TIMING CHARACTERISTICS

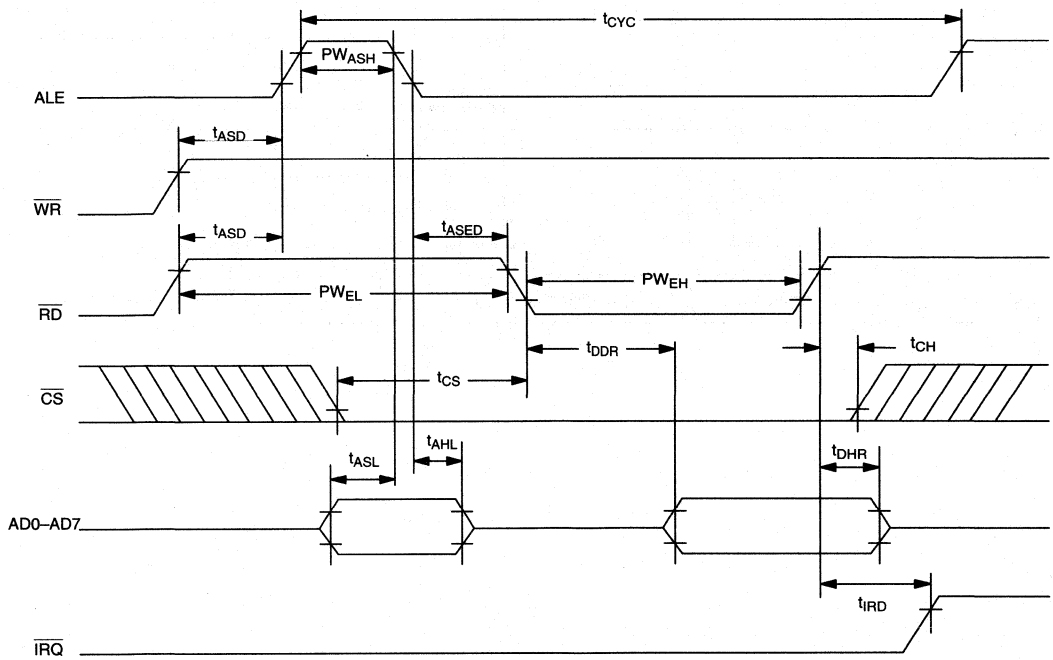
(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{EH}	125			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{EL}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	5
Data Setup Time to Write	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

DS1485/DS1488 BUS TIMING FOR WRITE CYCLE TO RTC



DS1485/DS1488 BUS TIMING FOR READ CYCLE TO RTC

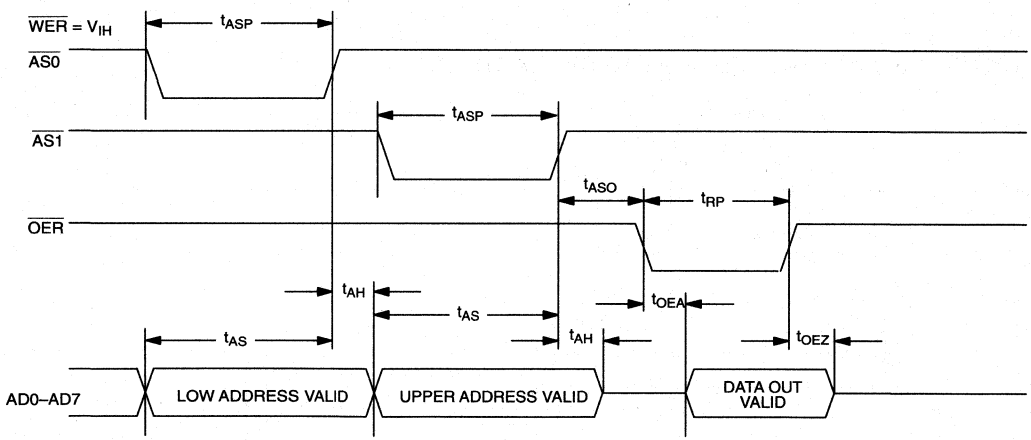


8K X 8 AC TIMING CHARACTERISTICS

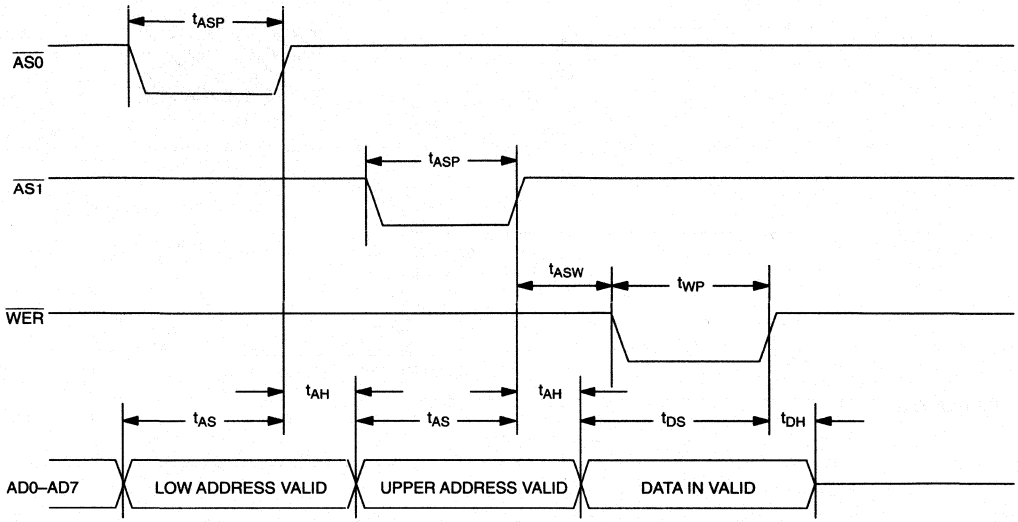
($0°C$ to $70°C$; V_{CC} = 5V + 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	50			ns	
Address Hold Time	t_{AH}	0			ns	
Data Setup Time	t_{DS}	75			ns	
Data Hold Time	t_{DH}	0			ns	
Output Enable Access Time	t_{OEA}			200	ns	7
Write Pulse Width	t_{WP}	200			ns	
$\overline{OER}$ Pulse Width	t_{RP}	200			ns	
$\overline{OER}$ to Output in High Z	t_{OEZ}			50	ns	
$\overline{AS0}$, $\overline{AS1}$ Pulse Width	t_{ASP}	75			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{OER}$ Low	t_{ASO}	20			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{WER}$ Low	t_{ASW}	20			ns	

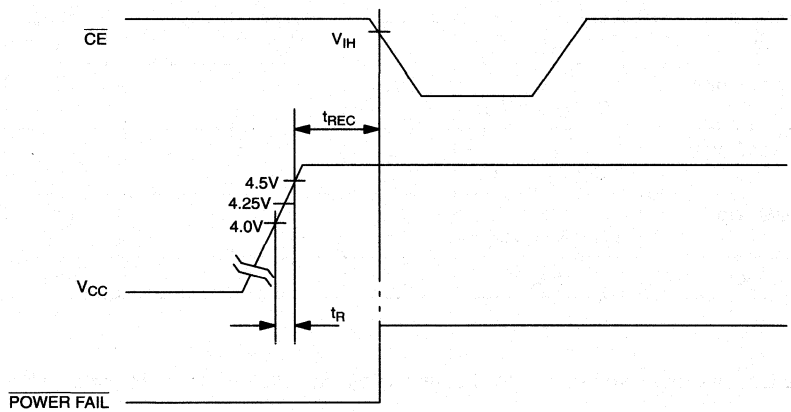
BUS TIMING FOR READ CYCLE TO 8K X 8 NV SRAM



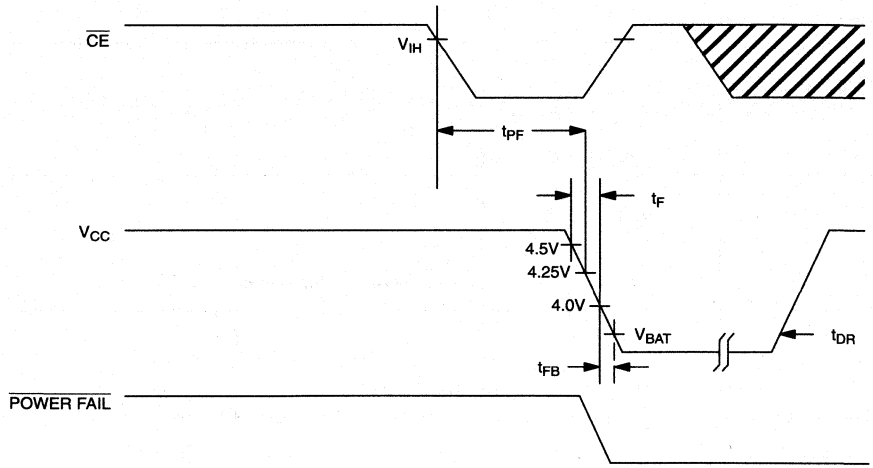
BUS TIMING FOR WRITE CYCLE TO 8K X 8 SRAM



POWER-UP CONDITION



POWER-DOWN CONDITION



POWER-UP POWER-DOWN TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	8

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

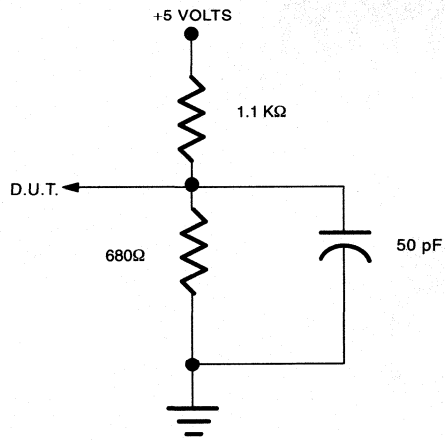
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

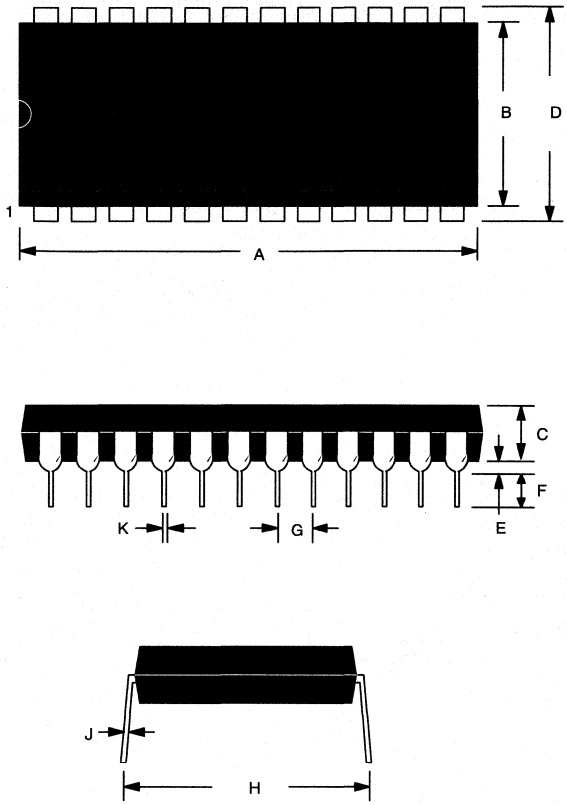
NOTES:

1. All voltages are referenced to ground.
2. All outputs are open.
3. Applies to the AD0-AD7 pins, and the SQW pin when each is in the high impedance state.
4. The $\overline{IRQ}$ pin is open drain.
5. Measured with a load as shown in Figure 4.
6. All other inputs at CMOS levels.
7. Measured with a load as shown in Figure 4.
8. The real-time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
9. Applies to DS1485 only.

OUTPUT LOAD Figure 4

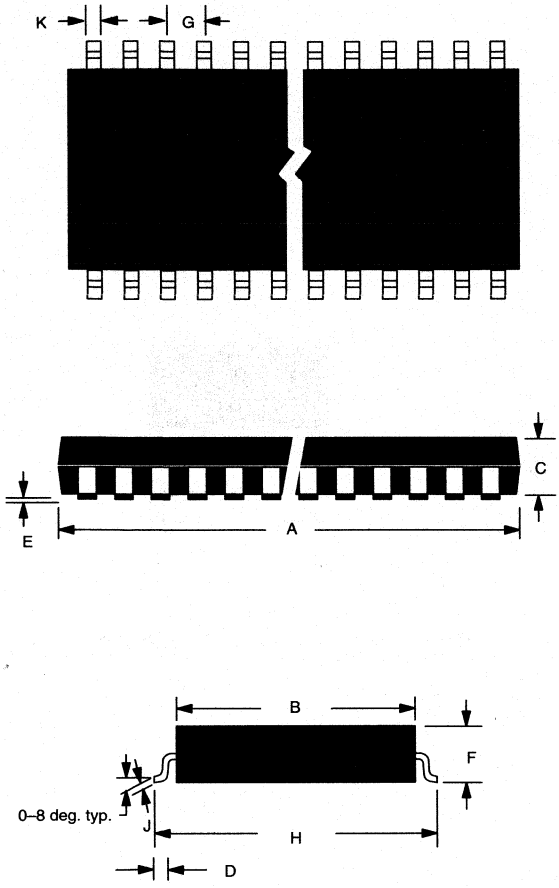


DS1485 24–PIN DIP



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN.	1.245	1.270
MM	31.62	32.26
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.050
MM	0.38	1.27
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

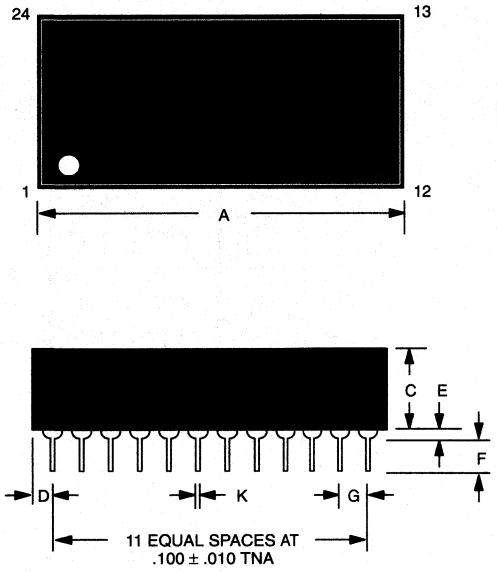
DS1485S 28–PIN SOIC



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	0.706	0.728
MM	17.93	18.49
B IN.	0.338	0.350
MM	8.58	8.89
C IN.	0.086	0.110
MM	2.18	2.79
D IN.	0.020	0.050
MM	0.58	1.27
E IN.	0.002	0.014
MM	0.05	0.36
F IN.	0.090	0.124
MM	2.29	3.15
G IN.	0.050	BSC
MM	1.27	
H IN.	0.460	0.480
MM	11.68	12.19
J IN.	0.006	0.013
MM	0.15	0.33
K IN.	0.014	0.020
MM	0.36	0.51

3

DS1488 24–PIN 740 MIL FLUSH ENCAPSULATED



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN.	1.320	1.335
MM	33.53	33.91
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.345	0.370
MM	8.76	9.40
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.89
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

DS1486
RAMified Watchdog Timekeeper

3

FEATURES

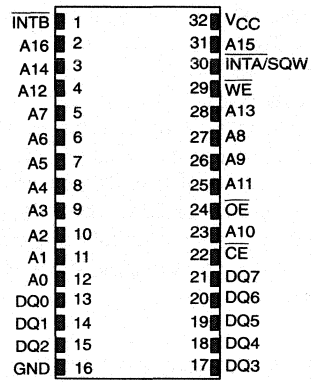
- 128K bytes of user NV RAM
- Real time quartz clock/calendar keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Will operate in 32-pin JEDEC footprint
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities such as system wakeup
- Embedded lithium energy cell maintains time, watchdog, user RAM, and alarm information
- Programmable interrupts and square wave outputs
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25°C
- Greater than 10 years of timekeeping in the absence of V_{CC} @ 25%
- Interrupt signals active in power-down mode

ORDERING INFORMATION

DS1486-XX — RTC and 128K x 8 NVSRAM

- -12 120 ns access
- -15 150 ns access

PIN ASSIGNMENT



DS1486 128K x 8
32-Pin Encapsulated Package

PIN DESCRIPTION

INTB(INTB)	-	Interrupt Output B (open drain)
A0-A16	-	Address Inputs
DQ0-DQ7	-	Data Input/Output
CE	-	Chip Enable
OE	-	Output Enable
WE	-	Write Enable
V_{CC}	-	+5 Volts
GND	-	Ground
INTA/SQW	-	Interrupt Output A/Square Wave Output (INTA is open drain)

DESCRIPTION

The DS1486 RAMified Timekeeper is a self-contained real time clock (RTC), alarm, watchdog timer, and interval timer in a 32-pin JEDEC DIP package. The DS1486 contains an embedded lithium energy source and a quartz crystal which eliminates the need for any external circuitry. Data contained within 128K by 8-bit memory and the timekeeping registers can be read or written in the same manner as bytewide static RAM. The timekeeping registers are located in the first 14 bytes of memory space. Data is maintained in the RAMified Timekeeper by intelligent control circuitry which detects the status of V_{CC} and write protects memory when V_{CC} is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of V_{CC}. Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The RAMified Timekeeper operates in either 24 hour or 12 hour format with an AM/

PM indicator. The watchdog timer provides alarm interrupts and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week. Interrupts for both watchdog and RTC will operate when system is powered down. Either can provide system "wake-up" signals.

OPERATION - READ REGISTERS

The DS1486 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (High) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (Low). The unique address specified by the address inputs (A0-A16) defines which of the registers is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE REGISTERS

The DS1486 is in the write mode whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set-Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

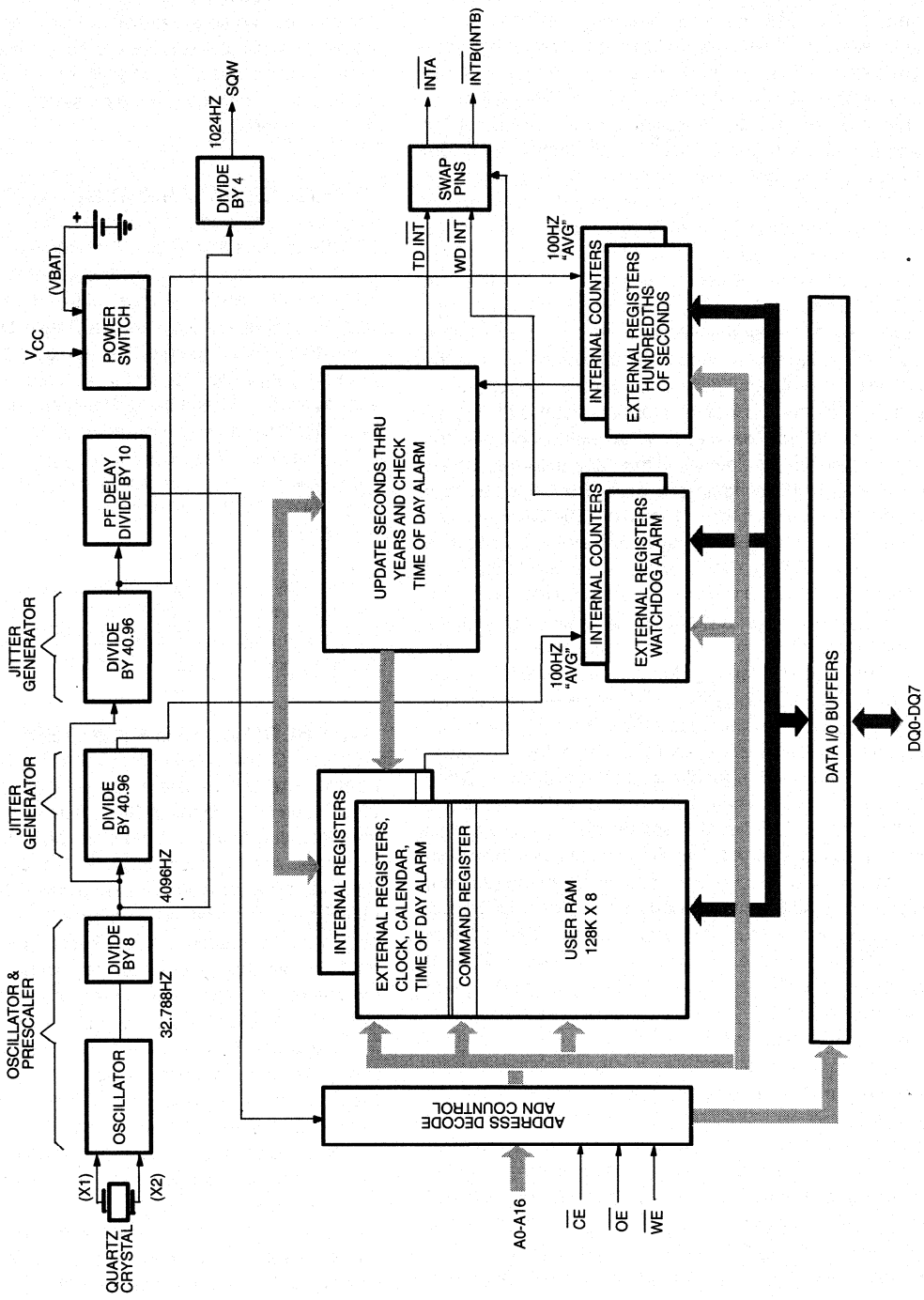
DATA RETENTION

The RAMified Timekeeper provides full functional capability when V_{CC} is greater than 4.5 volts and write-protects the register contents at 4.25 volts typical. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1486 constantly monitors V_{CC}. Should the supply voltage decay, the RAMified Timekeeper will automatically write-protect itself and all inputs to the registers become "don't care". The two interrupts $\overline{INTA}$ and $\overline{INTB}$ (INTB) and the internal clock and timers continue to run regardless of the level of V_{CC}. However, it is important to insure that the pull–up resistors used with the interrupt pins are never pulled up to a value that is greater than V_{CC} + 0.3V. As V_{CC} falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} and disconnects the internal lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for a period of 200 ms.

RAMIFIED TIMEKEEPER REGISTERS

The RAMified Timekeeper has 14 registers which are eight bits wide that contain all of the timekeeping, alarm, watchdog and control information. The clock, calendar, alarm, and watchdog registers are memory locations which contain external (user-accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. Register 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm Registers and information which is stored in these two registers is in BCD. Register E through 1FFFF are user bytes and can be used to maintain data at the user's discretion.

BLOCK DIAGRAM Figure 1



TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic zero, $\overline{EOSC}$ (Bit 7) enables the real time clock oscillator. This bit is set to logic one as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the $\overline{INTA}$/Square Wave Output (pin 30). When set to logic zero, the $\overline{INTA}$/Square Wave Output pin will output a 1024 Hz square wave signal. When set to logic one the Square Wave Output pin is available for interrupt A output ($\overline{INTA}$) only. Bit 6 of the Hours register is defined as the 12 or 24 hour select bit. When set to logic one, the 12 hour format is selected. In the 12 hour format, bit 5 is the AM/PM bit with logic one being PM. In the 24 hour mode, bit 5 is the second 10 hour bit (20-23 hours). The Time of Day registers are updated every .01 seconds from the Real Time Clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the RAMified Timekeeper is to access the Command register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable bit) to a logic zero. This will freeze the External Time of Day registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic one, will put the Time of Day Registers back to being updated every .01 second. No time is lost in the real time clock because the internal copy of the Time of Day register buffers is continually incremented while the external memory registers are frozen. An alternate method of reading and writing the Time of Day registers is to ignore synchronization. However, any single read may give erroneous data as the real time clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented, and the Time of Day Alarm is checked during the period that hundreds of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the RAMified Timekeeper.

TIME OF DAY ALARM REGISTERS

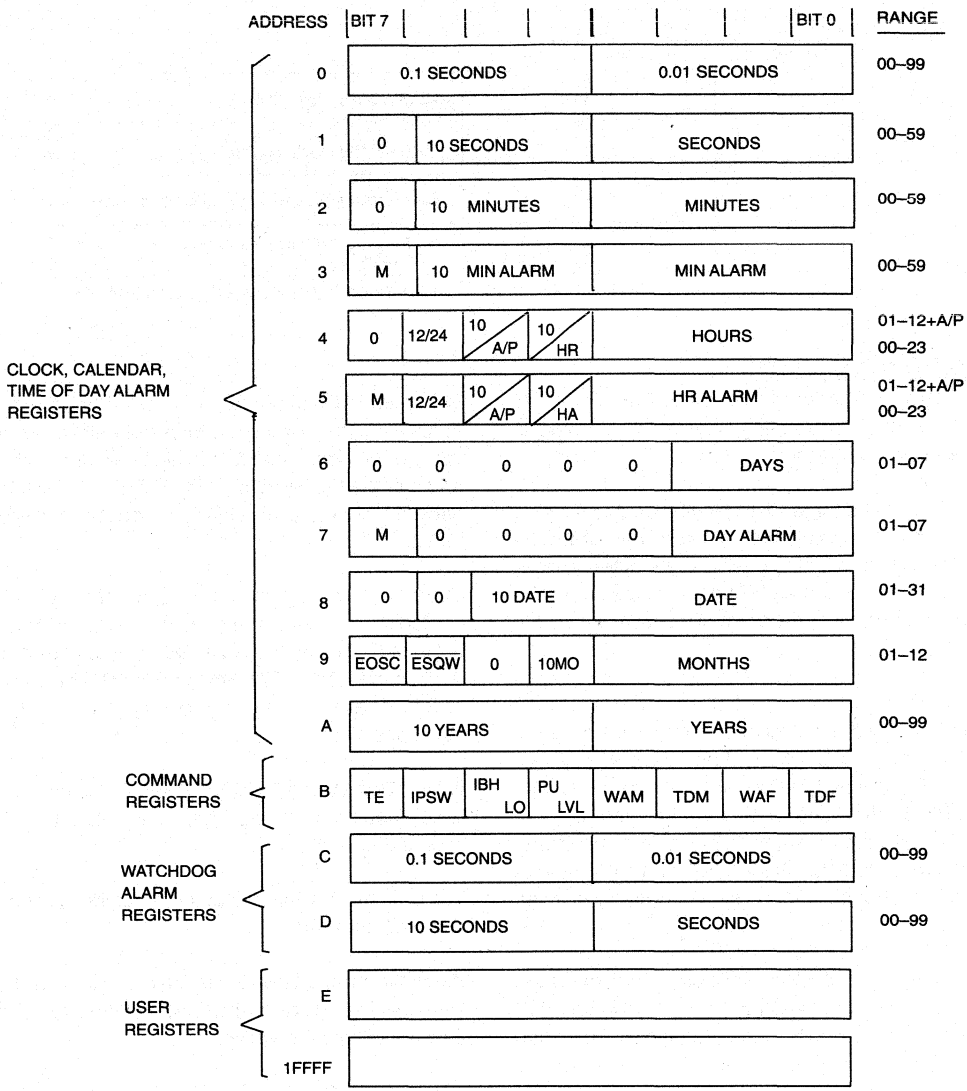
Registers 3, 5, and 7 contain the Time of Day Alarm Registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logic zero, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic one. Similarly, an alarm is generated every hour when bit 7 of Registers 7 and 5 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm Registers are written and read in the same format as the Time of Day Registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm Registers are read or written.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer Countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual count- down register is internal and is not readable. Writing registers C and D to zero will disable the Watchdog Alarm feature.

DS1486 RAMIFIED TIMEKEEPER REGISTERS Figure 2



TIME OF DAY ALARM MASK BITS Figure 3

REGISTER			
(3) MINUTES	(5) HOURS	(7) DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

NOTE: ANY OTHER BIT COMBINATIONS OF MASK BIT SETTINGS PRODUCE ILLOGICAL OPERATION.

COMMAND REGISTER

Address location 0Bh is the Command Register where mask bits, control bits and flag bits reside. The operation of each bit is as follows:

TE - Bit 7 Transfer enable - This bit when set to a logic 0 will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and reads or writes will not be affected with updates. This bit must be set to a logic 1 to allow updates.

IPSW - Bit 6 Interrupt switch - When set to a logic 1, $\overline{INTA}$ is the Time of Day Alarm and INTB/($\overline{INTB}$) is the Watchdog Alarm. When set to logic 0, this bit reverses the output pins. $\overline{INTA}$ is now the Watchdog Alarm output and INTB/($\overline{INTB}$) is the Time of Day Alarm output. The $\overline{INTA}$/SQW output pin shares both the interrupt A and square wave output function. $\overline{INTA}$ and the square wave function should never be simultaneously enabled or a conflict may occur.

IBH/LO - Bit 5 Interrupt B Sink or Source Current - When this bit is set to a logic 1 and V_{CC} is applied, INTB/($\overline{INTB}$) will source current (see DC characteristics IOH). When this bit is set to a logic 0, INTB will sink current (see DC characteristics IOL).

PU/LVL - Bit 4 Interrupt pulse mode or level mode - This bit determines whether both interrupts will output a pulse or level signal. When set to a logic 0, $\overline{INTA}$ and INTB/($\overline{INTB}$) will be in the level mode. When this bit is set to a logic 1, the pulse mode is selected and $\overline{INTA}$ will sink current for a minimum of 3 ms and then release. INTB/($\overline{INTB}$) will either sink or source current, depending on the condition of Bit 5, for a minimum of 3 ms and then release.

WAM - Bit 3 Watchdog Alarm Mask - When this bit is set to a logic 0, the Watchdog Interrupt output will be activated. The activated state is determined by bits 1,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Watchdog interrupt output is deactivated.

TDM - Bit 2 Time of Day Alarm Mask - When this bit is set to a logic 0, the Time of Day Alarm Interrupt output will be activated. The activated state is determined by bits 0,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1 , the Time of Day Alarm interrupt output is deactivated.

WAF - Bit 1 Watchdog Alarm Flag - This bit is set to a logic 1 when a watchdog alarm interrupt occurs. This bit is read only.

The bit is reset when any of the Watchdog Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

TDF - Bit 0 Time of Day Flag - This is a read only bit. This bit is set to a logic 1 when a Time of Day alarm has occurred. The time the alarm occurred can be determined by reading the Time of Day Alarm registers. This bit is reset to a logic 0 state when any of the Time of Day Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to + 70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	10
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	10
Input Logic 0	V_{IL}	-0.3		+0.8	V	10

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
Output Leakage Current	I_{LO}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LIO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}			2.1	mA	13
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE}$ = V_{CC} -0.5	I_{CCS2}			4.0	mA	
Active Current	I_{CC}			85	mA	
Write Protection Voltage	V_{TP}		4.25		V	

CAPACITANCE

(t_A = 25°C)

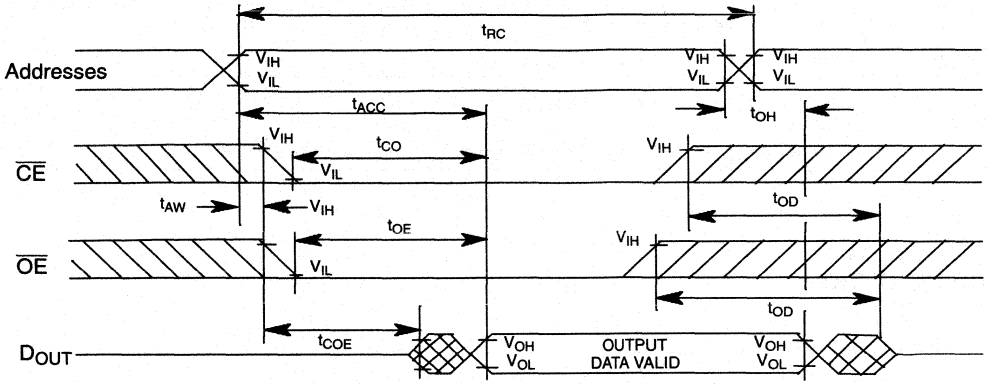
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		7	15	pF	
Output Capacitance	C_{OUT}		7	15	pF	
Input/Output Capacitance	$C_{I/O}$		7	15	pF	

AC ELECTRICAL CHARACTERISTICS

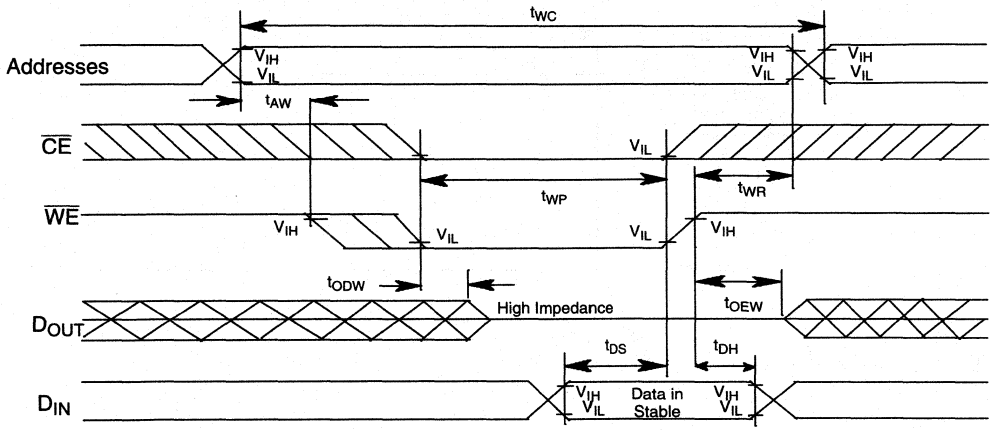
(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	DS1486–12		DS1486–15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	1
Address Access Time	t_{ACC}		120		150	ns	
$\overline{CE}$ Access Time	t_{CO}		120		150	ns	
$\overline{OE}$ Access Time	t_{OE}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10		10		ns	
Output High Z from Deselect	t_{OD}		40		50	ns	
Output Hold from Address Change	t_{OH}	10		10		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Write Pulse Width	t_{WP}	110		140		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	10		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		40		50	ns	
Output Active from $\overline{WE}$	t_{OEW}	10		10		ns	
Data Setup Time	t_{DS}	85		110		ns	4
Data Hold Time	t_{DH}	10		15		ns	4,5
$\overline{INTA}$, $\overline{INTB}$ Pulse Width	t_{IPW}	3		3		ms	11,12

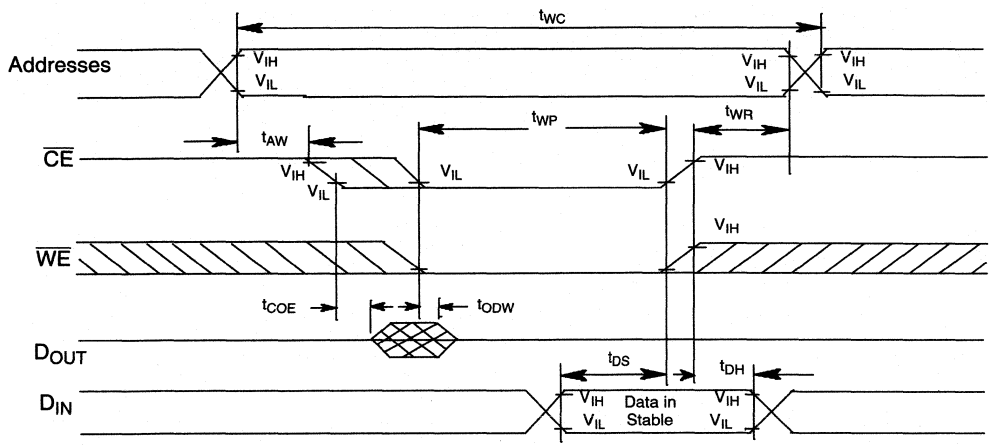
READ CYCLE (Note1)



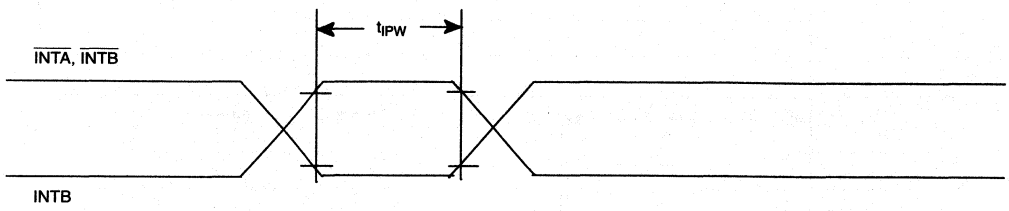
WRITE CYCLE 1 (Notes 2, 6, 7)



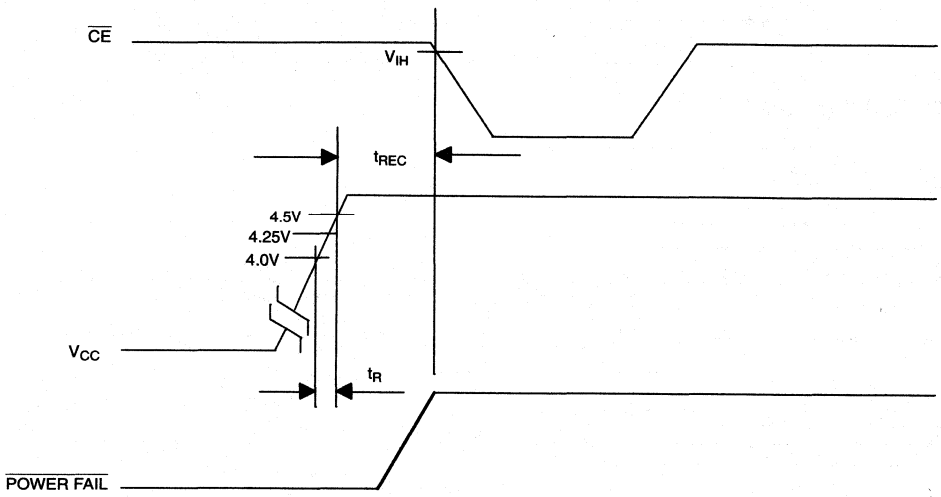
WRITE CYCLE 2 (Notes 2, 8)



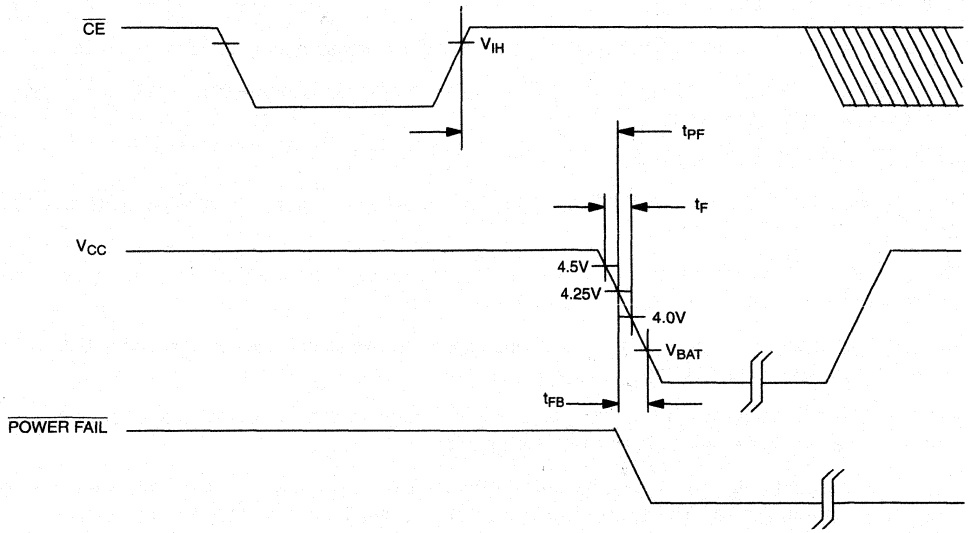
TIMING DIAGRAM: INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



POWER-UP CONDITION



POWER-DOWN CONDITION



AC ELECTRICAL CHARACTERISTICS POWER-UP POWER-DOWN TIMING (0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}		0	ns	
Recovery at Power Up	t_{REC}		200	ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300		µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.25V$	10		µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0		µs	
Expected Data Retention	t_{DR}	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of the $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} or t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle, then t_{DH} = 20 ns for –12 parts and t_{DH} = –25 ns for –15 parts.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1486 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All voltages are referenced to ground.
11. Applies to both interrupt pins when the alarms are set to pulse.
12. Interrupt output occurs within 100 ns on the alarm condition existing.
13. Both $\overline{INTA}$ and $\overline{INTB}$(INTB) are open drain outputs.

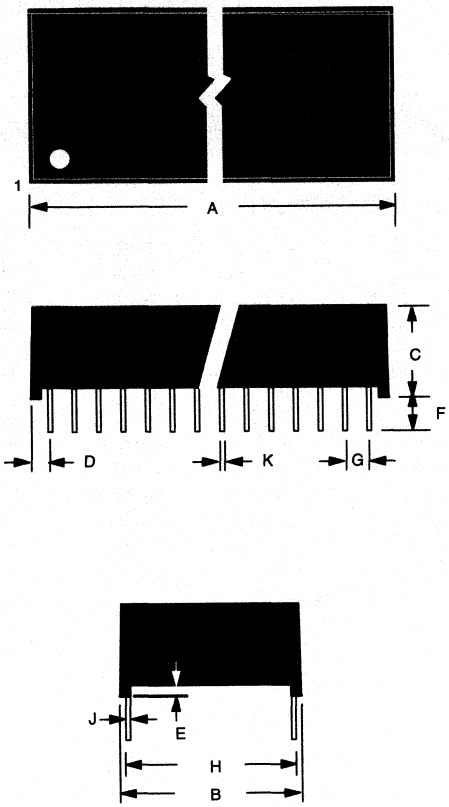
AC TEST CONDITIONS

Input Levels:	0V to 3V
Transition Times:	5 ns

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns.

DS1486 32 PIN 740 MIL MODULE



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.720	1.740
MM	43.69	44.20
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.090	0.120
MM	2.29	3.05
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

3

DALLAS SEMICONDUCTOR

DS1585/DS1587
Serialized Real Time Clocks

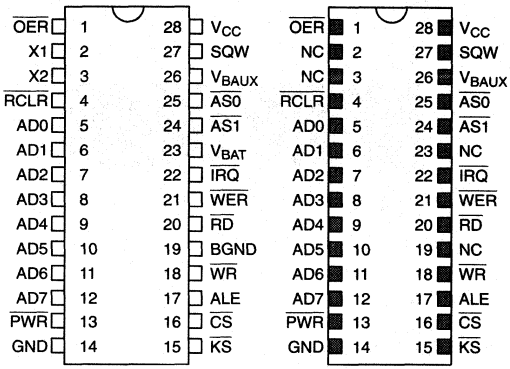
FEATURES
Incorporates industry standard DS1287 PC clock plus enhanced features:

- 64-bit Silicon serial number
- Power control circuitry supports system power on from date/time alarm or key closure
- 114 bytes user NVRAM
- 8K bytes additional NVRAM
- Auxiliary battery input
- RAM clear input
- Century register
- 32 KHz output for power management
- Supports Intel timing mode
- Compatible with existing BIOS for original DS1287 functions
- Available as chip (DS1585) or stand-alone module (DS1587) with embedded lithium battery and crystal

ORDERING INFORMATION

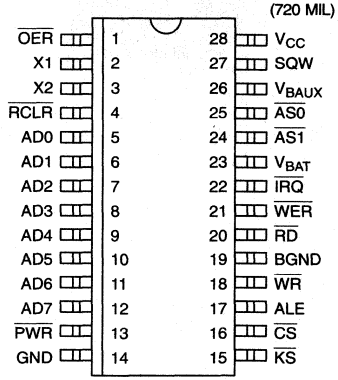
DS1585	RTC Chip; 28–pin DIP
DS1585S	RTC Chip; 28–pin SOIC
DS1587	RTC Module; 28–pin DIP

PIN ASSIGNMENT



DS1585 28-PIN DIP (600 MIL)

DS1587 28-PIN ENCAPSULATED PACKAGE (720 MIL)



DS1585S 28-PIN SOIC (330 MIL)

PIN DESCRIPTION

OER	-	RAM output enable
X1	-	Crystal input
X2	-	Crystal output
RCLR	-	RAM clear input
AD0-AD7	-	Mux'ed address/data bus
PWR	-	Power on interrupt output (open drain)
KS	-	Kickstart input
CS	-	RTC Chip select input
ALE	-	RTC address strobe
WR	-	RTC write data strobe
RD	-	RTC read data strobe
WER	-	RAM write data strobe
IRQ	-	Interrupt request output (open drain)
AS1	-	RAM upper address strobe
AS0	-	RAM lower address strobe
SQW	-	Square wave output
V_{CC}	-	+5V supply
GND	-	Ground
V_{BAT}	-	Battery + supply
V_{BAUX}	-	Auxiliary battery supply
BGND	-	Battery ground

DESCRIPTION

The DS1585/DS1587 are RAMified real–time clocks (RTC's) designed as upward-compatible successors to the industry standard DS1287, DS1387, DS1487, and DS1488 PC real–time clocks. As such, these devices incorporate a number of enhanced features including a silicon serial number, power on/off control circuitry, 114 bytes of user NVSRAM, and 8K bytes of additional NVSRAM.

Each DS1585/DS1587 is individually manufactured with a unique 64-bit serial number. The serial number is written by laser and tested at Dallas to insure that no two devices are alike. As a result, the serial number can be used to electronically identify a system for purposes such as establishment of a network node address, or for maintenance. Blocks of available numbers from Dallas Semiconductor can be reserved by the customer.

The Serialized RTC's also incorporate power control circuitry which allows the system to be powered on via the keyboard or by a time and date (wake up) alarm. The $\overline{PWR}$ output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS1585 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. The DS1587 incorporates the DS1585 chip, a 32.768 KHz crystal, and a lithium battery in a complete, self-contained timekeeping module. The entire unit is fully tested at Dallas such that a minimum of 10 years of timekeeping and data retention in the absence of V_{CC} is guaranteed.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1585/DS1587. The following paragraphs describe the function of each pin.

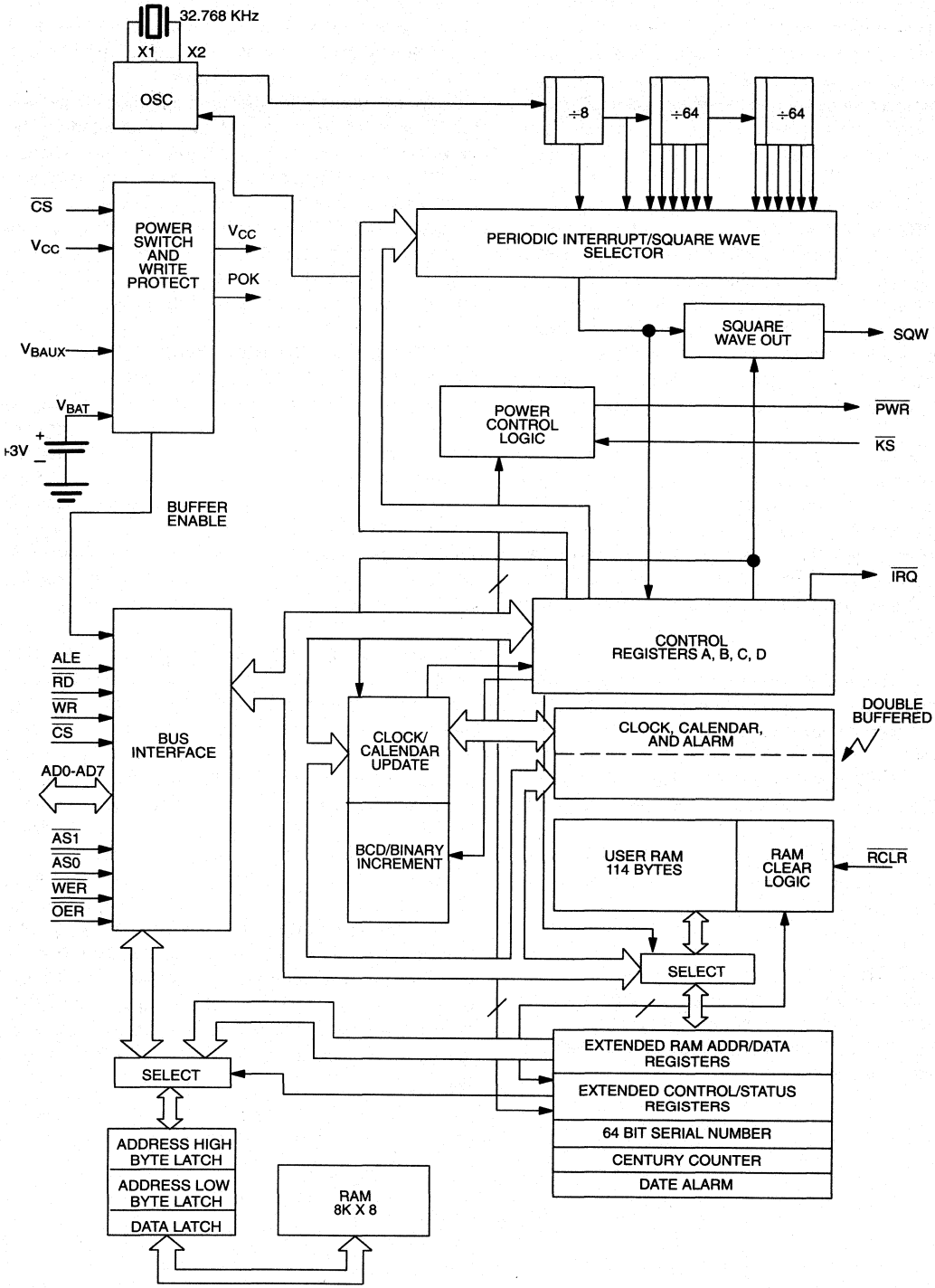
SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to lithium battery connected either to the V_{BAT} pin or V_{BAUX} pin in the case of the DS1585, or to the internal lithium battery in the case of the DS1587. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real–time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. A 32 KHz SQW signal is output when SQWE=1 and the Enable 32 KHz (E32K=1) in extended register 04BH and V_{CC} is above 4.25V. A 32 KHz square wave is also available when V_{CC} is less than 4.25 volts typical if E32K=1, SQWE=1, ABE=1, and voltage applied to V_{BAUX}.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1585/DS1587 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, $\overline{AS0}$, or $\overline{AS1}$, at which time the DS1585/DS1587 latches the address from AD0 to AD7. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ or $\overline{WER}$ pulses. In a read cycle the DS1585/DS1587 outputs 8 bits of data during the latter portion of the $\overline{RD}$ or $\overline{OER}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ or $\overline{OER}$ transitions high.

DS1585/DS1587 BLOCK DIAGRAM Figure 1



ALE (RTC Address Strobe Input) - A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1585/DS1587.

$\overline{RD}$ (RTC Read Input) - $\overline{RD}$ identifies the time period when the DS1585/DS1587 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

$\overline{WR}$ (RTC Write Input) -The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed clock register.

$\overline{CS}$ (RTC Chip Select Input) - The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1585/DS1587 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place with ALE asserted but without asserting $\overline{CS}$ will latch addresses. However, no data transfer will occur.

$\overline{IRQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS1585/DS1587 that can be tied to the interrupt input of a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application software must clear all enabled flag bits contributing to $\overline{IRQ}$'s active state.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ pin is an open drain output and requires an external pull-up resistor.

$\overline{AS0}$ (RAM Address Strobe Zero) - The rising edge of $\overline{AS0}$ latches the lower eight bits of the 8K x 8 extended RAM address.

$\overline{AS1}$ (RAM Address Strobe One) - The rising edge of $\overline{AS1}$ latches the upper five bits of the 8K x 8 extended RAM address.

$\overline{OER}$ (RAM Output Enable) - $\overline{OER}$ is active low and identifies the time period when the DS1585/DS1587 drives the bus with 8K x 8 extended RAM read data.

$\overline{WER}$ (RAM Write Enable) - $\overline{WER}$ is an active low signal and defines the time period during which data is written to the 8K x 8 extended RAM portion of the DS1585/DS1587.

$\overline{PWR}$ - Power On Output; open drain; active low. The $\overline{PWR}$ pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the DS1585/DS1587, $\overline{PWR}$ may be automatically activated from a Kickstart input via the $\overline{KS}$ pin or from a Wake Up interrupt. Once the system is powered on, the state of the $\overline{PWR}$ pin can be controlled via bits in the Dallas registers.

$\overline{KS}$ - Kickstart input, active low. When V_{CC} is removed from the DS1585/DS1587, the system can be powered on in response to an active low transition on the $\overline{KS}$ pin, as might be generated from a key closure. V_{BAUX} must be present and ABE must be set to 1 if the kickstart function is used, and the $\overline{KS}$ pin must be pulled up to the V_{BAUX} supply. Do not apply positive voltage to the $\overline{KS}$ pin that exceeds V_{BAUX} while in battery-backed mode. While V_{CC} is applied, the $\overline{KS}$ pin can be used as an interrupt input.

$\overline{RCLR}$ - RAM Clear Input; active low. If enabled by software, taking $\overline{RCLR}$ low will result in the clearing of the 114 bytes of user RAM. When enabled, $\overline{RCLR}$ can be activated whether or not V_{CC} is present.

V_{BAUX} - Auxiliary battery input required for kickstart and wake up features. Also supports clock/calendar and NVRAM function if V_{BAT} at lower voltage or not present. Standard +3 volt lithium cell or other energy source can be used. Battery voltage must be held between +2.5 and +3.7 volts for proper operation. If V_{BAUX} is not going to be used it should be grounded and auxiliary battery enable bit bank 1, register 01BH, should = 0.

(DS1585 ONLY)

X1, X2 - Connections for a standard 32.768 KHz quartz crystal, Daiwa part number DT-26S or equivalent. When ordering, request a load capacitance of 6 pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF.

V_{BAT} - Battery input for any standard 3 Volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage is set by the internal circuitry and is 4.25 volts typical. A maximum load of 1 µA at 25°C and 3.0V on V_{BAT} should be used to size the external energy source. This pin is not present on the DS1587 as the battery supply is contained within the package.

BGND - Ground for battery inputs.

POWER-DOWN/POWER-UP CONSIDERATIONS

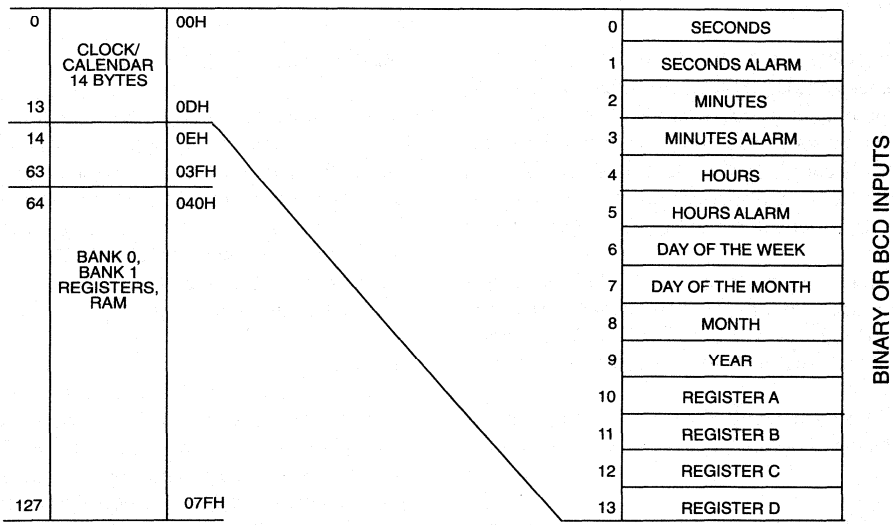
The real-time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS1585/DS1587 and reaches a level of greater than 4.25 volts, the device becomes accessible after 150 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts, the chip is internally disabled and is, therefore, write-protected. With the possible exception of the $\overline{KS}$, $\overline{PWR}$, and SQW pins, all inputs are ignored and all outputs are in a high impedance state. When the DS1585/DS1587 is in a write-protected state, V_{CC} falls below a level of approximately 3 volts, the external V_{CC} supply is switched off and either the internal lithium energy source or the auxiliary battery supplies power to the real-time clock and the RAM memory.

RTC ADDRESS MAP

The address map for the RTC registers of the DS1585/DS1587 is shown in Figure 2. The address map consists of the 14 clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and four bytes are used for control and status. All registers can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

REAL–TIME CLOCK ADDRESS MAP DS1585/DS1587 Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching will be explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The SET bit in Reg-

ister B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The four alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second use condition is to insert a "don't care" state in one or more of the four alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second. The three alarm bytes may be used in conjunction with the date alarm as described in the Wakeup/Kickstart section. The century counter will be discussed later in this text.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
00H	Seconds	0-59	00-3B	00-59
01H	Seconds Alarm	0-59	00-3B	00-59
02H	Minutes	0-59	00-3B	00-59
03H	Minutes Alarm	0-59	00-3B	00-59
04H	Hours 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours 24-Hour Mode	0-23	00-17	00-23
05H	Hours Alarm 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92 PM
	Hours Alarm 24-hr. Mode	0-23	00-17	00-23
06H	Day of Week Sunday=1	1-7	01-07	01-07
07H	Date of Month	1-31	01-1F	01-31
08H	Month	1-12	01-0C	01-12
09H	Year	0-99	00-63	00-99
BANK 1, 48H	Century	0-99	00-63	00-99
BANK 1, 49H	Date Alarm	1-31	01-1F	01-31

CONTROL REGISTERS

The four control registers; A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

NONVOLATILE RAM - RTC

The 114 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1585/ DS1587. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible when bank 0 is selected.

INTERRUPT CONTROL

The DS1585/DS1587 includes six separate, fully automatic sources of interrupt for a processor:

1. Alarm interrupt
2. Periodic interrupt
3. Update-ended interrupt
4. Wake up interrupt
5. Kickstart interrupt
6. RAM clear interrupt

The conditions which generate each of these independent interrupt conditions are described in greater detail elsewhere in this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are a total of six bits including three bits in Register B and three bits in Extended Register B which enable the interrupts. The extended register locations are described later. Writing a logic 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ will immediately be set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits which are set remain stable throughout the read cycle. All bits which were set are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the $\overline{IRQ}$ pin will be driven low when an interrupt flag bit is set and its corresponding enable bit is also set. $\overline{IRQ}$ will be held low as long as at least one of the six possible interrupt sources has it s flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS1585/DS1587 initiated an interrupt is accomplished by reading Register C and finding IRQF=1. IRQF will remain set until all enabled interrupt flag bits are cleared to 0.

SQUARE WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768 KHz crystal tied to X1 and X2. The square wave output is enabled and disabled via the SQWE bit in Register B. If the square wave is enabled (SQWE=1), then the output frequency will be determined by the settings of the E32K bit in Extended Register B and by the RS3-0 bits in Register A. If the E32K=1, then a 32.768 KHz square wave will be output on the SQW pin regardless of the settings of RS3-0.

If E32K=0, then the square wave output frequency is determined by the RS3-0 bits. These bits control a 1-of-15 decoder which selects one of thirteen taps that divide the 32.768 KHz frequency. The RS3-0 bits establish the SQW output frequency as shown in Table 2. In addition, RS3-0 bits control the periodic interrupt selection as described below.

If SQWE=1, E32K=1, the Auxiliary Battery Enable bit (ABE, bank 1; register 04BH) is enabled, and voltage is applied to V_{BAUX} then the 32 KHz square wave output signal will be output on the SQW pin in the absence of V_{CC}. This facility is provided to clock external power management circuitry. If any of the above requirements are not met, no square wave output signal will be generated on the SQW pin in the absence of V_{CC}.

OSCILLATOR CONTROL BITS

When the DS1587 timekeeping module with crystal and lithium battery is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system.

A pattern of 01X in the DV2, DV1, and DV0, bits respectively, will turn the oscillator on and enable the countdown chain. Note that this is different than the DS1287, which required a pattern of 010 in these bits. DV0 is now a "don't care" because it is used for selection between register banks 0 and 1.

A pattern of 11X will turn the oscillator on, but the oscillator's countdown chain will be held in reset, as it was in the DS1287. Any other bit combination for DV2 and DV1 will keep the oscillator off.

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3-0 bits in Register A which select the square wave frequency (see Table 2). Changing the bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The Serialized RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

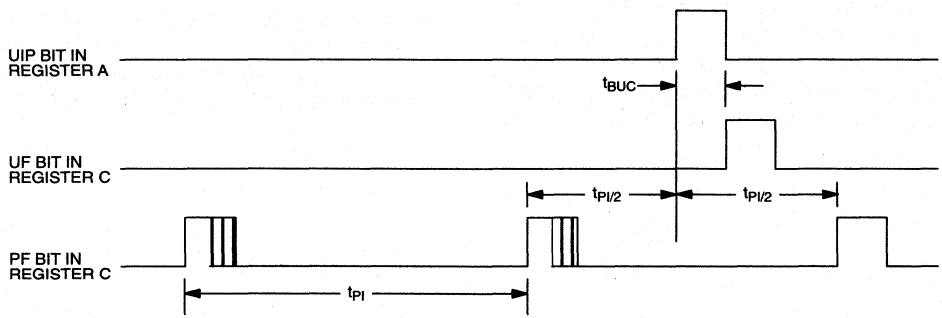
PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

EXT. REG. B E32K	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625 ms	256 Hz
0	0	0	1	0	7.8125 ms	128 Hz
0	0	0	1	1	122.070 µs	8.192 KHz
0	0	1	0	0	244.141 µs	4.096 KHz
0	0	1	0	1	488.281 µs	2.048 KHz
0	0	1	1	0	976.5625 µs	1.024 KHz
0	0	1	1	1	1.953125 ms	512 Hz
0	1	0	0	0	3.90625 ms	256 Hz
0	1	0	0	1	7.8125 ms	128 Hz
0	1	0	1	0	15.625 ms	64 Hz
0	1	0	1	1	31.25 ms	32 Hz
0	1	1	0	0	62.5 ms	16 Hz
0	1	1	0	1	125 ms	8 Hz
0	1	1	1	0	250 ms	4 Hz
0	1	1	1	1	500 ms	2 Hz
1	X	X	X	X	*	32.768 KHz

*RS3-RS0 determine periodic interrupt rates as listed for E32K=0.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within (t_{PI} / 2+t_{BUC}) to ensure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1
t_{BUC} = DELAY TIME BEFORE UPDATE CYCLE = 244 µs

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2 - These bits are defined as follows:

DV2 = Countdown Chain
1 - resets countdown chain only if DV1=1
0 - countdown chain enabled

DV1 = Oscillator Enable
0 - oscillator off
1 - oscillator on

DV0 = Bank Select
0 - original bank
1 - extended registers

A pattern of 01X is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 01X is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

Enable the interrupt with the PIE bit;

Enable the SQW output pin with the SQWE bit;

Enable both at the same time and the same rate; or

Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1585/DS1587.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1585/DS1587 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1585/DS1587 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 and the E32K bit is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified

by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 WF = WIE = 1
AF = AIE = 1 KF = KSE = 1
UF = UIE = 1 RF = RIE = 1

i.e., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE) + (WF • WIE) + (KF • KSE) + (RF • RIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 0 THROUGH BIT 3 - These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit indicates the condition of the internal battery (the battery connected to the V_{BAT} pin in the case of the DS1585) or the battery connected to V_{BAUX}, whichever is at a higher voltage. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

EXTENDED FUNCTIONS

The extended functions provided by the DS1585/DS1587 that are new to the RAMified RTC family are accessed via a software controlled bank switching scheme, as illustrated in Figure 4. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS1585/DS1587 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

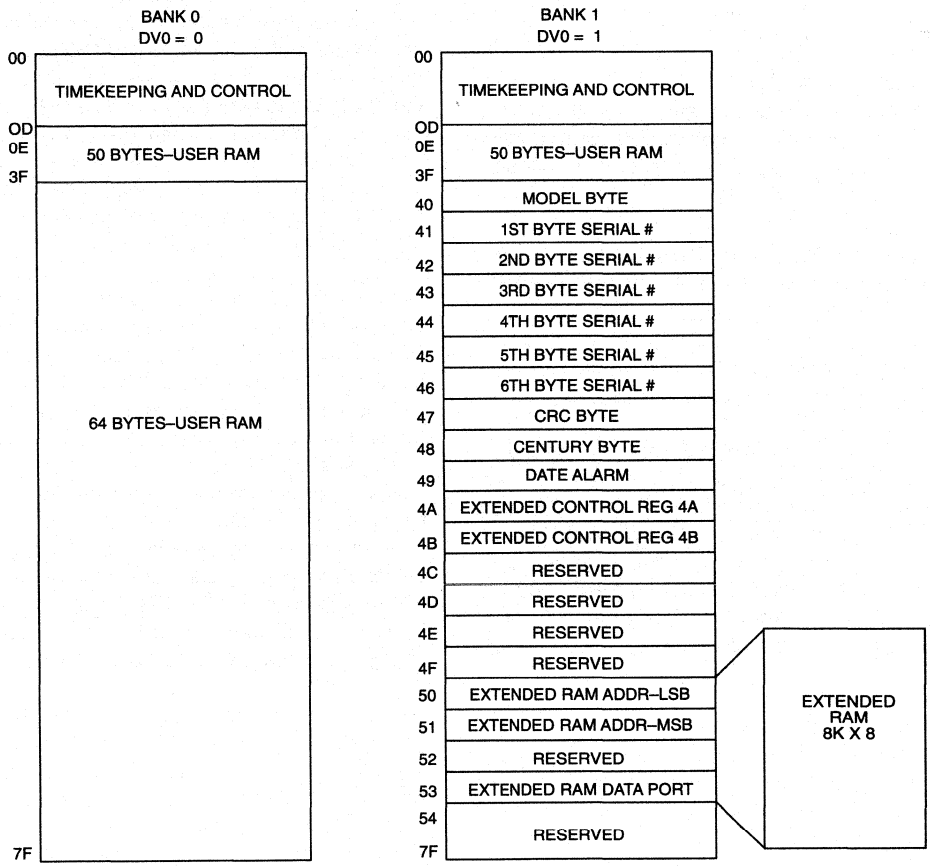
When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers which provide control and status for the extended functions will be accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

1. Silicon Revision byte
2. Serial Number
3. Century counter
4. 8 Kbyte Extended RAM access
5. Auxiliary Battery Control/Status
6. Wake Up
7. Kickstart
8. RAM Clear Control/Status

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and will return a 0 if read.

3

DS1585/DS1587 EXTENDED REGISTER BANK DEFINITION Figure 4



SILICON SERIAL NUMBER

A unique 64-bit lasered serial number is located in bank 1 registers 40H - 47H. This serial number is divided into three parts. The first byte in register 40H contains a model number to identify the device type and revision of the DS1585/DS1587. Registers 41H-46H contain a unique binary number. Register 47H contains a CRC byte used to validate the data in registers 40H-46H. All 8 bytes of the serial number are read only registers.

The DS1585/DS1587 is manufactured such that no two devices will contain an identical number in locations 41H-47H. Blocks of numbers for these locations can be reserved by the customer. Contact Dallas Semiconductor for special ordering information for DS1585/DS1587's with reserved blocks of serial numbers.

CENTURY COUNTER

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

8K X 8 RAM

The DS1585/DS1587 provides 8K x 8 of on-chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by the internal power OK signal (POK) generated from the write protect circuitry. The POK signal becomes active at 4.25 volts (typical).

The on-chip 8K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7-AD0. Access to the SRAM is controlled by three on-chip latch registers. Two registers are used to hold the SRAM address, and the third register is used to hold read/write data. The SRAM address space is from 0000H to 1FFFH. A direct hardware interface to the SRAM as well as indirect access under software control is supported.

The hardware access uses four control signals, $\overline{AS0}$, $\overline{AS1}$, $\overline{OER}$, and $\overline{WER}$ to access the extended SRAM. This access mode is identical to that supported by the DS1385/DS1387 and DS1485/DS1488. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ($\overline{AS0}$) and Address Strobe 1 ($\overline{AS1}$) signals. $\overline{AS0}$ is used to latch the lower 8-bits of address, and $\overline{AS1}$ is used to latch the upper 5-bits of address. It is necessary to meet the setup and hold times given in the Electrical Specifications with valid address information in order to properly latch the address. If the upper or lower order address is correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation in the hardware access method requires valid data to placed on the bus (AD7-AD0) followed by the activation of the Write Enable RAM ($\overline{WER}$) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Output Enable RAM ($\overline{OER}$) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met. The $\overline{WER}$ and $\overline{OER}$ signals should never be active at the same time. In addition, access to the clock/calendar registers and user RAM (via $\overline{CS}$) must not be attempted when the 8K x 8 RAM is being accessed. The RAM is enabled when either $\overline{WER}$ or $\overline{OER}$ is active. $\overline{CS}$ is only used for the access of the clock calendar registers (including the extended Dallas registers) and the 114 bytes of user RAM.

The software method allows access to the 8K x 8 RAM via three of the Dallas registers shown in Figure 2. The Dallas registers in bank 1 must first be selected by setting the DV0 to 1 in Register A. The 13-bit address of the RAM location to be accessed must first be loaded into the two RAM address registers located at 50H and 51H. The least significant address byte should be written to location 50H, and the most significant 5 bits (right-justified) should be loaded in location 51H. Data in the addressed location may be read by performing a read operation from location 53H, or written by performing a write operation to location 53H. Data in any addressed location may be read or written repeatedly without changing the address in locations 50H, 51H.

With the software method, the extended RAM may be accessed using only the control signals assigned to the clock/calendar and 114 byte user RAM; namely, ALE, $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$. As a result, the RAM control signals ($\overline{AS1}$, $\overline{AS0}$, $\overline{WER}$, and $\overline{OER}$) do not have to be used and should be tied to their inactive levels.

AUXILIARY BATTERY

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS1585/DS1587's kickstart, wake up, and SQW output features in the absence of V_{CC}. This power source must be available in order to use these auxiliary features when no V_{CC} is applied to the device.

The Auxiliary Battery Enable (ABE; bank 1, register 04BH) bit in extended control register B is used to turn on and off the auxiliary battery for the above functions in the absence of V_{CC}. When set to a 1, V_{BAUX} battery power is enabled, and when cleared to 0, V_{BAUX} battery power is disabled to these functions. In the DS1587, this bit is shipped from the factory cleared to 0.

In the DS1585, this auxiliary battery may be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS1585 is to be backed-up using a single battery with the auxiliary features enabled, then V_{BAUX} should be used and connected to V_{BAT}. If V_{BAUX} is not to be used, it should be grounded and ABE should be cleared to 0.

WAKE UP/KICKSTART

The DS1585/DS1587 incorporates a wake up feature which can power the system on at a pre-determined date through activation of the $\overline{PWR}$ output pin. In addition, the kickstart feature can allow the system to be powered up in response to a low going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin. As a result, system power may be applied upon such events as a key closure, or modem ring detect signal. In order to use either the wake up or the kickstart features, the DS1585/DS1587 must have an auxiliary battery connected to the V_{BAUX} pin and the oscillator must be running and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the $\overline{PWR}$ pin will not be driven low in response to a kickstart or wakeup condition, while in battery-backed mode.

The wake up feature is controlled through the Wake up Interrupt Enable bit in extended control register B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake up feature, clearing WIE to 0 disables it. Similarly, the kickstart feature is controlled through the Kickstart Interrupt Enable bit in extended control register B (KSE, bank 1, 04BH).

A wake up sequence will occur as follows: When wake up is enabled via WIE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar will monitor the current date for a match condition with the date alarm register (bank 1, register 049H). In conjunction with the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake up will occur at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm will occur regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the $\overline{PWR}$ pin will automatically be driven low. This output can be used to turn on the main system power supply which provides V_{CC} voltage to the DS1585/DS1587 as well as the other major components in the system. Also at this time, the Wake Up flag (WF, bank 1, register 04AH) will be set, indicating that a wake up condition has occurred.

A kickstart sequence will occur when kickstarting is enabled via KSE = 1. While the system is powered down, the $\overline{KS}$ input pin will be monitored for a low going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line will be pulled low, as it is for a wake up condition. Also at this time, the Kickstart Flag (KF, bank 1, register 04AH) will be set, indicating that a kickstart condition has occurred.

The timing associated with both the wake up and kickstarting sequences is illustrated in the Wake Up / Kickstart Timing Diagram in the Electrical Specifications section of this data sheet. The timing associated with these functions is divided into 5 intervals, labeled 1-5 on the diagram.

The occurrence of either a kickstart or wake up condition will cause the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS1585/DS1587 V_{CC} pin rises above the V_{BAT} level before the power on timeout period (t_{POTO}) expires, then $\overline{PWR}$ pin will remain at the active low level. If V_{CC} does not rise above V_{BAT} voltage in this time, then the $\overline{PWR}$ output pin will be turned off and will return to its high impedance level. In this event, the $\overline{IRQ}$ pin will also remain tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power on sequence will remain set until cleared by software during a subsequent system power on.

If V_{CC} is applied within the timeout period, then the system power on sequence will continue as shown in intervals 2-5 in the timing diagram. During interval 2, $\overline{PWR}$ will remain active and $\overline{IRQ}$ will be driven to its active low level, indicating that either WF or KF was set in initiating the power on. In the diagram $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit will be automatically cleared to 0 in response to a successful power on. The $\overline{PWR}$ line will remain active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing zeroes to both of these control bits. As long as no other interrupt within the DS1585/DS1587 is pending, the $\overline{IRQ}$ line will be taken inactive once these bits are reset. Execution of the application software may proceed. During this time, both the wake up and kickstart functions may be used to generate status and interrupts. WF will be set in response to a date, hours, and minutes match condition. KF will be set in response to a low going transition on $\overline{KS}$. If the associated interrupt enable bit is set (WIE and/or KSE) then the $\overline{IRQ}$ line will driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS1585/DS1587 may cause $\overline{IRQ}$ to be driven low. While system power is applied, the on chip logic will always attempt to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake up or kickstart.

The system may be powered down under software control by setting the PAB bit to a logic 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ}$ output pin will be placed in a high impedance state when V_{CC} goes below V_{PF}. If the system is to be again powered on in response to a wake up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and nonvolatile RAM is in effect, $\overline{PWR}$ and $\overline{IRQ}$ are tri-stated, and monitoring of wake up and kickstart takes place.

RAM CLEAR

The DS1585/DS1587 provides a RAM clear function for the 114 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V_{CC} pin.

The RAM clear function is enabled or disabled via the RAM Clear Enable bit (RCE; bank 1, register 04BH). When this bit is set to a logic 1, the 114 bytes of user RAM will be cleared (all bits set to 1) when an active low transition is sensed on the $\overline{RCLR}$ pin. This action will have no effect on either the clock/calendar settings or upon the contents of the 8K x 8 Extended RAM. The RAM clear Flag (RF, bank 1, register 04BH) will be set when the RAM clear operation has been completed. If V_{CC} is present at the time of the RAM clear and RIE=1, the $\overline{IRQ}$ pin will also be driven low upon completion. The interrupt condition can be cleared by writing a zero to the RF bit. The $\overline{IRQ}$ pin will then return to its inactive high level provided there are no other pending interrupts. Once the $\overline{RCLR}$ pin is activated, all read/write accesses are locked out for a minimum recover time, specified as t_{REC} in the Electrical Characteristics section.

When RCE is cleared to zero, the RAM clear function is disabled. The state of the $\overline{RCLR}$ pin will have no effect on the contents of the user RAM, and transitions on the $\overline{RCLR}$ pin have no effect on RF.

EXTENDED REGISTERS

Two extended control registers are provided supply controls and status information for the extended features offered by the DS1585/DS1587. These are designated as extended control registers A and B and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows:

EXTENDED CONTROL REGISTER 4A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	*	*	PAB	RF	WF	KF

VRT2 - This status bit gives the condition of the auxiliary battery. It is set to a logic 1 condition when the external lithium battery is connected to the V_{BAUX}. If this bit is read as a logic 0, the external battery should be replaced.

INCR - Increment in Progress status bit. This bit is set to a 1 when an increment is in progress to the time/date registers and the alarm checks are being made. INCR will be set to a 1 at 122 µs before the update cycle starts and will be cleared to 0 at the end of each update cycle.

PAB - Power Active Bar control bit. When this bit is 0, the $\overline{PWR}$ pin is in the active low state. This bit can be written to a logic 1 or 0 by the user. If either WF AND WIE = 1 OR KF AND KSE = 1, the PAB bit will be cleared to 0.

RF - Ram Clear Flag. This bit will be set to a logic 1 when a high to low transition occurs on the $\overline{RCLR}$ input pin if RCE=1. The RF bit is cleared by writing it to a logic 0. This bit can also be written to a logic 1 to force an interrupt condition.

WF - Wake up Alarm Flag - This bit is set to 1 when a wake up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

KF - Kickstart Flag - This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

EXTENDED CONTROL REGISTER 4B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32K	*	RCE	*	RIE	WIE	KSE

ABE - Auxiliary Battery Enable. This bit when written to a logic 1 will enable the V_{BAUX} pin for extended functions. On the DS1587 with an embedded lithium cell, this bit is shipped from the factory set to a logic 0.

E32K - Enable 32.768 KHz output. This bit when written to a logic 1 will enable the 32.768 KHz oscillator frequency to be output on the SQW pin provided SQWE=1.

RCE - RAM Clear Enable bit. When set to a 1, this bit enables a low level on $\overline{RCLR}$ to clear all 114 bytes of user RAM. When RCE = 0, $\overline{RCLR}$ and the RAM clear function are disabled.

RIE - Ram Clear Interrupt Enable. When RIE is set to a 1, the $\overline{IRQ}$ pin will be driven low when a RAM clear function is completed.

WIE - Wake Up Alarm Interrupt Enable. When V_{CC} voltage is absent and WIE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a wake up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If WIE is set while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to WF being set to 1. When WIE is cleared to a 0, the WF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

KSE - Kickstart Interrupt Enable. When V_{CC} voltage is absent and KSE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If KSE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to KF being set to 1. When KSE is cleared to a 0, the KF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

* Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no effect on operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to 7.0V
Operating Temperature	0°C to 70°C
Storage Temperature DS1587	–40°C to +70°C
Storage Temperature DS1585	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	9
Auxiliary Battery Voltage	V_{BAUX}	2.5		3.7	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

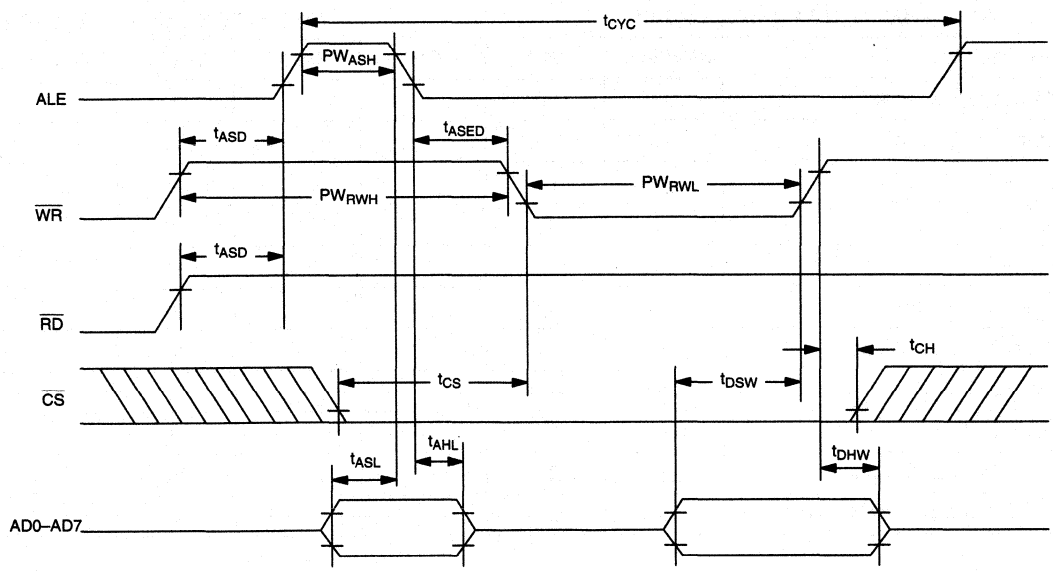
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		35	50	mA	2
Standby Current $\overline{CS}$ = V_{CC} -0.3V	I_{CC2}		1	5.0	mA	6
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	3, 4
Output @ 2.4V	I_{OH}	-1.0			mA	1, 4
Output @ 0.4V	I_{OL}			2.0	mA	1
Power Fail Trip Point	V_{PF}		4.25		V	1
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			10.0	mA	1

RTC AC TIMING CHARACTERISTICS

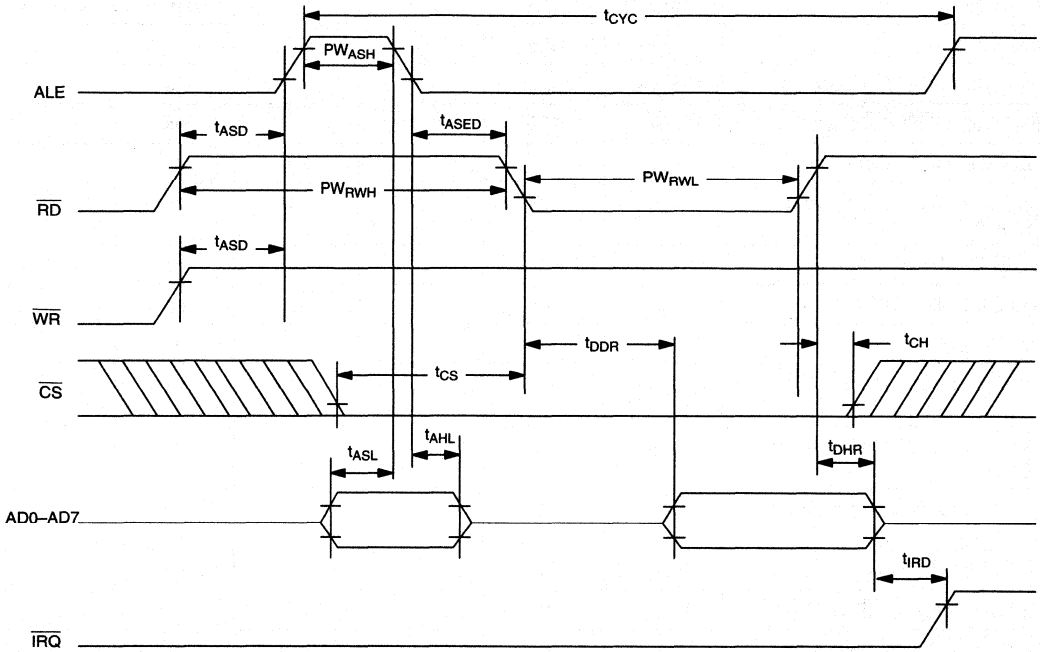
(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{OWL}	125			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{RWH}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	5
Data Setup Time	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

DS1585/DS1587 BUS TIMING FOR WRITE CYCLE TO RTC



DS1585/DS1587 BUS TIMING FOR READ CYCLE TO RTC



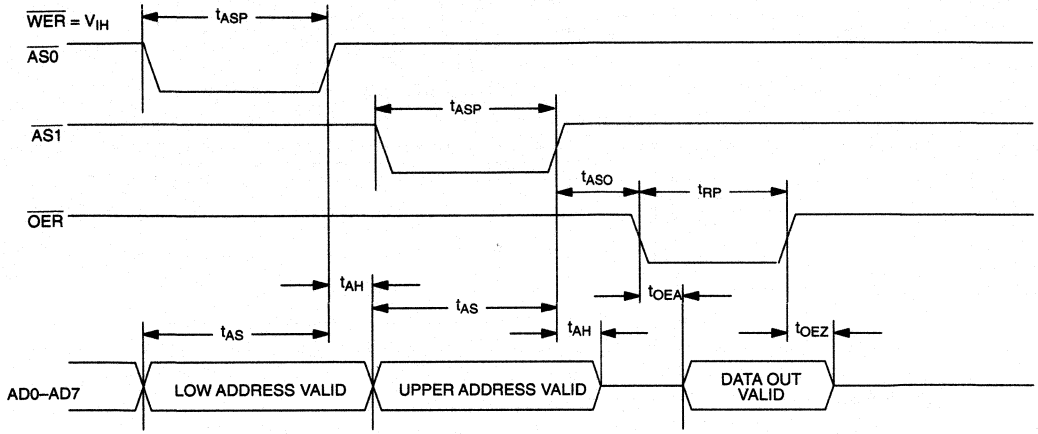
NOTE:
Input Levels=0 volts and 3.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

8K X 8 AC TIMING CHARACTERISTICS

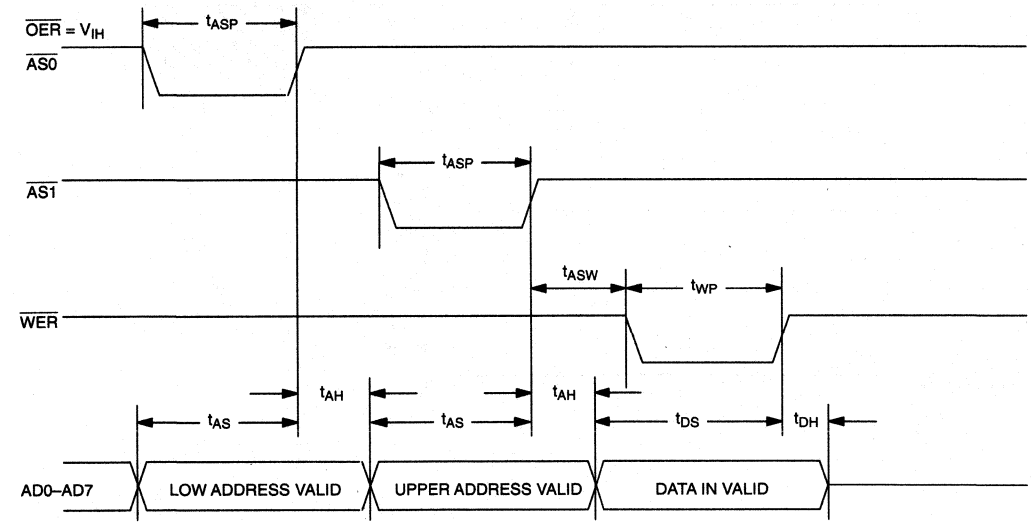
(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	50			ns	
Address Hold Time	t_{AH}	0			ns	
Data Setup Time	t_{DS}	75			ns	
Data Hold Time	t_{DH}	0			ns	
Output Enable Access Time	t_{OEA}			200	ns	7
Write Pulse Width	t_{WP}	125			ns	
$\overline{OER}$ to Output in High Z	t_{OEZ}			50	ns	
$\overline{OER}$ Pulse Width	t_{RP}	200			ns	
$\overline{AS0}$, $\overline{AS1}$ Pulse Width	t_{ASP}	75			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{OER}$ Low	t_{ASO}	20			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{WER}$ Low	t_{ASW}	20			ns	

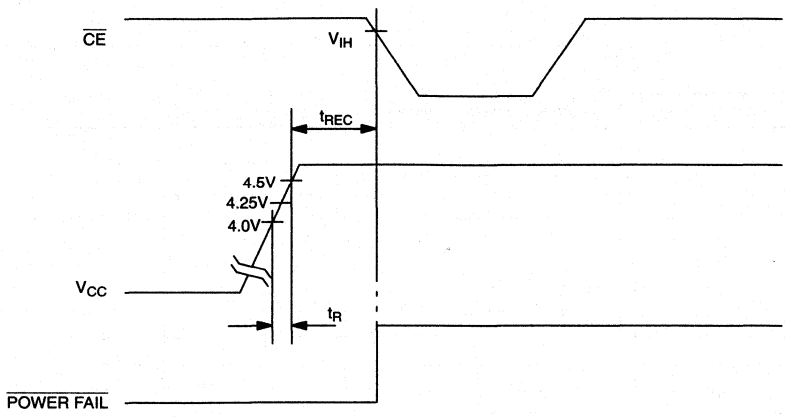
BUS TIMING FOR READ CYCLE TO 8K X 8 NV SRAM



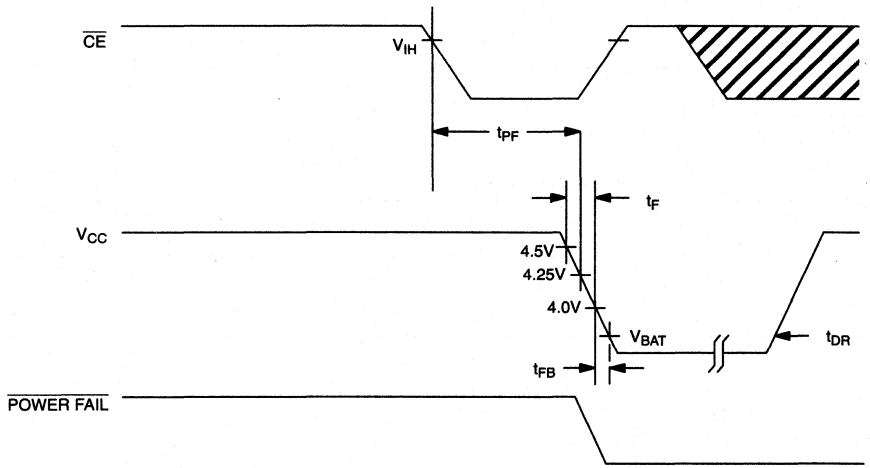
BUS TIMING FOR WRITE CYCLE TO 8K X 8 SRAM



POWER-UP CONDITION



POWER-DOWN CONDITION



POWER-UP POWER-DOWN TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \leq V_{CC} \leq 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \leq V_{CC} \leq 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \geq V_{CC} \geq 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	8

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

(t_A = 25°C)

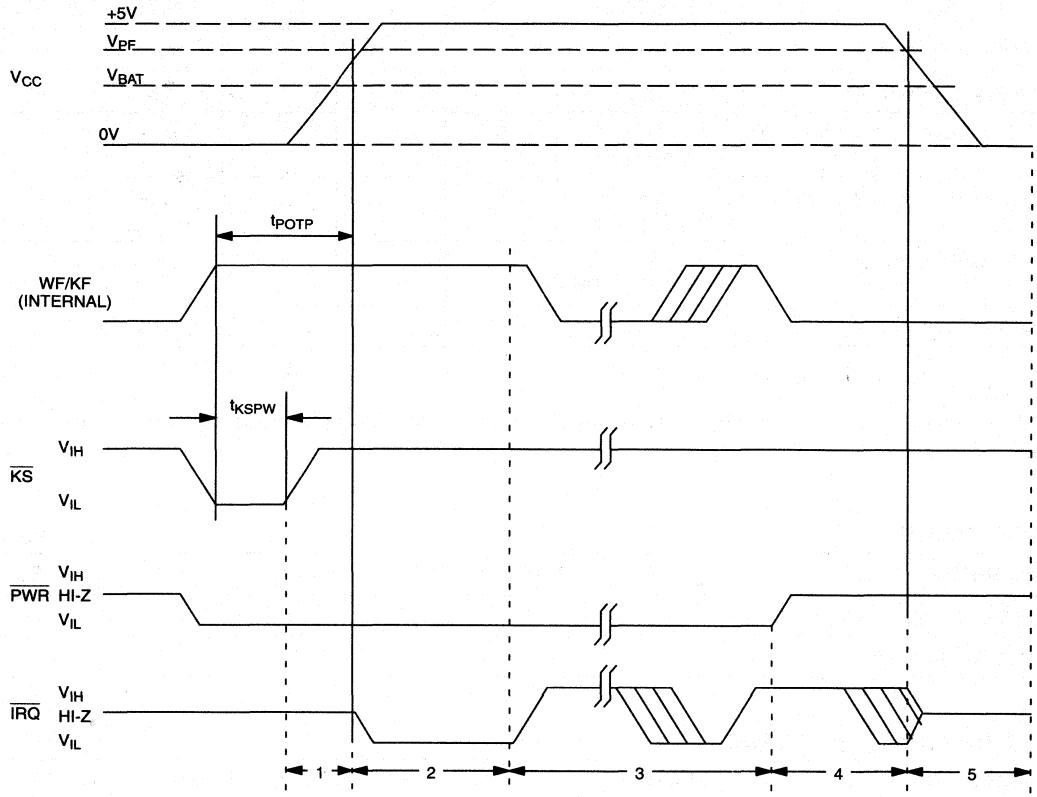
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

WAKE UP/KICKSTART TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t_{KSPW}	2			µs	
Wake up/Kickstart Power On Timeout	t_{POTO}	2			seconds	10

WAKE UP/KICKSTART TIMING



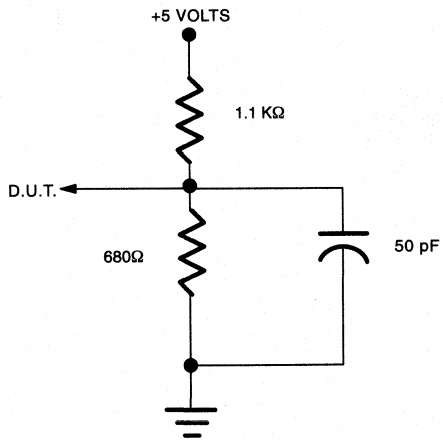
NOTE:

Time intervals shown above are referenced in Wake up/Kickstart section.

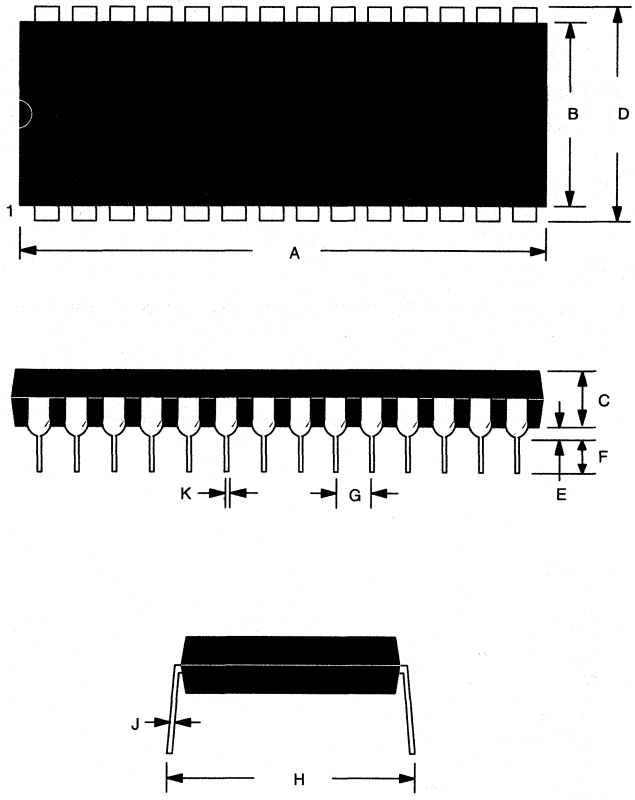
NOTES:

1. All voltages are referenced to ground.
2. All outputs are open.
3. Applies to the AD0-AD7 pins, and the SQW pin when each is in the high impedance state.
4. The $\overline{IRQ}$ pin is open drain.
5. Measured with a load as shown in Figure 5.
6. All other inputs at CMOS levels.
7. Measured with a load as shown in Figure 5.
8. The real-time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
9. Applies to DS1585 only.
10. Wake up/Kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.

OUTPUT LOAD Figure 5

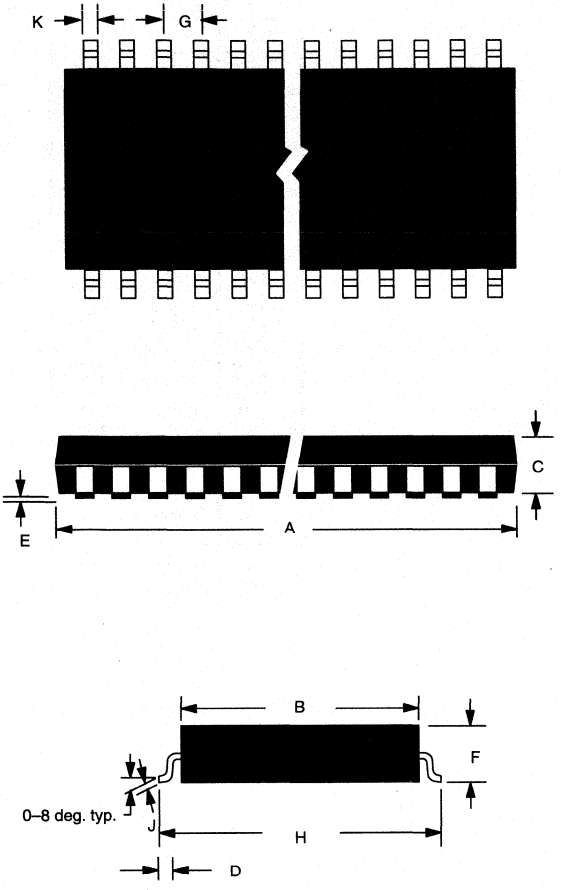


DS1585 28–PIN DIP



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.445	1.470
MM	36.70	37.34
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

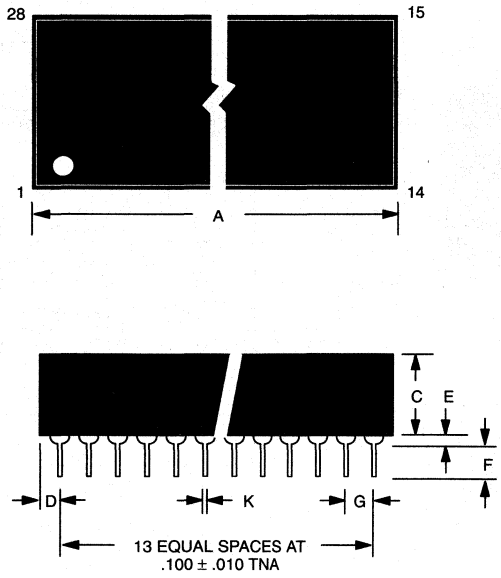
DS1585S 28–PIN SOIC



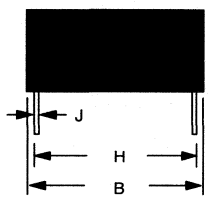
PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	0.706	0.728
MM	17.93	18.49
B IN.	0.338	0.350
MM	8.58	8.89
C IN.	0.086	0.110
MM	2.18	2.79
D IN.	0.020	0.050
MM	0.58	1.27
E IN.	0.002	0.014
MM	0.05	0.36
F IN.	0.090	0.124
MM	2.29	3.15
G IN.	0.050	BSC
MM	1.27	
H IN.	0.460	0.480
MM	11.68	12.19
J IN.	0.006	0.013
MM	0.15	0.33
K IN.	0.014	0.020
MM	0.36	0.51

3

DS1587 28 PIN 720 MIL MODULE



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



NOTE: PINS 2, 3, 19 AND 23 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

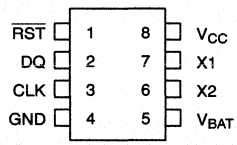
DS1602
Elapsed Time Counter

3

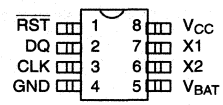
FEATURES

- Two 32–bit counters keep track of real time and elapsed time
- Counters keep track of seconds for over 125 years
- Battery powered counter counts seconds from the time battery is attached until V_{BAT} is less than 2.5 volts
- V_{CC} powered counter counts seconds while V_{CC} is above 4.25 volts and retains the count in the absence of V_{CC} under battery backup power
- Clear function resets selected counter to zero
- Read/Write serial port affords low pin count
- Maximum current drain of less than 1 µA from V_{BAT} pin when serial port is disabled
- One byte protocol defines read/write, counter address and software clear function
- 8–pin DIP or optional 8–pin SOIC
- Operating temperature range of -40°C to +85°C
- Reduced performance operation down to V_{CC} = 2.5V

PIN ASSIGNMENT



DS1602
8–PIN DIP (300 mil)



DS1602
8–PIN SOIC (200 mil)

PIN DESCRIPTION

$\overline{RST}$	-	Reset
CLK	-	Clock
DQ	-	Data input/output
GND	-	Ground
X1, X2	-	Crystal inputs
V_{BAT}	-	+ Battery input
V_{CC}	-	+5 volts

DESCRIPTION

The DS1602 is a real time clock/elapsed time counter designed to count seconds when V_{CC} power is applied and continually count seconds under battery backup power with an additional counter regardless of the condition of V_{CC}. The continuous counter can be used to derive time of day, week, month, and year by using a software algorithm. The V_{CC} powered counter will automatically record the amount of time that V_{CC} power is applied. This function is particularly useful in determining the operational time of equipment in which the DS1602 is used. Alternatively, this counter can also be used under software control to record real time events. Communication to and from the DS1602 takes place via a 3–wire serial port. A one byte protocol selects read/write functions, counter clear functions and oscillator trim. A low cost 32.768 KHz crystal attaches directly to the X1 and X2 pins. If battery powered only operation is desired, the V_{BAT} pin must be grounded and the V_{CC} pin must be connected to the battery.

OPERATION

The main elements of the DS1602 are shown in Figure 1. As shown, communications to and from the elapsed time counter occur over a 3–wire serial port. The port is activated by driving $\overline{RST}$ to a high state. With $\overline{RST}$ at high level 8 bits are loaded into the protocol shift register providing read/write, register select, register clear, and oscillator trim information. Each bit is serially input on the rising edge of the clock input. After the first eight clock cycles have loaded the protocol register with a valid protocol additional clocks will output data for a read or input data for a write. V_{CC} must be present to access the DS1602. If $V_{CC} < V_{BAT}$ the DS1602 will go into a battery backup mode which disables the serial port to conserve battery capacity. For battery only operations, the V_{BAT} pin must be grounded and the V_{CC} pin must be connected to the battery. This will keep the DS1602 out of battery backup mode. Battery powered operation down to 2.5V is possible with reduced speed performance on the serial port.

PROTOCOL REGISTER

The protocol bit definition is shown in Figure 2. Valid protocols and the resulting actions are shown in Table 1. Each data transfer to the protocol register designates what action is to occur. As defined, the MSB (bit 7 which is designated ACC) selects the 32–bit continuous counter for access. If ACC is a logical 1 the continuous counter is selected and the 32 clock cycles that follow the protocol will either read or write this counter. If the counter is being read, the contents will be latched into a different register at the end of protocol and the latched contents will be read out on the next 32 clock cycles. This avoids reading garbled data if the counter is clocked by the oscillator during a read. Similarly, if the counter is to be written, the data is buffered in a register and all 32 bits are jammed into the counter simultaneously on the rising edge of the 32nd clock. The next bit (bit 6 which is designated AVC) selects the 32 bit V_{CC} active counter for access. If AVC is a logical 1 this counter is selected and the 32 clock cycles that follow will either read or write this counter. If both bit 7 and bit 6 are written to a logic high, all clock cycles beyond the protocol are ignored and bit 5, 4, and 3 are loaded into the oscillator trim register. A value of binary 3 (011) will give a clock accuracy of ±120 seconds per month at 25°C. Increasing the binary number towards 7 will cause the real time clock to run faster. Conversely, lowering the binary number towards zero will cause the clock to run slower. Binary 000 will stop the oscillator completely. This feature can be used to conserve battery life during storage. In this mode the I_{BAT} current is reduced to 100 nA maximum. In applications where oscillator trimming is not practical or not needed, a default setting of 011 is recommended. Bit 2 of protocol (designated CCC) is used to clear the continuous counter. When set to logic 1, the continuous counter will reset to zero when $\overline{RST}$ is taken low. Bit 1 of protocol (designated CVC) is used to clear the V_{CC} active counter. When set to logical 1, the V_{CC} active counter will reset to zero when $\overline{RST}$ is taken low. Both counters can be reset simultaneously by setting CCC and CVC both to a logical 1. Bit zero of the protocol (designated RD) determines whether the 32 clocks to follow will write a counter or read a counter. When RD is set to a logical 0 a write action will follow when RD is set to a logical 1 a read action will follow. When sending the protocol, eight bits should always be sent. Sending less than 8 bits can produce erroneous results. If clearing the counters or trimming the oscillator, the data transfer can be terminated after the 8–bit protocol is sent. However, when reading or writing the counters, 32 clock cycles should always follow the protocol.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input has two functions. First, $\overline{RST}$ turns on the serial port logic which allows access to the protocol register for the protocol data entry. Second, the $\overline{RST}$ signal provides a method of terminating the protocol transfer or the 32 bit counter transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For write inputs, data must be valid during the rising edge of the clock. Data bits are output on the falling edge of the clock when data is being read. All data transfers terminate if the $\overline{RST}$ input is transitioned low and the DQ pin goes to a high impedance state. $\overline{RST}$ should only be transitioned low while the clock is high to avoid disturbing the last bit of data. All data transfers must consist of 8 bits when transferring protocol only or 8 + 32 bits when reading or writing either counter. Data transfer is illustrated in Figure 3.

DATA INPUT

Following the 8–bit protocol that inputs write mode, 32 bits of data are written to the selected counter on the rising edge of the next 32 CLK cycles. After 32 bits have been entered any additional CLK cycles will be ignored until $\overline{RST}$ is transitioned low to end data transfer and then high again to begin new data transfer.

DATA OUTPUT

Following the eight CLK cycles that input read mode protocol, 32 bits of data will be output from the selected counter on the next 32 CLK cycles. The first data bit to be transmitted from the selected 32–bit counter occurs on the falling edge after the last bit of protocol is written. When transmitting data from the selected 32 bit counter, $\overline{RST}$ must remain at high level as a transition to low level will terminate data transfer. Data is driven out the DQ pin as long as CLK is low. When CLK is high the DQ pin is tristated.

CRYSTAL SELECTION

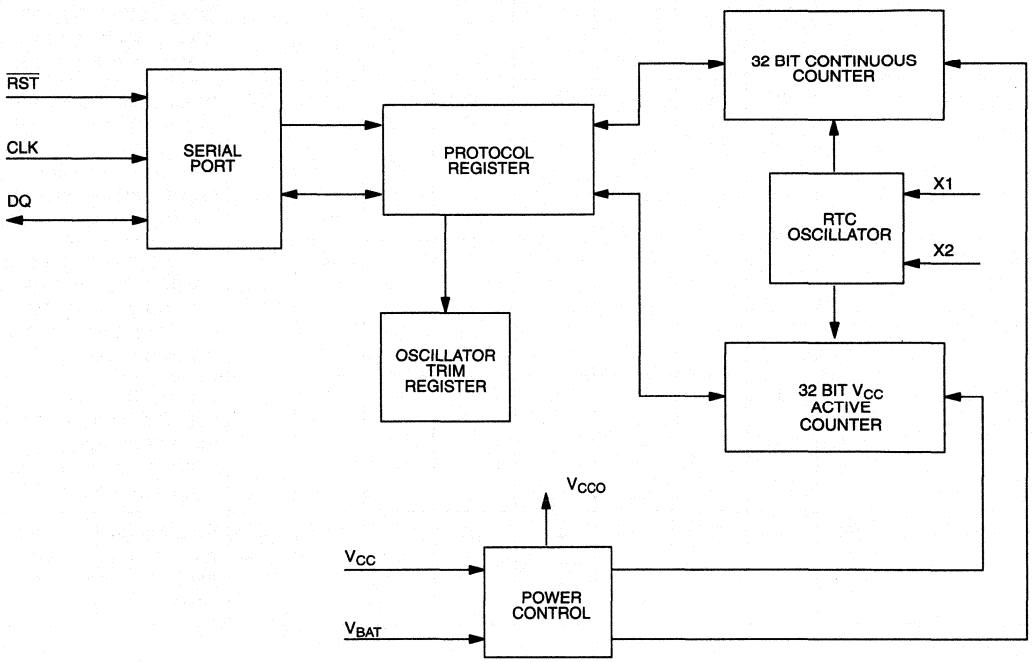
A 32.768 KHz crystal, Daiwa Part No. DT26S or Seiko Part No. DS-VT-200 or equivalent can be directly connected to the DS1602 via pins 6 and 7. The crystal selected for use should have a specified load capacitance (C_L) of 6 pF. Crystals with different load capacitance may cause the RTC oscillator to run faster or slower which effects the clock accuracy.

BATTERY SELECTION

The battery selected for use with the DS1602 should have an output voltage between 2.5 and 3.5 volts. A lithium battery of 35 mAh or greater will run the elapsed time counter for over 10 years in the absence of power. Small lithium coin cell batteries produce both the proper output voltage and have the capacity to supply the DS1602 for the useable lifetime of the equipment where they are installed.

3

DS1602 ELAPSED TIME COUNTER BLOCK DIAGRAM Figure 1



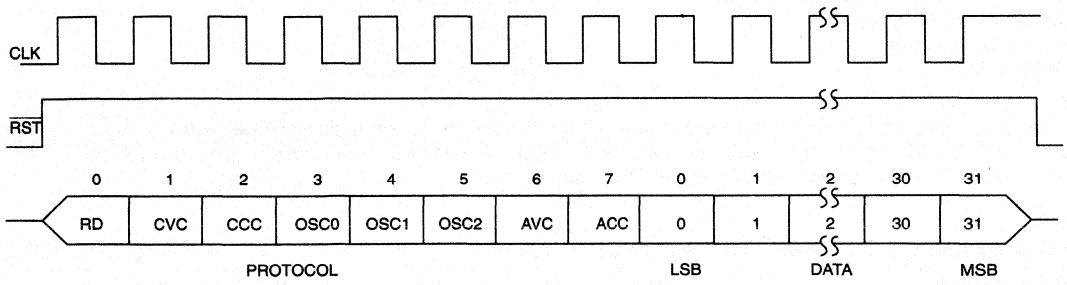
PROTOCOL BIT MAP Figure 2

7	6	5	4	3	2	1	0
ACC	AVC	OSC2	OSC1	OSC0	CCC	CVC	RD

VALID PROTOCOLS Table 1

ACTION	PROTOCOL								DESCRIPTION
	ACC	AVC	OSC2	OSC1	OSC0	CCC	CVC	RD	
Read Continuous Counter	1	0	X	X	X	X	X	1	Output continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Write Continuous Counter	1	0	X	X	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Read V_{CC} Active Counter	0	1	X	X	X	X	X	1	Output V_{CC} active counter on the 32 clocks following protocol, oscillator trim register is not updated. Counters are not reset.
Write V_{CC} Active Counter	0	1	X	X	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Clear Continuous Counter	0	0	X	X	X	1	X	X	Resets the continuous counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Clear V_{CC} Active Counter	0	0	X	X	X	X	1	X	Resets the V_{CC} active counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Set Oscillator Trim Bits	1	1	A	B	C	X	X	0	Sets the oscillator trim register to a value of ABC. Counters are unaffected.
X = Don't Care									

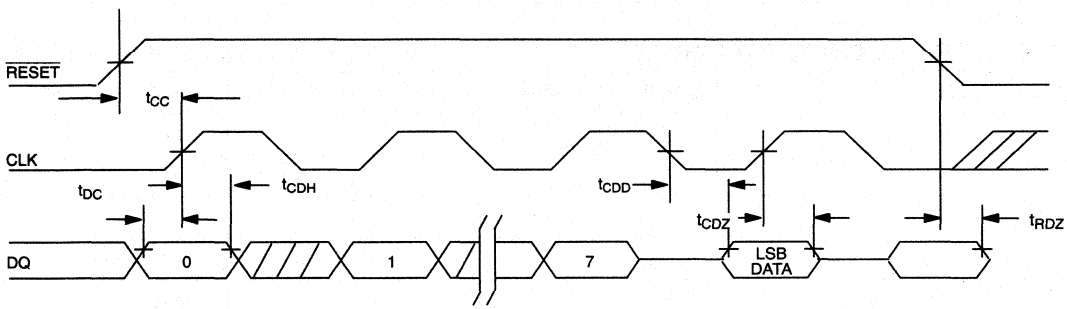
DATA TRANSFER Figure 3



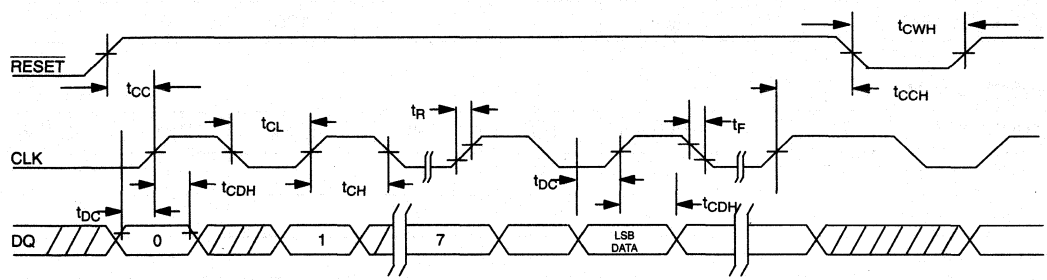
3

TIMING DIAGRAM: READ/WRITE DATA TRANSFER

READ DATA TRANSFER



WRITE DATA TRANSFER



NOTE: t_{CL}, t_{CH}, t_R, and t_F apply to both read and write data transfer.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Battery Supply Voltage	V_{BAT}	2.5	3.0	3.5	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; V_{CC} = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	-1		+1	µA	
I/O Leakage	I_{LO}	-1		+1	µA	
Logic 1 Output	V_{OH}	2.4			V	2
Logic 0 Output	V_{OL}			0.4	V	3
Active Supply Current	I_{CC}			1	mA	4
Timekeeping Current	I_{CC1}			50	µA	5
Timekeeping Current	I_{BAT}			400	nA	6
Leakage Current	I_{BATL}			100	nA	11

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Capacitance	C_X		6		pF	10

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±10%, -40°C to +85°C)

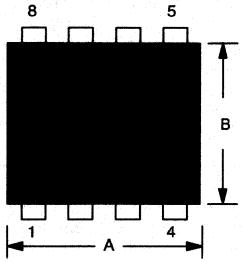
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	7
CLK to Data Hold	t_{CDH}	70			ns	7
CLK to Data Delay	t_{CDD}			200	ns	7, 8, 9
CLK Low Time	t_{CL}	250			ns	7
CLK High Time	t_{CH}	250			ns	7
CLK Frequency	f_{CLK}	DC		2.0	MHz	7
CLK Rise & Fall	t_F, t_R			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	100			ns	7
CLK to RST Hold	t_{CCH}	60			ns	7
$\overline{RST}$ Inactive Time	t_{CWH}	1			µs	7
$\overline{RST}$ Low to I/O High Z	t_{RDZ}			70	ns	7
CLK High to I/O High Z	t_{CDZ}			20	ns	7

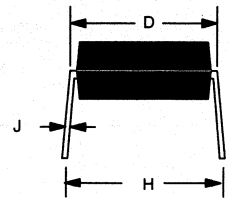
3

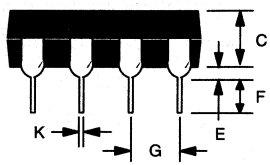
NOTES:

1. All voltages are reference to ground.
2. Logic one voltages are specified at a source current of 1 mA.
3. Logic zero voltages are specified at a sink current of 4 mA.
4. I_{CC} is specified with the DQ pin open.
5. I_{CC1} is specified with V_{CC} at 5.0V and $\overline{RST}$ = GND.
6. I_{BAT} is specified with $V_{CC} < V_{BAT}$ and V_{BAT} within DC recommended operating conditions.
7. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V.
8. Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
9. Load capacitance = 50 pF.
10. Specified as the load capacitance for which the crystal frequency is guaranteed (see crystal manufacturer's data sheet).
11. Leakage current is the amount of current consumed from the battery when V_{CC} is not present and the oscillator is turned off.

DS1602 8–PIN DIP 300 MIL

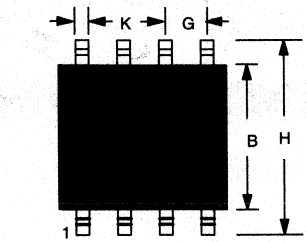


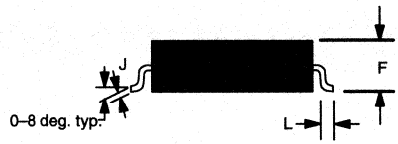


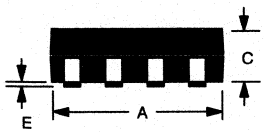


PKG	8-PIN	
DIM	**MIN**	**MAX**
A IN.	0.360	0.400
MM	9.14	10.16
B IN.	0.240	0.260
MM	6.10	6.60
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.300	0.325
MM	7.62	8.26
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.140
MM	3.04	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.320	0.370
MM	8.13	9.4
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1602 8–PIN SOIC 200 MIL







PKG	8-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.203 5.16	0.213 5.41
B IN. MM	0.203 5.16	0.213 5.41
C IN. MM	0.070 1.78	0.074 1.88
E IN. MM	0.004 0.102	0.007 0.254
F IN. MM	0.074 1.88	0.84 2.13
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.302 7.67	0.318 8.07
J IN. MM	0.006 0.152	0.010 0.254
K IN. MM	0.013 0.33	0.020 0.508
L IN. MM	0.19 4.83	0.030 0.762

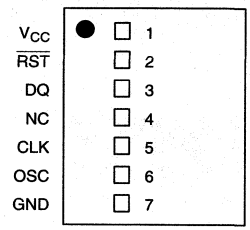
DALLAS SEMICONDUCTOR

DS1603
Elapsed Time Counter Module

FEATURES

- Two 32–bit counters keep track of real time and elapsed time
- Counters keep track of seconds for over 125 years
- Battery powered counter counts seconds from the time battery is attached until V_{BAT} is less than 2.5 volts
- V_{CC} powered counter counts seconds while V_{CC} is above 4.25 volts and retains the count in the absence of V_{CC} under battery backup power
- Clear function resets selected counter to zero
- Read/Write serial port affords low pin count
- Powered internally by a lithium energy cell that provides over 10 years of operation
- One byte protocol defines read/write, counter address and software clear function
- Self contained crystal provides an accuracy of ±2 min per month
- Operating temperature range of 0°C to 70°C
- Low profile SIP module

PIN ASSIGNMENT



PIN DESCRIPTION

$\overline{RST}$	-	Reset
CLK	-	Clock
DQ	-	Data Input/Output
GND	-	Ground
V_{CC}	-	+5 Volts
OSC	-	1 Hz Oscillator Output
NC	-	No Connection

DESCRIPTION

The DS1603 is a real time clock/elapsed time counter designed to count seconds when V_{CC} power is applied and continually count seconds under battery backup power with an additional counter regardless of the condition of V_{CC}. The continuous counter can be used to derive time of day, week, month, and year by using a software algorithm. The V_{CC} powered counter will automatically record the amount of time that V_{CC} power is applied. This function is particularly useful in determining the operational time of equipment in which the DS1603 is used. Alternatively, this counter can also be used under software control to record real time events. Communication to and from the DS1603 takes place via a 3–wire serial port. A one byte protocol selects read/write functions, counter clear functions and oscillator trim. The device contains a 32.768 KHz crystal which will keep track of time to within ±2 min/mo. An internal lithium energy source contains enough energy to power the continuous seconds counter for over 10 years.

OPERATION

The main elements of the DS1603 are shown in Figure 1. As shown, communications to and from the elapsed time counter occur over a 3–wire serial port. The port is activated by driving $\overline{RST}$ to a high state. With $\overline{RST}$ at high level 8 bits are loaded into the protocol shift register providing read/write, register select, register clear, and oscillator trim information. Each bit is serially input on the rising edge of the clock input. After the first eight clock cycles have loaded the protocol register with a valid protocol additional clocks will output data for a read or input data for a write. V_{CC} must be present to access the DS1603. If V_{CC} < the internal power supply (approximately 3.0 volts) the DS1603 will switch to internal power and disable the serial port to conserve energy. When running off of the internal power supply, only the continuous counter will continue to count and the counter powered by V_{CC} will stop, but retain the count which had accumulated when V_{CC} power was lost.

PROTOCOL REGISTER

The protocol bit definition is shown in Figure 2. Valid protocols and the resulting actions are shown in Table 1. Each data transfer to the protocol register designates what action is to occur. As defined, the MSB (bit 7 which is designated ACC) selects the 32–bit continuous counter for access. If ACC is a logical 1 the continuous counter is selected and the 32 clock cycles that follow the protocol will either read or write this counter. If the counter is being read, the contents will be latched into a different register at the end of protocol and the latched contents will be read out on the next 32 clock cycles. This avoids reading garbled data if the counter is clocked by the oscillator during a read. Similarly, if the counter is to be written, the data is buffered in a register and all 32 bits are jammed into the counter simultaneously on the rising edge of the 32nd clock. The next bit (bit 6 which is designated AVC) selects the 32 bit V_{CC} active counter for access. If AVC is a logical 1 this counter is selected and the 32 clock cycles that follow will either read or write this counter. If both bit 7 and bit 6 are written to a logic high, all clock cycles beyond the protocol are ignored and bit 5, 4, and 3 are loaded into the oscillator trim register. A value of binary 3 (011) will give a clock accuracy of ±120 seconds per month at 25°C. Increasing the binary number towards 7 will cause the real time clock to run faster. Conversely, lowering the binary number towards zero will cause the clock to run slower. Binary 000 will stop the oscillator completely. This feature can be used to conserve battery life during storage. In this mode the internal power supply current is reduced to 100 nA maximum. In applications where oscillator trimming is not practical or not needed, a default setting of 011 is recommended. Bit 2 of protocol (designated CCC) is used to clear the continuous counter. When set to logic 1, the continuous counter will reset to zero when $\overline{RST}$ is taken low. Bit 1 of protocol (designated CVC) is used to clear the V_{CC} active counter. When set to logical 1, the V_{CC} active counter will reset to zero when $\overline{RST}$ is taken low. Both counters can be reset simultaneously by setting CCC and CVC both to a logical 1. Bit zero of the protocol (designated RD) determines whether the 32 clocks to follow will write a counter or read a counter. When RD is set to a logical 0 a write action will follow when RD is set to a logical 1 a read action will follow. When sending the protocol, eight bits should always be sent. Sending less than 8 bits can produce erroneous results. If clearing the counters or trimming the oscillator, the data transfer can be terminated after the 8–bit protocol is sent. However, when reading or writing the counters, 32 clock cycles should always follow the protocol.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input has two functions. First, $\overline{RST}$ turns on the serial port logic which allows access to the protocol register for the protocol data entry. Second, the $\overline{RST}$ signal provides a method of terminating the protocol transfer or the 32–bit counter transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For write inputs, data must be valid during the rising edge of the clock. Data bits are output on the falling edge of the clock when data is being read. All data transfers terminate if the $\overline{RST}$ input is transitioned low and the DQ pin goes to a high impedance state. $\overline{RST}$ should only be transitioned low while the clock is high to avoid disturbing the last bit of data. All data transfers must consist of 8 bits when transferring protocol only or 8 + 32 bits when reading or writing either counter. Data transfer is illustrated in Figure 3.

DATA INPUT

Following the 8–bit protocol that inputs write mode, 32 bits of data are written to the selected counter on the rising edge of the next 32 CLK cycles. After 32 bits have been entered any additional CLK cycles will be ignored until $\overline{RST}$ is transitioned low to end data transfer and then high again to begin new data transfer.

DATA OUTPUT

Following the eight CLK cycles that input read mode protocol, 32 bits of data will be output from the selected counter on the next 32 CLK cycles. The first data bit to be transmitted from the selected 32–bit counter occurs on the falling edge after the last bit of protocol is written. When transmitting data from the selected 32–bit counter, $\overline{RST}$ must remain at high level as a transition to low level will terminate data transfer. Data is driven out the DQ pin as long as CLK is low. When CLK is high the DQ pin is tristated.

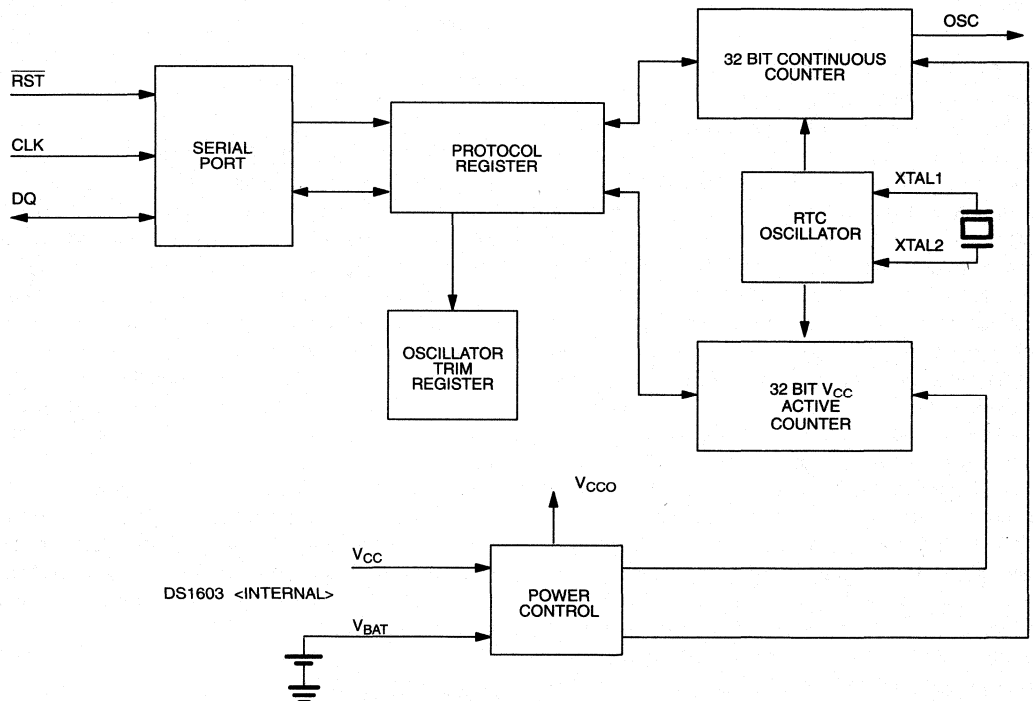
OSCILLATOR OUTPUT

Pin 6 of the DS1603 module is a 1 Hz output signal. This signal is present only when V_{CC} is applied and greater than the internal power supply. However, the output is guaranteed to meet TTL requirement only while V_{CC} is within normal limits. This output can be used as a one second interrupt or time tick needed in some applications.

INTERNAL POWER

The internal battery of the DS1603 module provides 35 mAh and will run the elapsed time counter for over 10 years in the absence of power.

DS1603 ELAPSED TIME COUNTER BLOCK DIAGRAM Figure 1



PROTOCOL BIT MAP Figure 2

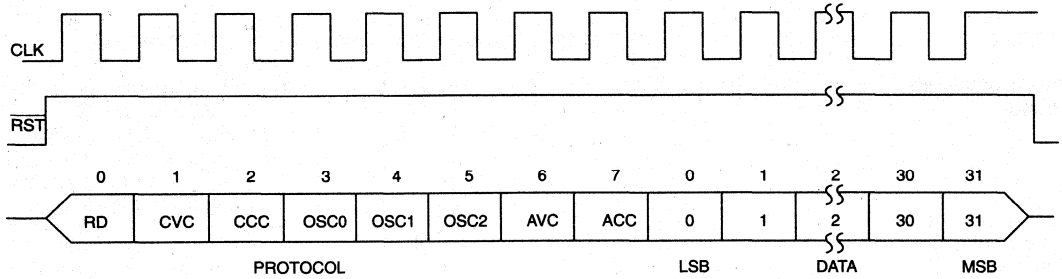
7	6	5	4	3	2	1	0
ACC	AVC	OSC2	OSC1	OSC0	CCC	CVC	RD

VALID PROTOCOLS Table 1

ACTION	PROTOCOL								DESCRIPTION
	ACC	AVC	**OSC2**	**OSC1**	**OSC0**	**CCC**	**CVC**	**RD**	
Read Continuous Counter	1	0	X	X	X	X	X	1	Output continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Write Continuous Counter	1	0	X	X	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Read V_{CC} Active Counter	0	1	X	X	X	X	X	1	Output V_{CC} active counter on the 32 clocks following protocol, oscillator trim register is not updated. Counters are not reset.
Write V_{CC} Active Counter	0	1	X	X	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Clear Continuous Counter	0	0	X	X	X	1	X	X	Resets the continuous counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Clear V_{CC} Active Counter	0	0	X	X	X	X	1	X	Resets the V_{CC} active counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Set Oscillator Trim Bits	1	1	A	B	C	X	X	0	Sets the oscillator trim register to a value of ABC. Counters are unaffected.
X = Don't Care									

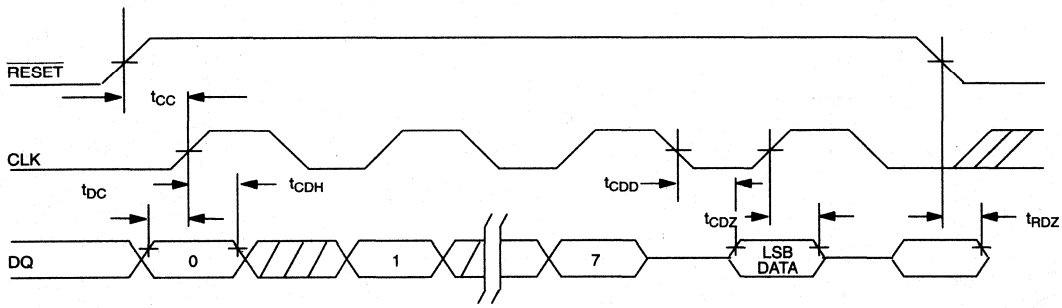
3

DATA TRANSFER Figure 3

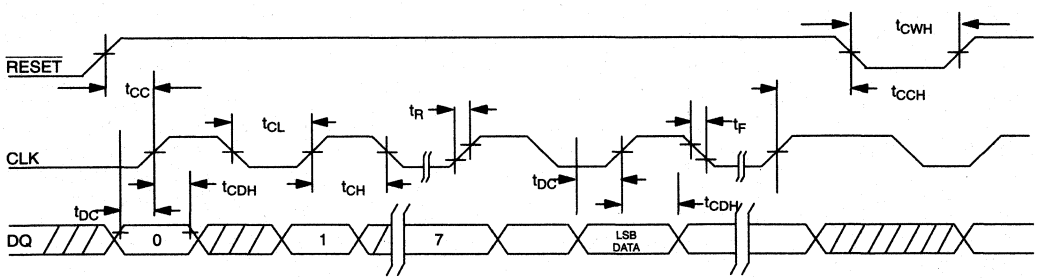


TIMING DIAGRAM: READ/WRITE DATA TRANSFER

READ DATA TRANSFER



WRITE DATA TRANSFER



NOTE: t_{CL}, t_{CH}, t_R, and t_F apply to both read and write data transfer.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = +5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	-1		+1	µA	
I/O Leakage	I_{LO}	-1		+1	µA	
Logic 1 Output	V_{OH}	2.4			V	2
Logic 0 Output	V_{OL}			0.4	V	3
Active Supply Current	I_{CC}			1	mA	4
Timekeeping Current	I_{CC1}			50	µA	5
Battery Trip Point	V_{TP}	2.2		3.7	V	9

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±10%, 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	6
CLK to Data Hold	t_{CDH}	70			ns	6
CLK to Data Delay	t_{CDD}			200	ns	6, 7, 8
CLK Low Time	t_{CL}	250			ns	6
CLK High Time	t_{CH}	250			ns	6
CLK Frequency	f_{CLK}	DC		2.0	MHz	6
CLK Rise & Fall	t_F, t_R			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	100			ns	6
CLK to RST Hold	t_{CCH}	60			ns	6
$\overline{RST}$ Inactive Time	t_{CWH}	1			µs	6
$\overline{RST}$ Low to I/O High Z	t_{RDZ}			70	ns	6
CLK High to I/O High Z	t_{CDZ}			20	ns	6

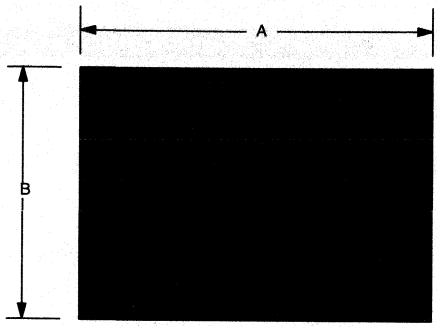
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	10

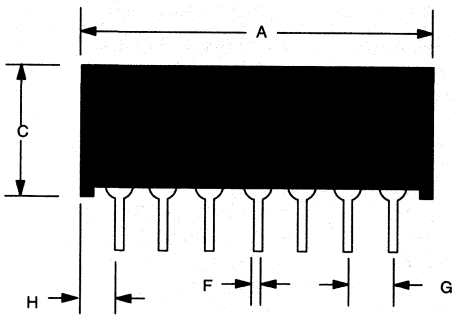
NOTES:

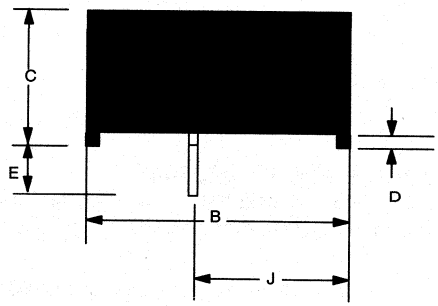
1. All voltages are reference to ground.
2. Logic one voltages are specified at a source current of 1 mA.
3. Logic zero voltages are specified at a sink current of 4 mA.
4. I_{CC} is specified with the DQ pin open.
5. I_{CC1} is specified with V_{CC} at 5.0V and $\overline{RST}$ = GND.
6. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V.
7. Measured at V_{OH} = 2.4V or V_{OL} - 0.4V.
8. Load capacitance = 50 pF.
9. Battery trip point is the point at which the V_{CC} powered counter and the serial port stop operation.
10. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} with the clock oscillator running.

DS1603 7–PIN MODULE



PKG	7-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.830 21.08	0.850 21.59
B IN. MM	0.650 16.51	0.670 17.02
C IN. MM	0.310 7.87	0.330 8.38
D IN. MM	0.015 0.38	0.030 0.76
E IN. MM	0.110 2.79	0.140 3.56
F IN. MM	0.015 0.38	0.021 0.53
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.105 2.67	0.135 3.43
J IN. MM	0.360 9.14	0.390 9.91





DALLAS SEMICONDUCTOR

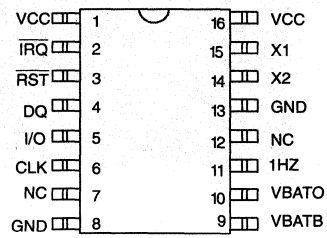
DS1608
EconoRAM Time Chip

FEATURES
- Unique 1-wire interface requires only one port pin for communication
- 3-wire I/O interface for high speed data communications
- Contains real-time clock/calendar in binary format
- 4096 bits of SRAM organized in 16 pages, 256 bits per page
- Interval timer can automatically accumulate time when power is applied
- Programmable cycle counter can accumulate the number of system power-on/off cycles
- Programmable alarms can be set to generate interrupts for interval timer, real-time clock, and/or cycle counter
- Data integrity assured with strict read/write protocols
- Space-saving 16-pin SOIC package
- Operating voltage range from 2.5 to 5.5 Volts

COMPARISON TD DS2404
The DS1608 and DS2404 share many features. The differences between the two parts are as follows:

- The clock oscillator is permanently enabled in the DS1608
- Permanent write protection and programmable expiration are not available with the DS1608
- The DS1608 does not incorporate the parasite powered circuitry
- Lasered serial number: family codes differ between the two and the 48 bit serial number is fixed with the DS1608

PIN ASSIGNMENT



16 PIN SOIC (300 Mil)

PIN DESCRIPTION

V_{CC}	– 2.5 to 5.5 Volts
$\overline{IRQ}$	– Interrupt Output
$\overline{RST}$	– 3-Wire Reset Input
DQ	– 3-Wire Input/Output
I/O	– 1-Wire Input/Output
CLK	– 3-Wire Clock Input
NC	– No Connection
GND	– Ground
V_{BATB}	– Battery Backup Input
V_{BATO}	– Battery Operate Input
1 Hz	– 1 Hz Output
X_1, X_2	– Crystal Connections

ORDERING INFORMATION

DS1608	16–pin DIP; –20°C to +70°C
DS1608S	16–pin SOIC; –20°C to +70°C

DESCRIPTION
TheDS1608EconoRAMTimeChipoffersasimplesolution for storing and retrieving vital data and time information with minimal hardware. The DS1608 contains a lasered ROM, real-time clock/calendar, interval timer, cycle counter, programmable interrupts and 4096 bits of SRAM. Two separate ports are provided for communication, 1-wire and 3-wire. Using the 1-wire port, only one pin is required for communication. The 3-wire port

provides high speed communication using the traditional Dallas Semiconductor 3-wire interface. With either interface, a strict protocol for accessing the DS1608 insures data integrity. Utilizing backup energy sources, the data is nonvolatile and allows for stand-alone operation.

The DS1608 features can be used to create a stopwatch, alarm clock, time and date stamp, logbook, hour meter, calendar, system power cycle timer, and event scheduler.

DETAILED PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1, 16	V_{CC}	**Power input pins** for V_{CC} operate mode. 2.5 to 5.5 volts operation. Either pin can be used for V_{CC}. Only one is required for normal operation. (See V_{BATO} pin description and "Power Control" section).
2	$\overline{IRQ}$	**Interrupt output pin:** Open drain.
3	$\overline{RST}$	**Reset input pin** for 3-wire operation.
4	DQ	**Data input/output pin** for 3-wire operation.
5	I/O	**Data input/output** for 1-wire operation: Open drain.
6	CLK	**Clock input pin** for 3-wire operation.
7, 12	NC	**No connection pins.**
8, 13	GND	**Ground pin:** Either pin can be used for ground.
9	V_{BATB}	**Battery backup input pin:** Battery voltage can be 2.5 to 5.5 volts. (See V_{BATO} pin description and "Power Control" section.)
10	V_{BATO}	**Battery operate input pin** for 2.5 to 5.5 volt operation. The V_{CC} & V_{BATB} pins must be grounded when this pin is used to power the chip. (See "Power Control" section.)
11	1Hz	**1 Hz square wave output:** Open drain.
14, 15	X_1, X_2	**Crystal pins.** Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S (be sure to request 6 pF load capacitance). **NOTE:** X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area.

OVERVIEW

The DS1608 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) timekeeping registers. The timekeeping section utilizes an on-chip oscillator that is connected to an external 32.768 kHz crystal. The SRAM and timekeeping registers reside in one contiguous address space referred to hereafter as memory. All data is read and written least significant bit first.

Two communication ports are provided, a 1-wire port and a 3-wire port. A port selector determines which of the two ports is being used. The ROM data is accessible only through the 1-wire port. The scratchpad and memory are accessible via either port.

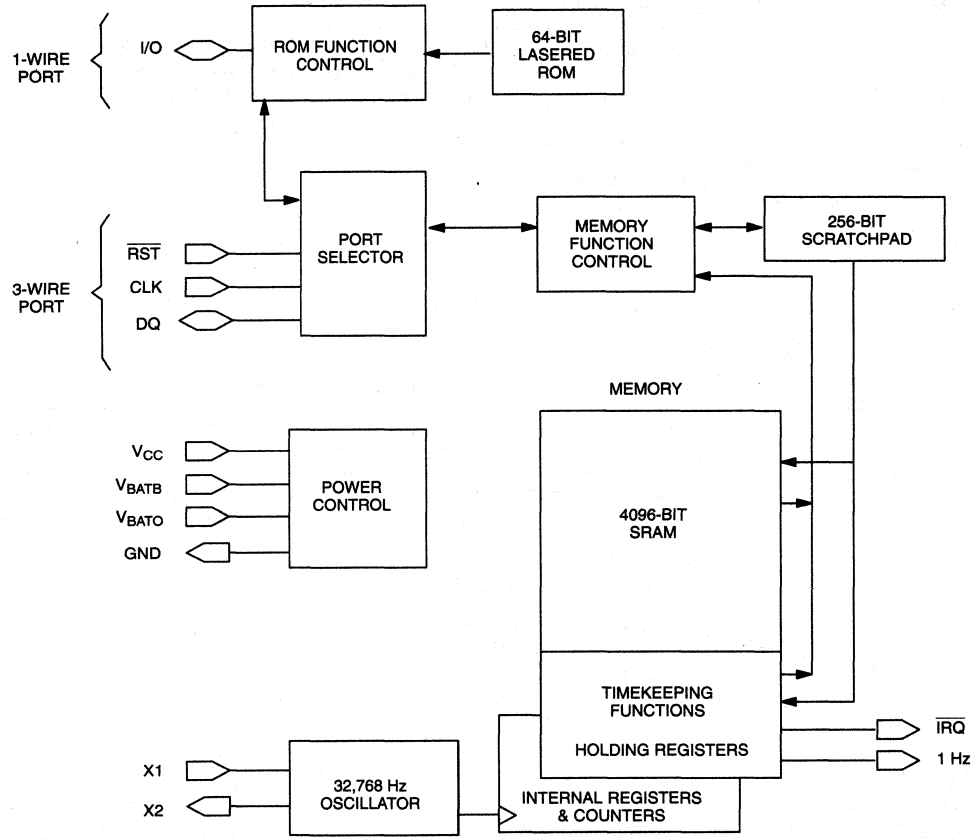
If the 3-wire port is used, the master provides one of four memory function commands: 1) read memory, 2) read scratchpad, 3) write scratchpad, or 4) copy scratchpad. The only way to write memory is to first write the scratchpad and then copy the scratchpad data to memory. (See Figure 6.)

If the 1-wire port is used, the memory functions will not be available until the ROM function protocol has been established. This protocol is described in the ROM functions flow chart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the

master may then provide any one of the four memory function commands.

The "Power Control" section provides for two basic power configurations, battery operate mode and V_{CC} operate mode. The battery operate mode utilizes one supply connected to V_{BATO}. The V_{CC} operate mode may utilize two supplies; the primary supply connects to V_{CC} and a backup supply connects to V_{BATB}.

DS1608 BLOCK DIAGRAM Figure 1



COMMUNICATION PORTS

Two communication ports are provided, a 1–wire and a 3–wire port. The advantages of using the 1–wire port are as follows: 1) provides access to the 64–bit lasered ROM, 2) consists of a single communication signal (I/O), and 3) multiple devices may be connected to the 1–wire bus. The 1–wire bus has a maximum data rate of 16.6K bits/second and requires one 5KΩ external pullup.

The 3-wire port consists of three signals, $\overline{RST}$, CLK, and DQ. $\overline{RST}$ is an enable input, DQ is bidirectional serial data, and the CLK input is used to clock in or out the serial data. The advantages of using the 3-wire port are 1) high data transfer rate (2 MHz), 2) simple timing, and 3) no external pull-up required.

Port selection is accomplished on a first-come, first-serve basis. Whichever port comes out of reset first will

obtain control. For the 3-wire port, this is done by bringing $\overline{RST}$ high. For the 1-wire port, this is done on the first falling edge of I/O after the reset and presence pulses. (See "1-Wire Signalling" section.)

64-BIT LASERED ROM

Each DS1608 contains a ROM code that is 64 bits long. The first eight bits are a 1-wire family code (DS1608 code is 40h). The next 48 bits are a serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 2.)

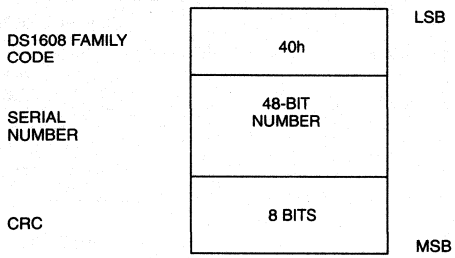
The 1-wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$.

Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in an application note entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products".

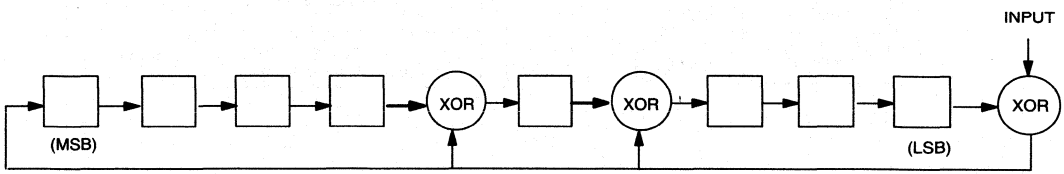
The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

3

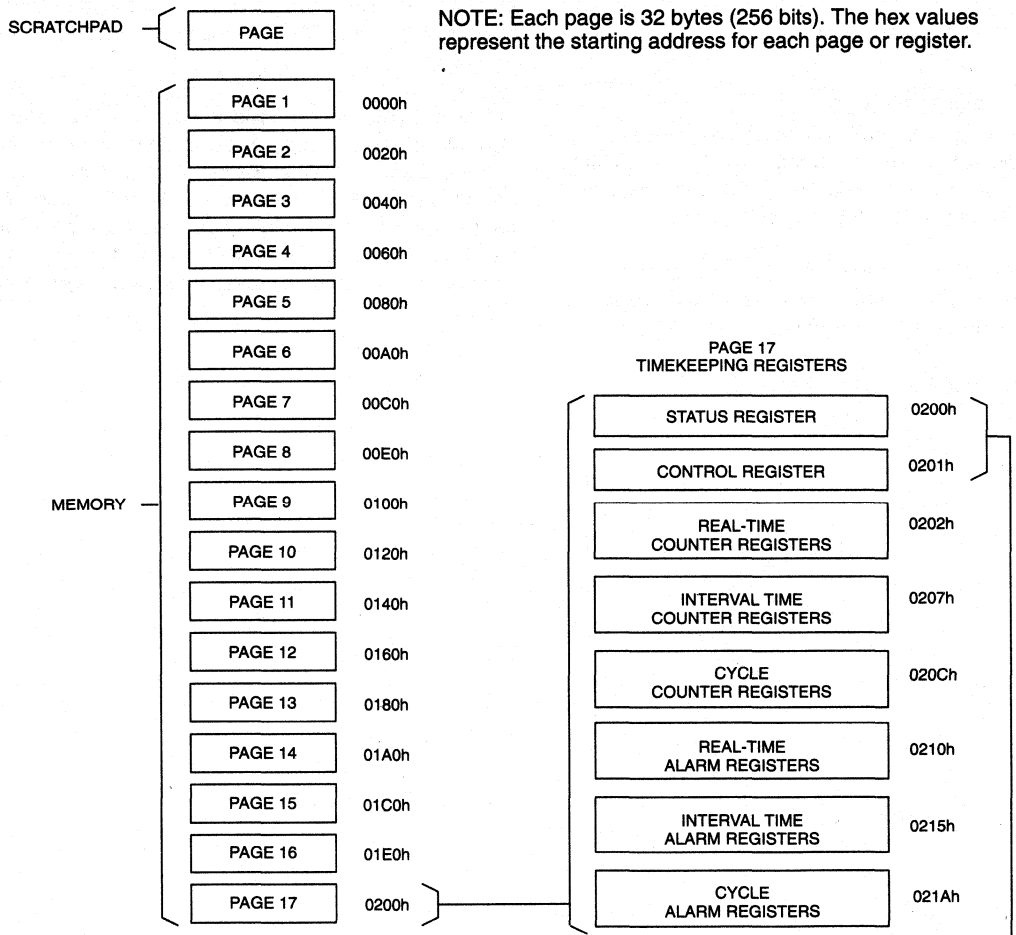
64-BIT LASERED ROM Figure 2



1-WIRE CRC CODE Figure 3



MEMORY MAP Figure 4



STATUS REGISTER

7	6	5	4	3	2	1	0	
X	X	$\overline{CCE}$	$\overline{ITE}$	$\overline{RTE}$	CCF	ITF	RTF	0200h

CONTROL REGISTER

7	6	5	4	3	2	1	0	
DSEL	STOP / START	AUTO / MAN	1	0	0	0	0	0201h

MEMORY

The memory map in Figure 4 shows a page (32 bytes) called the scratchpad and 17 pages called memory. Pages 1 through 16 each contain 32 bytes which make up the 4096-bit SRAM. Page 17 has only 30 bytes which contain the timekeeping registers.

The scratchpad is an additional page of memory that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process insures data integrity when modifying the memory.

TIMEKEEPING

A 32,768 Hz crystal oscillator is used as the time base for the timekeeping functions. The oscillator must be on for the real time clock, interval timer, cycle counter and 1 Hz output to function.

Oscillator

The DS1608 oscillator is always enabled. When the circuit is first powered on, it may take several seconds for the oscillator to start, especially at temperature extremes.

The timekeeping functions are double buffered. This feature allows the master to read time or count without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers which the user accesses. This occurs after the eighth bit of the Read Memory Function command.

Real-Time Clock

The real-time clock is a 5-byte binary counter. It is incremented 256 times per second. The least significant byte is a count of fractional seconds. The upper four bytes are a count of seconds. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point which is determined by the user. For example, 12:00A.M., January 1, 1970 could be a reference point.

Interval Timer

The interval timer is a 5-byte binary counter. When enabled, it is incremented 256 times per second. The least significant byte is a count of fractional seconds. The interval timer can accumulate 136 years of seconds before rolling over. The interval timer has two modes of operation which are selected by the AUTO/$\overline{\text{MAN}}$ bit in the control register. In the auto mode, the interval timer will begin counting after the I/O line has been high for a period of time determined by the DSEL bit in the control register. Similarly, the interval timer will stop counting after the I/O line has been low for a period of time determined by the DSEL bit. In the manual mode, time accumulation is controlled by the STOP/$\overline{\text{START}}$ bit in the control register.

NOTE: For auto mode operation, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.

Cycle Counter

The cycle counter is a 4-byte binary counter. It increments after the falling edge of the I/O line if the appropriate I/O line timing has been met. This timing is selected by the DSEL bit in the control register. (See "Status/Control" section).

NOTE: For cycle counter operation, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.

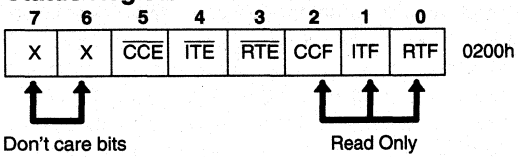
Alarm Registers

The alarm registers for the real-time clock, interval timer, and cycle counter all operate in the same manner. When the value of a given counter equals the value in its associated alarm register, the appropriate flag bit is set in the status register. If the corresponding interrupt enable bit(s) in the status register is set, an interrupt is generated. If a counter and its associated alarm register are write protected when an alarm occurs, access to the device becomes limited. (See "Status/Control", "Interrupts", and the "Programmable Expiration" sections.)

STATUS/CONTROL REGISTERS

The status and control registers are the first two bytes of page 17 (see "Memory Map", Figure 4).

Status Register



0	RTF	Real-time clock alarm flag
1	ITF	Interval timer alarm flag
2	CCF	Cycle counter alarm flag

When a given alarm occurs, the corresponding alarm flag is set to a logic 1. The alarm flag(s) is cleared by reading the status register.

3	$\overline{RTE}$	Real-time interrupt enable
4	$\overline{ITE}$	Interval timer interrupt enable
5	$\overline{CCE}$	Cycle counter interrupt enable

Writing any of the interrupt enable bits to a logic 0 will allow an interrupt condition to be generated when its corresponding alarm flag is set (see "Interrupts" section).

Control Register

7	6	5	4	3	2	1	0	
DSEL	STOP/$\overline{START}$	AUTO/$\overline{MAN}$.	1	0	0	0	0	0201h

Bits 0, 1, 2, and 3 will always read zero and bit 4 will always read 1 regardless of whether it is written to an opposite state or not.

5 AUTO/$\overline{MAN}$ Automatic/$\overline{Manual}$ Mode

When this bit is set to a logic 1, the interval timer is in automatic mode. In this mode, the interval timer is enabled by the I/O line. When this bit is set to a logic 0, the interval timer is in manual mode. In this mode the interval timer is enabled by the STOP/$\overline{START}$ bit.

6 STOP/$\overline{START}$ Stop/$\overline{Start}$ (in Manual Mode)

If the interval timer is in manual mode, the interval timer will start counting when this bit is set to a logic 0 and will stop counting when set to a logic 1. If the interval timer is in automatic mode, this bit has no effect.

7 DSEL Delay Select Bit

This bit selects the delay that it takes for the cycle counter and the interval timer (in auto mode) to see a transition on the I/O line. When this bit is set to a logic 1, the delay time is 123 ± 2 ms. This delay allows communication on the I/O line without starting or stopping the interval timer and without incrementing the cycle counter. When this bit is set to a logic 0, the delay time is 3.5 ± 0.5 ms.

MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the memory. Two examples follow the flowchart. Three address registers are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status byte (E/S).

The target address points to a unique byte location in memory. The first five bits of the target address (T4:T0) represent the byte offset within a page. This byte offset points to one of 32 possible byte locations within a given page. For instance, 00000b points to the first byte of a page where as 11111b would point to the last byte of a page.

The third register (E/S) is a read only register. The first five bits (E4: E0) of this register are called the ending offset. The ending offset is a byte offset within a page (1 of 32 bytes). Bit 5 (PF) is the partial byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

ADDRESS REGISTERS Figure 5

	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	OF	PF	E4	E3	E2	E1	E0

3

Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the user must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) will be set and the remaining data will be ignored. If the user writes an incomplete byte and an overflow has not occurred, the partial byte flag (PF) will be set.

Read Scratchpad Command [AAh]

This command may be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user may begin reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The user may read data until the end of the scratchpad after which the data read will be all logic 1's.

Copy Scratchpad [55h]

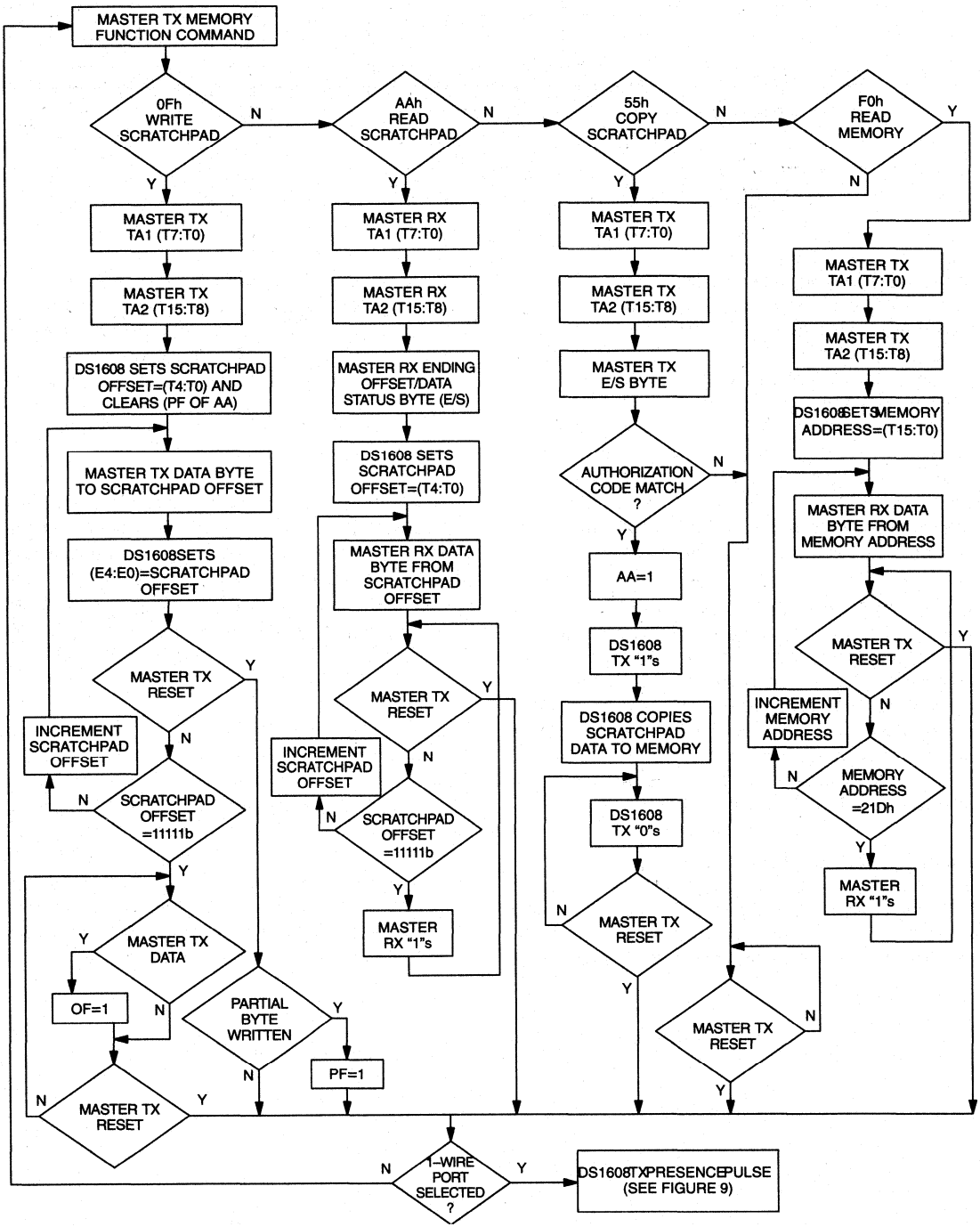
This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-byte authorization pattern. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. At this point, the part will go into a T_X mode, transmitting a logic 1 to indicate the copy is in progress. A logic 0 will be transmitted after the data has been copied. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30 µs.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 2 to 32 bytes may be copied to memory with this command. Whole bytes are copied even if only partially written. The AA flag will be cleared only by executing a write scratchpad command.

Read Memory [F0h]

The read memory command may be used to read the entire memory. After issuing the command, the user must provide the 2-byte target address. After the two bytes, the user reads data beginning from the target address and may continue until the end of page 17. After the end of page 17, logic 1's will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

MEMORY FUNCTION FLOW CHART Figure 6



MEMORY FUNCTION EXAMPLES

Example 1: Write one page of data to page 16
Read page 16 (3-wire port)

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Master pulses $\overline{RST}$ low
TX	0Fh	Issue "write scratchpad" command
TX	E0h	TA1, beginning offset=0
TX	01h	TA2, address=01E0h
TX	<32 data bytes>	Write 1 page of data to scratchpad
TX	Reset	Master pulses $\overline{RST}$ low
TX	AAh	Issue "read scratchpad" command
RX	E0h	Read TA1, beginning offset=0
RX	01h	Read TA2, address=01E0h
RX	1Fh	Read E/S, ending offset=31d, flags=0
RX	<32 data bytes>	Read scratchpad data and verify
TX	Reset	Master pulse $\overline{RST}$ low
TX	55h	Issue "copy scratchpad" command
TX	E0h	TA1 } AUTHORIZATION CODE
TX	01h	TA2 } AUTHORIZATION CODE
TX	1Fh	E/S } AUTHORIZATION CODE
RX	<busy indicator>	Wait until DQ=0 (~30 µs typical)
TX	Reset	Master pulse $\overline{RST}$ low
TX	F0h	Issue "read memory" command
TX	E0h	TA1, beginning offset=0
TX	01h	TA2, address=01E0h
RX	<32 data bytes>	Read memory page 16 and verify
TX	Reset	Master pulse $\overline{RST}$ low, done

Example 2: Write two data bytes to memory locations 0026h and 0027h (the seventh and eighth bytes of page 2). Read entire memory (1-wire port).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	0Fh	Issue "write scratchpad" command
TX	26h	TA1, beginning offset=6
TX	00h	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	AAh	Issue "read scratchpad" command
RX	26h	Read TA1, beginning offset=6
RX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7, flags=0
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	55h	Issue "copy scratchpad" command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
RX	<busy indicator>	Wait until 0
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	F0h	Issue "read memory" command
TX	00h	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX	<542 bytes>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

1-WIRE BUS SYSTEM

The 1-wire bus is a system which has a single bus master and one or more slaves. In most instances the DS1608 behaves as a slave. The exception is when the DS1608 generates an interrupt due to a timekeeping alarm. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-wire signalling (signal types and timing).

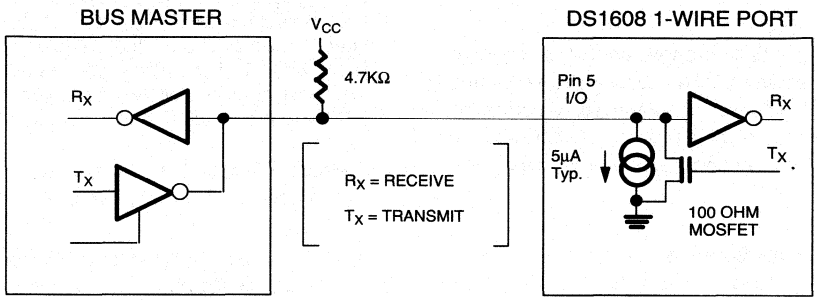
HARDWARE CONFIGURATION

The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain or 3-state outputs. The 1-wire port of the DS1608 (I/O pin 5) is open drain with an internal circuit equivalent to that shown in Figure 7. A multidrop bus consists of a 1-wire bus with multiple slaves attached. The 1-wire bus requires a pull-up resistor of approximately 5KΩ.

The idle state for the 1-wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

3

HARDWARE CONFIGURATION Figure 7



TRANSACTION SEQUENCE

The protocol for accessing the DS1608 via the 1-wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1608 is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 8):

Read ROM [33h]

This command allows the bus master to read the DS1608's 8-bit family code, 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single 1–wire device is on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result).

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific 1–wire device on a multidrop bus. If the DS1608 ROM

sequence is issued it will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wire-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus.

Example of a ROM Search

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1	00110101...
ROM2	10101010...
ROM3	11110101...
ROM4	00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.

2. The bus master will then issue the search ROM command on the 1-wire bus.

3. The bus master reads a bit from the 1-wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 0 onto the 1-wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1-wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the search ROM data command is being executed, all of the devices on the 1-wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 1 onto the 1-wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1-wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-wire bus that have a 0 in the first position and others that have a 1.

   The data obtained from the two reads of the 3-step routine have the following interpretations:

   00 - There are still devices attached which have conflicting bits in this position.

   01 - All devices still coupled have a 0 bit in this bit position.

   10 - All devices still coupled have a 1 bit in this bit position.

   11 - There are no devices attached to the 1-wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.

5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.

6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.

7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.

8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.

9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-wire bus.

10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.

11. The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.

12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.

13. The bus master starts a new ROM search by repeating steps 1 through 3.

14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.

15. The bus master executes two read time slots and receives two zeros.

16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.

17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.

18. The bus master starts a new ROM search by repeating steps 13 through 15.

19. The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.

20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

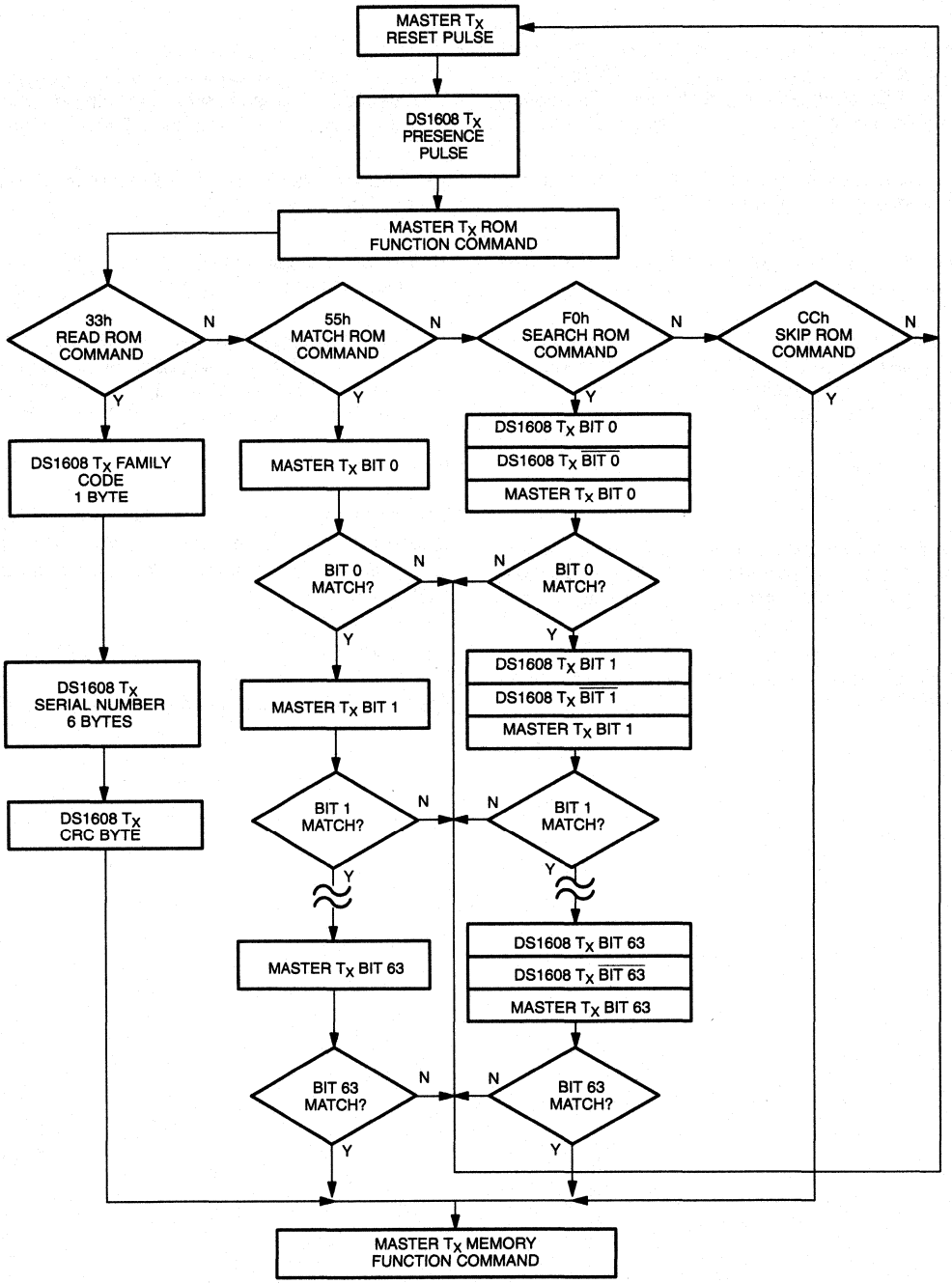
Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

$$960\ \mu s + (8 + 3 \times 64)\ 61\ \mu s = 13.16\ ms$$

The bus master is therefore capable of identifying 75 different 1-wire devices per second.

ROM FUNCTIONS FLOW CHART (1-WIRE PORT ONLY) Figure 8



(SEE FIGURE 5)

I/O SIGNALLING

The DS1608 requires strict protocols to insure data integrity. The protocol consists of seven types of signalling on one line: reset pulse, presence pulse, write 0, write 1, read 0, read 1, and interrupt pulse. All these signals, with the exception of the interrupt pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS1608 is shown in Figure 9. A reset pulse followed by a presence pulse indicates the DS1608 is ready to send or receive data given the correct ROM command and memory function command.

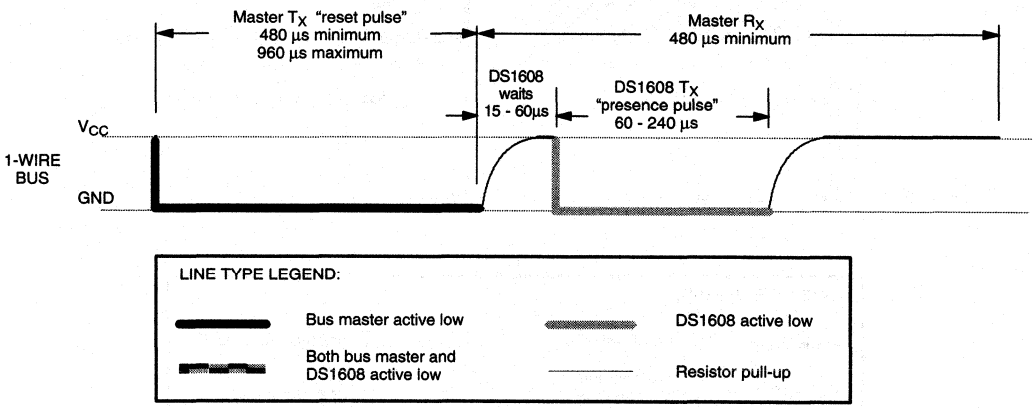
The bus master transmits (T_X) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into receive mode (R_X). The 1-wire bus is pulled to a high state via the 5K pull-up resistor. After detecting the rising edge on the I/O pin, the DS1608 waits 15-60 µs and then transmits the presence pulse (a low signal for 60 - 240 µs). There are special conditions if interrupts are enabled where the bus master must check the state of the 1-wire bus after being in the R_X mode for 480 µs. These conditions will be discussed in the "Interrupt" section.

READ/WRITE TIME SLOTS

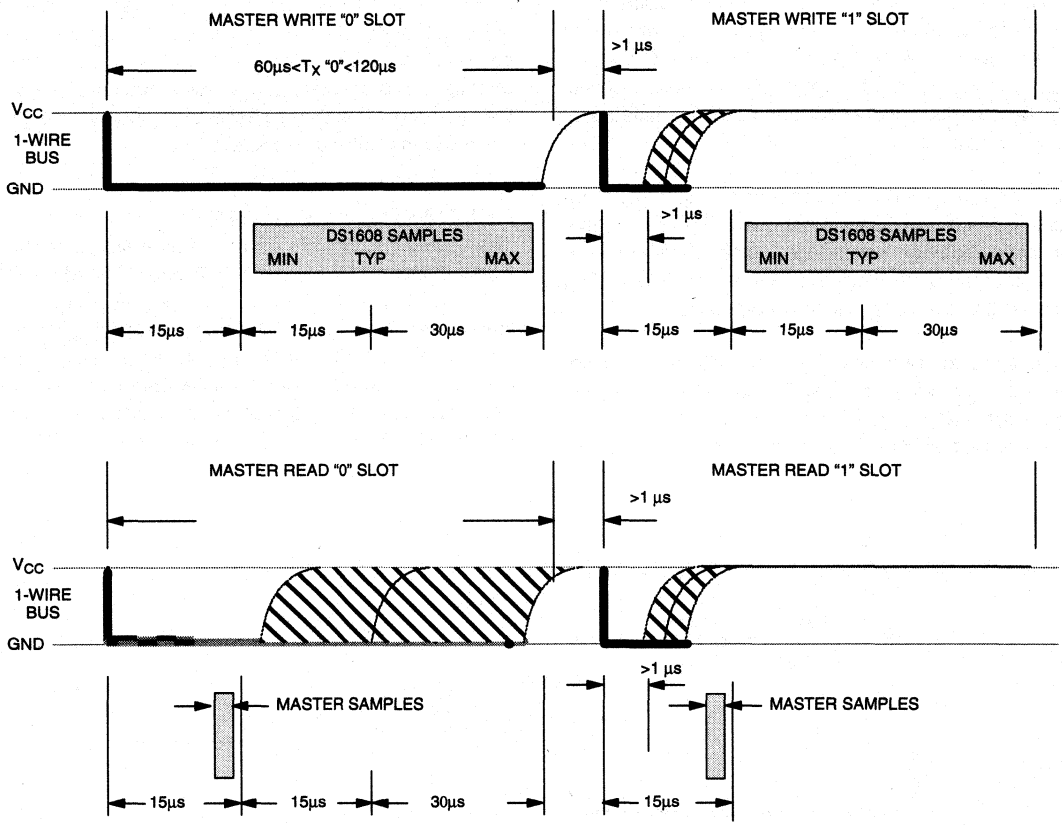
The definitions of write and read time slots are illustrated in Figure 10. All time slots are initiated by the master driving the I/O line low. The falling edge of the I/O line synchronizes the DS1608 to the master by triggering a delay circuit in the DS1608. During write time slots, the delay circuit determines when the DS1608 will sample the I/O line. For a "read 0" time slot, the delay circuit determines how long the DS1608 will hold the I/O line low.

3

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 9



READ/WRITE TIMING DIAGRAM Figure 10



DETAILED MASTER READ "1" TIMING Figure 11

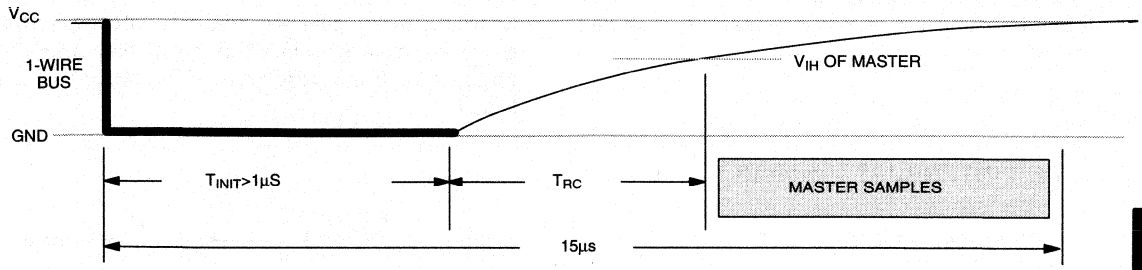
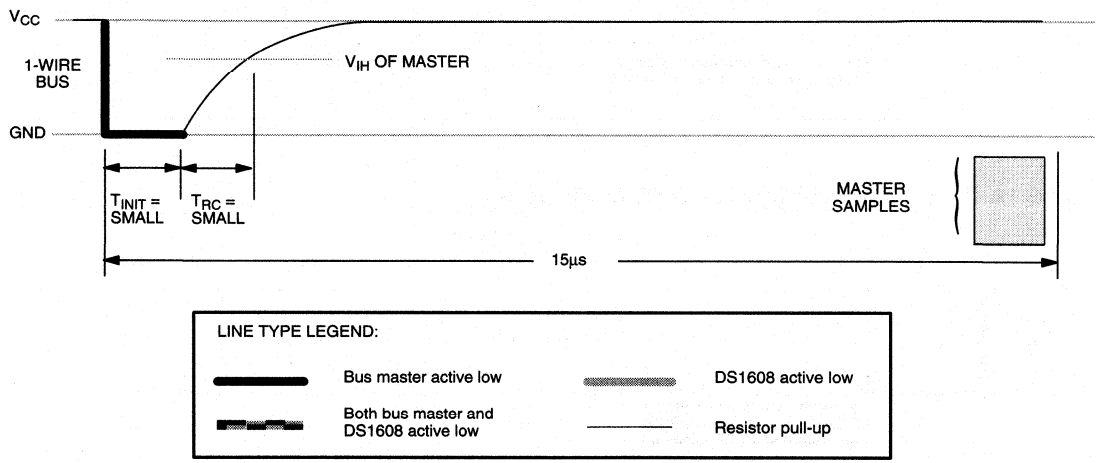


Figure 12 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15µs. Figure 13 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15µs period.

RECOMMENDED MASTER READ "1" TIMING Figure 12



Interrupts

An interrupt condition begins whenever any alarm flag is set and the flag's corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the flags are read) or if the corresponding interrupt enable bit(s) is disabled. An interrupt condition may be detected on either the $\overline{IRQ}$ pin or the I/O pin. During the interrupt condition, the open-drain $\overline{IRQ}$ pin is driven low and held low until the interrupt condition ceases.

On the 1-wire port, the part responds, in general, by driving the I/O pin low for an extended period of time and then releasing. The interrupt condition may produce two types of interrupts on the 1-wire port. A type 1 interrupt (Figure 13) occurs only when I/O is high and there has been no communication (i.e., there has not been a falling edge on I/O since the last presence pulse). If this is the case, I/O is driven low for a period of 960 µs to 3840 µs as soon as an interrupt condition begins. A presence pulse will follow the interrupt pulse.

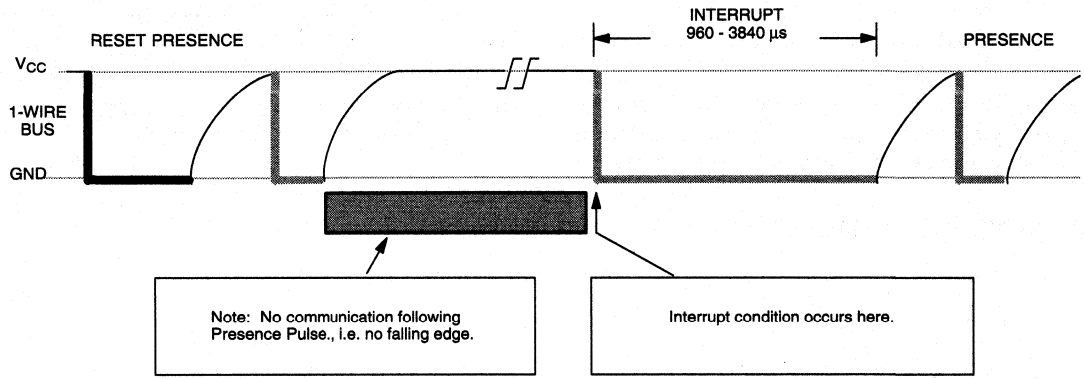
A type 2 interrupt (Figure 15) occurs if the host issues a reset pulse and an interrupt condition exists when the host releases the reset. If this is the case, I/O is driven low for an additional period of time, extending the reset pulse to a total period of 960 µs to 4800 µs. A presence pulse will follow the interrupt pulse. As long as the interrupt condition exists, the type 2 interrupt will occur with every reset pulse.

NOTE: If the interrupt condition begins during communication, a type 1 interrupt will not be issued. However, type 2 interrupts will occur during resets as expected.

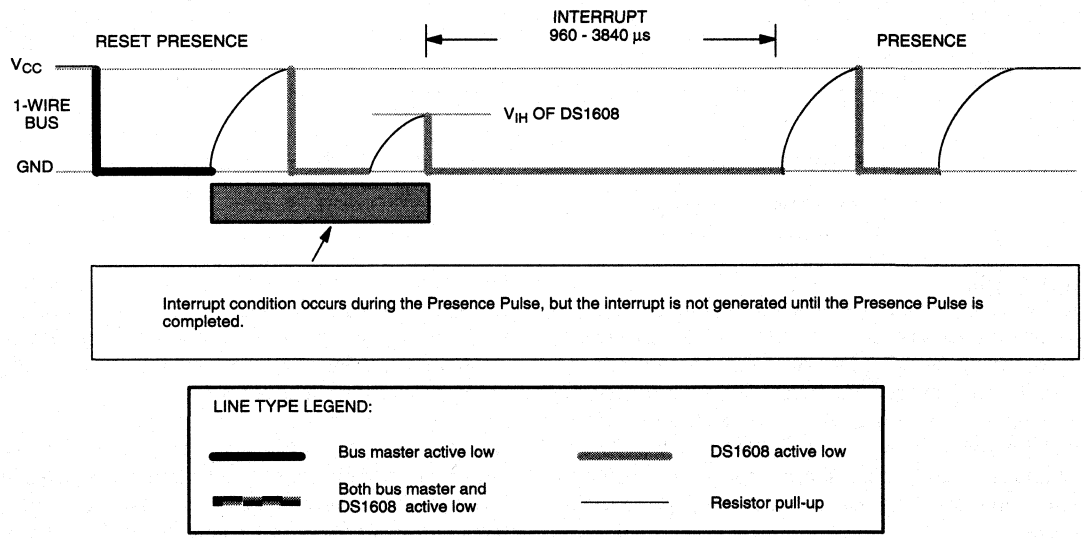
Special cases exist as follows:

Special Case A (Figure 14): If the interrupt condition begins during a presence pulse, the type 1 interrupt will be postponed until the presence pulse is over and I/O is a logic 1.

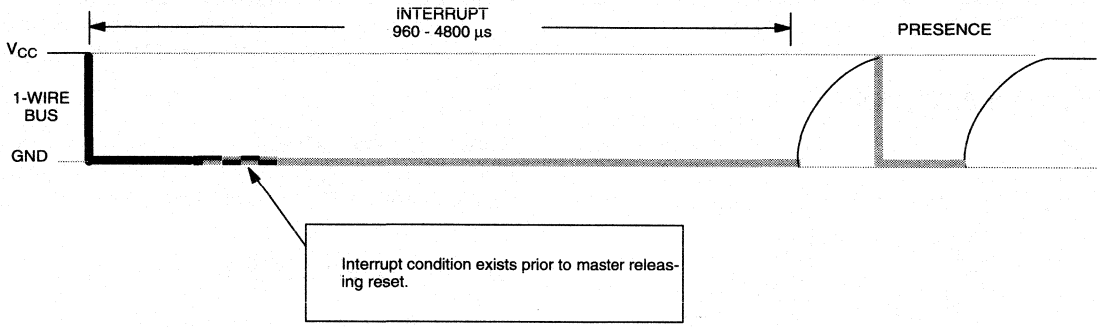
TYPE 1 INTERRUPT Figure 13

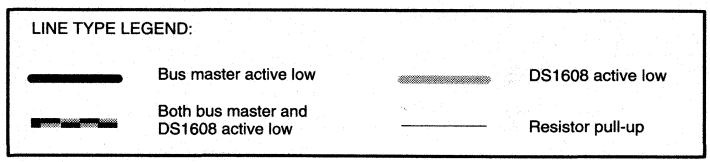


TYPE 1A INTERRUPT (SPECIAL CASE A) Figure 14



TYPE 2 INTERRUPT Figure 15





3

3-WIRE I/O COMMUNICATIONS

The 3-wire bus is comprised of three signals. These are the $\overline{RST}$ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{RST}$ input high. Driving the $\overline{RST}$ input low terminates communication. (See Figures 22 and 23.)

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. When reading data from the DS1608, the DQ pin goes to a high impedance state while the clock is high. Taking $\overline{RST}$ low will terminate any communication and cause the DQ pin to go to a high impedance state.

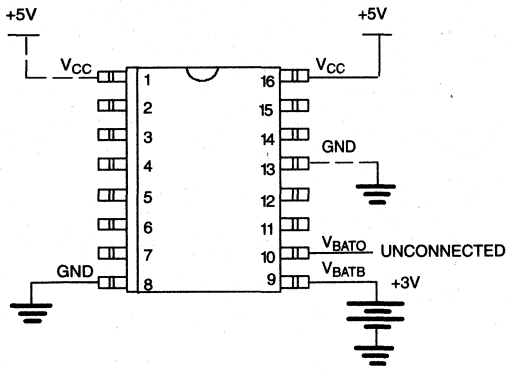
POWER CONTROL

There are two typical methods of supplying power to the DS1608, V_{CC} Operate mode and Battery Operate mode.

V_{CC} Operate Mode (Battery Backed)

Figure 16 shows the necessary connections for operating the DS1608 in V_{CC} Operate mode.

VCC OPERATE MODE Figure 16



V_{CC}	Pin 1 & 16	2.5 to 5.5 volts
V_{BATB}	Pin 9	2.5 to 5.5 volts*
V_{BATO}	Pin 10	must be unconnected

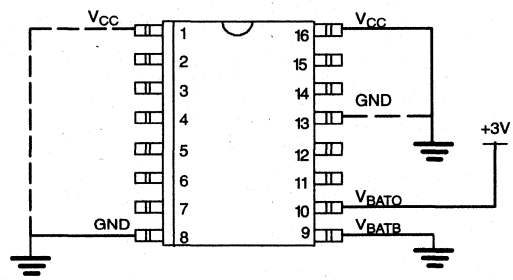
*While V_{BATB} may range from 2.5 to 5.5V, if the voltage on V_{BATB} ever exceeds the voltage on V_{CC}, the DS1608 will retain data, but will not allow access through the 1- or 3-wire port to the RAM.

The V_{BATB} pin is normally connected to any standard 3-volt lithium cell or other energy source. As V_{CC} falls below V_{BATB}, the power switching circuit allows V_{BATB} to provide energy for maintaining clock functionality and data retention. Communication can take place only with the ROM and not the RAM while V_{BATB} is greater than V_{CC}. During power-up, when V_{CC} rises above V_{BATB} (~200 mV), the power switching circuit connects V_{CC} and disconnects V_{BATB}. No communication can take place until V_{CC} has stayed (~200 mV) above V_{BATB} for 123 ± 2 ms.

Battery Operate Mode

Figure 17 shows the necessary connections for operating the DS1608 in Battery Operate mode.

BATTERY OPERATE MODE Figure 17



V_{CC}	Pin 1 & 16	Ground
V_{BATB}	Pin 9	Ground
V_{BATO}	Pin 10	2.5 to 5.5 volts

The V_{BATO} pin is normally connected to any standard 3-volt lithium cell or other energy source. Battery Operate mode provides low power consumption when used in conjunction with 1-wire interface.

Note: If the the 3-wire interface is used in Battery Operate mode, the voltage on DQ must never exceed the voltage on V_{BATO}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-20°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 9
Logic 0	V_{IL}	-0.3		+0.8	V	1
$\overline{RST}$ Logic 1		2.8		5.5	V	1
Supply	V_{CC}	2.8		5.5	V	1
Battery	V_{BATB}, V_{BATO}	2.8	3.0	5.5	V	1, 6

DC ELECTRICAL CHARACTERISTICS

(-20°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			1	mA	
$\overline{RST}$ Resistance to Ground	Z_{RST}		65		KΩ	
D/Q Resistance to Ground	Z_{DQ}		65		KΩ	
CLK Resistance to Ground	Z_{CLK}		65		KΩ	
Active Current	I_{CC1}			2	mA	5
Standby Current	I_{CC2}			500	µA	
I/O Operate Current	I_{BATO}			500	nC	10
Batt Current (OSC On)	I_{BAT1}			350	nA	7

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			15	pF	
I/O (1-Wire)	$C_{IN/OUT}$			80	pF	8

AC ELECTRICAL CHARACTERISTICS: 3-WIRE INTERFACE (-20°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
CLK to Data Hold	t_{CDH}	40			ns	2
CLK to Data Delay	t_{CDD}			100	ns	2,3,4
CLK Low Time	t_{CL}	250			ns	2
CLK High Time	t_{CH}	250			ns	2
CLK Frequency	t_{CLK}	DC		2.0	MHz	2
CLK Rise & Fall	t_R,t_F			500	ns	2
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	2
$\overline{RST}$ Inactive Time	t_{CWH}	250			ns	2
RST to I/O High Z	t_{CDZ}			50	ns	2

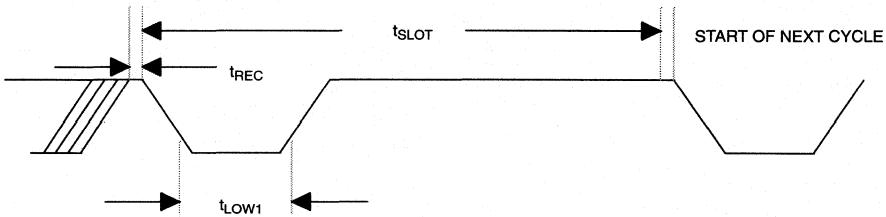
AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE (-20°C to 70°C; V_{CC}=2.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Interrupt	t_{INT}	960		4800	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		960	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

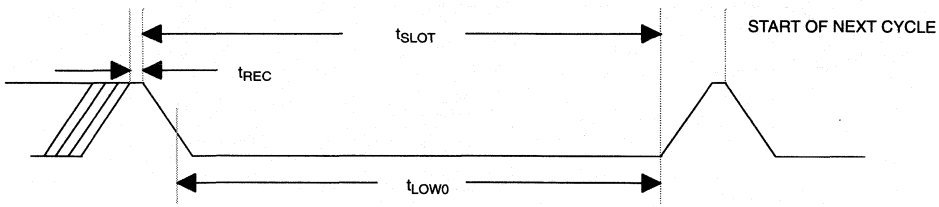
NOTES:

1. All voltages are referenced to ground.
2. V_{IH} = 2.0V or V_{IL} = 0.8V with 10 ns maximum rise and fall time.
3. V_{OH} = 2.4V and V_{OL} = 0.4V.
4. Load capacitance = 50 pF.
5. Measured with outputs open.
6. When battery is applied to V_{BATO} input, V_{CC} and V_{BATB} must be 0V.
7. V_{BATB}, or V_{BATO} = 3.0V; all inputs inactive state.
8. Capacitance on the I/O pin could be 80 pF when power is first applied. If a 5K resistor is used to pull-up the I/O line to V_{CC}, 5 µs after power has been applied, the parasite capacitance will not affect normal communications.
9. For auto-mode operation of the interval timer, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.
10. Read or write scratchpad (all 32 bytes) at 3.0V.

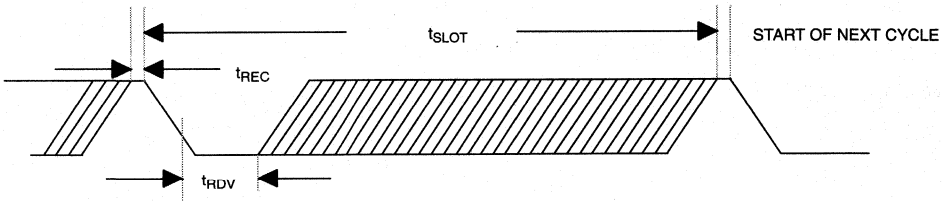
1-WIRE WRITE ONE TIME SLOT Figure 18



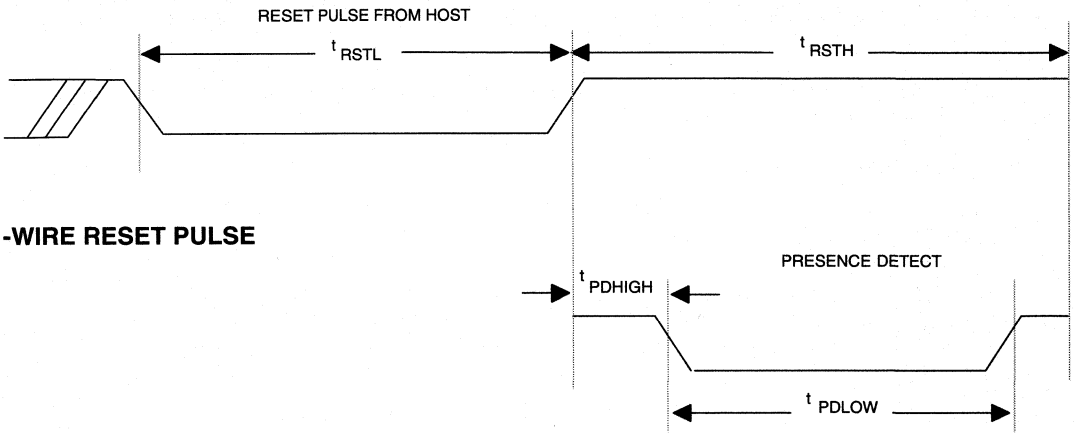
1-WIRE WRITE ZERO TIME SLOT Figure 19



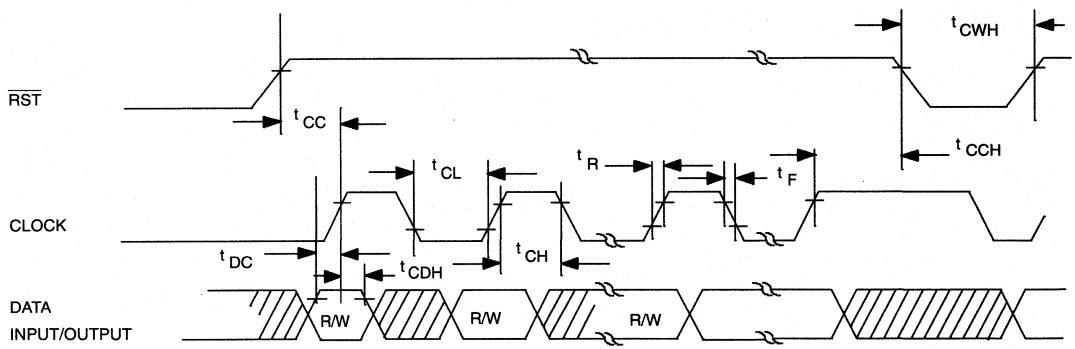
1-WIRE READ ZERO TIME SLOTS Figure 20



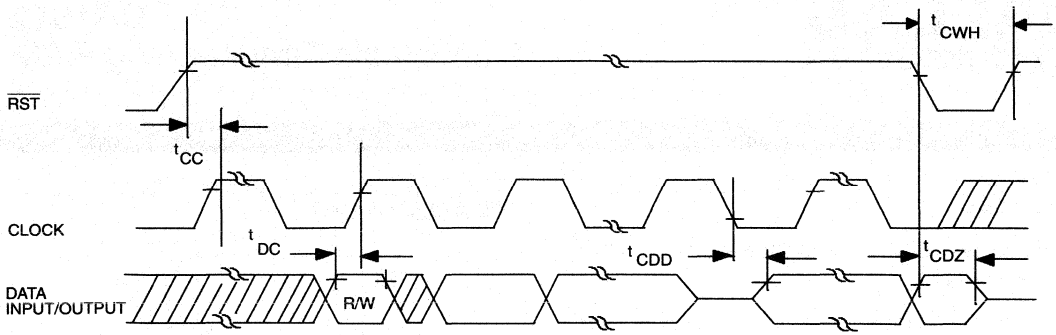
1-WIRE PRESENCE DETECT Figure 21



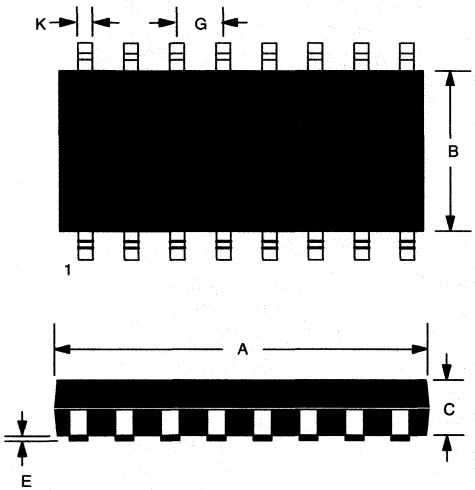
3-WIRE WRITE DATA TIMING DIAGRAM Figure 22

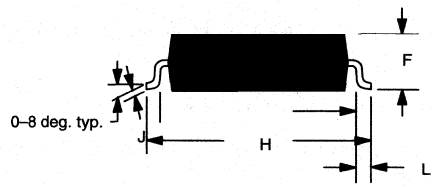


3-WIRE READ DATA TIMING DIAGRAM Figure 23



DS1608 ECONORAM TIME CHIP 16–PIN SOIC





PKG	16-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.402	0.412
B IN. MM	0.290	0.300
C IN. MM	0.089	0.095
E IN. MM	0.004	0.012
F IN. MM	0.094	0.105
G IN. MM	0.050 BSC	
H IN. MM	0.398	0.416
J IN. MM	0.009	0.013
K IN. MM	0.013	0.019
L IN. MM	0.016	0.040

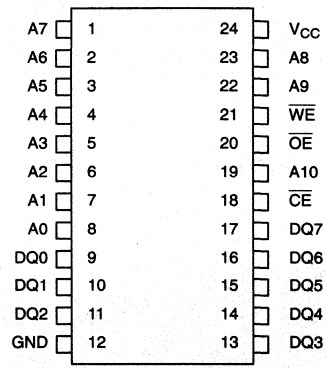
DALLAS SEMICONDUCTOR

DS1642
Nonvolatile Timekeeping RAM

FEATURES

- Form, fit, and function compatible with the MK48T02 Timekeeping RAM
- Integrated NV SRAM, real time clock, crystal, power fail control circuit and lithium energy source
- Standard JEDEC bytewide 2K x 8 static RAM pinout
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 120 ns and 150 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds
- Power fail write protection allows for ±10% V_{CC} power supply tolerance

PIN ASSIGNMENT



PIN DESCRIPTION

A0-A10	-	Address Input
$\overline{CE}$	-	Chip Enable
$\overline{OE}$	-	Output Enable
$\overline{WE}$	-	Write Enable
V_{CC}	-	+5 Volts
GND	-	Ground
DQ0–DQ7	-	Data Input/Output

DESCRIPTION

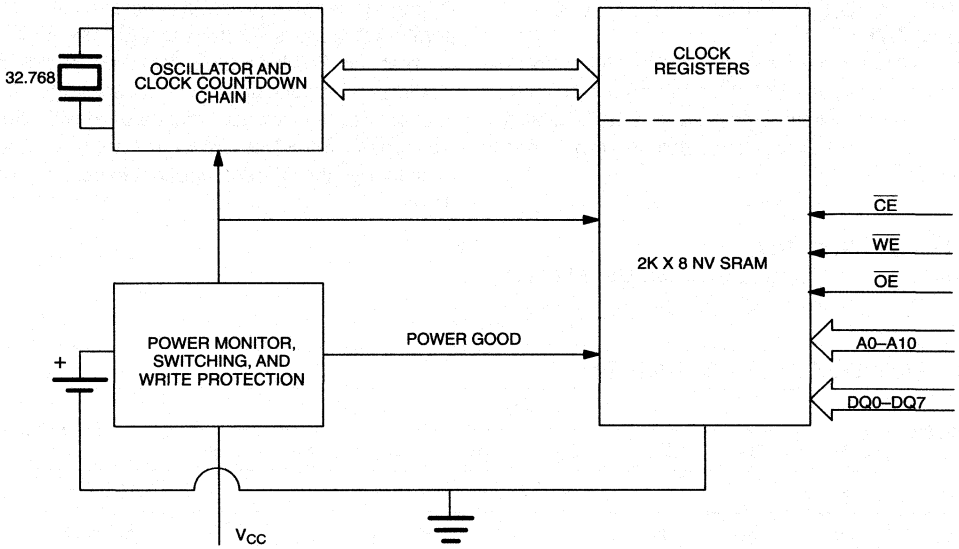
The DS1642 is an 2K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is pin and function equivalent to any JEDEC standard 2K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1642 also contains its own power fail circuitry which deselects the device when the V_{CC} supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

CLOCK OPERATIONS-READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1642 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1642 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

3

DS1642 BLOCK DIAGRAM Figure 1



DS1642 TRUTH TABLE Table 1

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5 VOLTS ± 10%	V_{IH}	X	X	DESELECT	HIGH Z	STANDBY
	V_{IL}	X	V_{IL}	WRITE	DATA IN	ACTIVE
	V_{IL}	V_{IL}	V_{IH}	READ	DATA OUT	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V_{BAT}	X	X	X	DESELECT	HIGH Z	CMOS STANDBY
<V_{BAT}	X	X	X	DESELECT	HIGH Z	DATA RETENTION MODE

SETTING THE CLOCK

The eighth bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1642 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume. Note that both the read bit and write bit perform similar functions and setting both bits during the same access cycle will prevent the clock registers from updating.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, and $\overline{OE}$ low) and address for seconds register remain valid and stable.

CLOCK ACCURACY

The DS1642 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1642 does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary. Attempts to calibrate the clock that may be used with similar device types (MK48T02 family) will not have any effect even though the DS1642 appears to accept calibration data.

DS1642 REGISTER MAP - BANK1 Table 2

ADDRESS	DATA								FUNCTION	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
7FF	-	-	-	-	-	-	-	-	YEAR	00-99
7FE	X	X	X	-	-	-	-	-	MONTH	01-12
7FD	X	X	-	-	-	-	-	-	DATE	01-31
7FC	X	FT	X	X	X	-	-	-	DAY	01-07
7FB	X	X	-	-	-	-	-	-	HOUR	00-23
7FA	X	-	-	-	-	-	-	-	MINUTES	00-59
7F9	$\overline{OSC}$	-	-	-	-	-	-	-	SECONDS	00-59
7F8	W	R	-	-	-	-	-	-	CONTROL	A

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

NOTES:

"X" bits are unused but must be set to zero during write cycle to insure proper clock operation.
Bits 0 through 5 of control register A are not dedicated to any particular function and can be used as normal RAM bits.

RETRIEVING DATA FROM RAM OR CLOCK

The DS1642 is in the read mode whenever $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1642 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CCI} is within nominal limits (V_{CC} > 4.5 volts) the DS1642 can be accessed as described above by read or write cycles. However, when V_{CC} is below the power fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level.

INTERNAL BATTERY LONGEVITY

The DS1642 has a self contained lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CCI} supply is not present. The capability of this internal power supply is sufficient to power the DS1642 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. The DS1642 is shipped from Dallas Semiconductor with the clock oscillator turned off, so the expected life should be considered to start from the time the clock oscillator is first turned on. Actual life expectancy of the DS1642 will be much longer than 10 years since no internal lithium battery energy is consumed when V_{CC} is present. In fact, in most applications, the life expectancy of the DS1642 will be approximately equal to the shelf life (expected useful life of the lithium battery with no load attached) of the lithium battery which may prove to be as long as 20 years.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-20°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC}+0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C $\leq t_A \leq$ 70°C; V_{CC} (MAX) $\leq V_{CC} \leq V_{CC}$ (MIN))

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		30	50	mA	2, 3
TTL Standby Current ($\overline{CE} = V_{IH}$)	I_{CC2}		3	6	mA	2, 3
CMOS Standby Current ($\overline{CE}$=V_{CC}-0.2V)	I_{CC3}		2	4.0	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Write Protection Voltage	V_{TP}	4.0	4.25	4.5	V	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V + 10%)

PARAMETER	SYMBOL	DS1642-12		DS1642-15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Address Access Time	t_{AA}		120		150	ns	
$\overline{CE}$ Access Time	t_{CEA}		120		150	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		40		50	ns	
Output Enable Access Time	t_{OEA}		100		120	ns	
Output Enable Data Off Time	t_{OEZ}		40		50	ns	
Output Enable to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns	
Output Hold from Address	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Address Setup Time	t_{AS}	0		0		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	100		120		ns	
Address Hold from End of Write	t_{AH}	15		20		ns	
Write Pulse Width	t_{WEW}	120		150		ns	
$\overline{WE}$ Data Off Time	t_{WEZ}		40		50	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10		15		ns	
Data Setup Time	t_{DS}	85		110		ns	
Data Hold Time High	t_{DH}	15		20		ns	

AC TEST CONDITIONS

Input Levels: 0V to 3V
Transition Times: 5 ns

CAPACITANCE

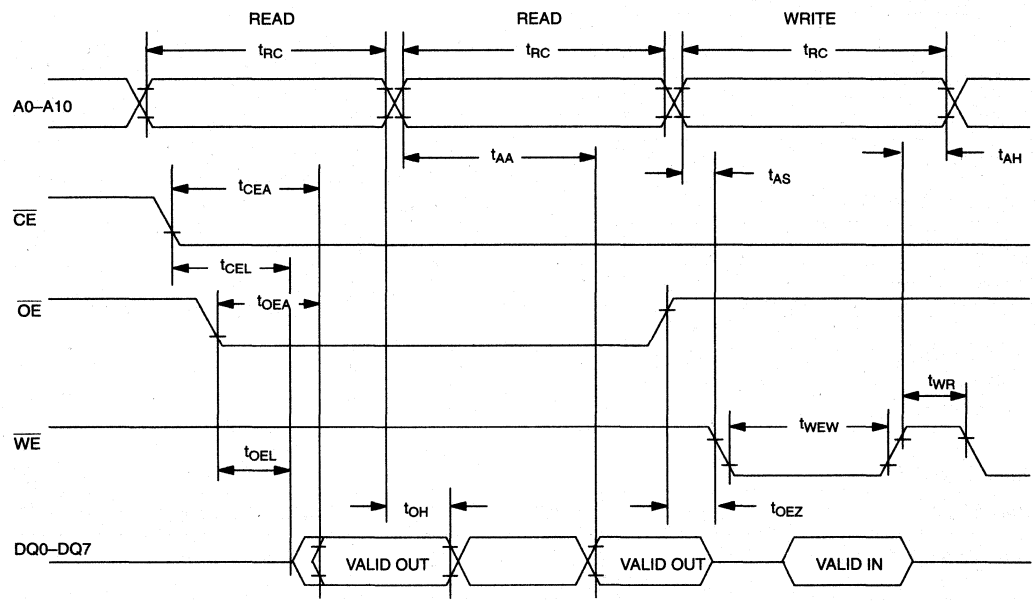
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	C_I			7	pF	
Capacitance on DQ pins	C_{DQ}			10	pF	

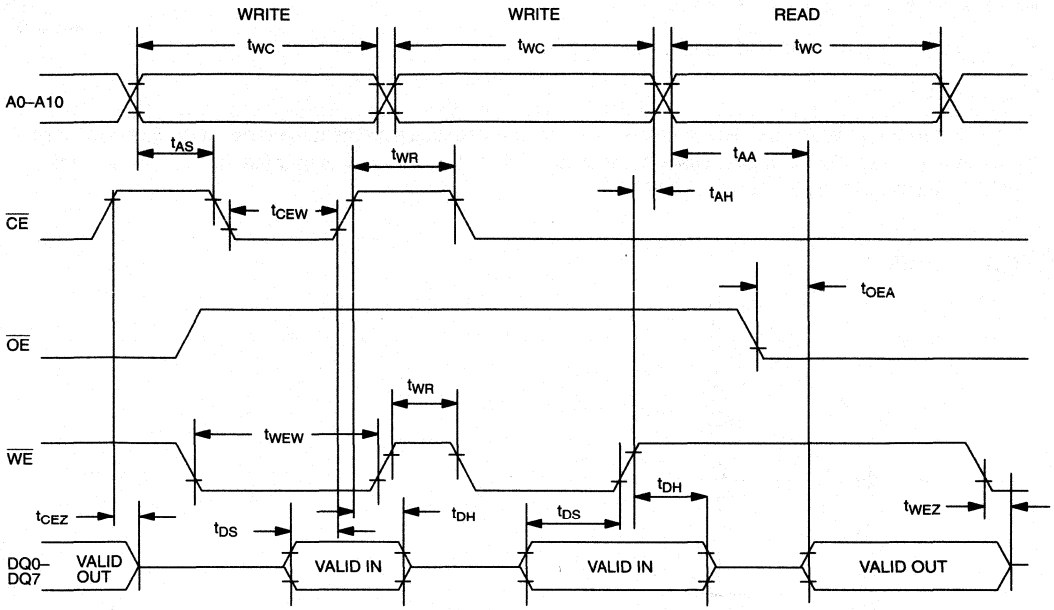
AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} before Power Down	t_{PD}	0			µs	
V_{PF} (Max) to V_{PF} (Min) V_{CC} Fall Time	t_F	300			µs	
V_{PF} (Min) to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{SO} to V_{PF} (Min) V_{CC} Rise Time	t_{RB}	1			µs	
V_{PF} (Min) to V_{PF} (Max) V_{CC} Rise Time	t_R	0			µs	
Power Up	t_{REC}	15	25	35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4

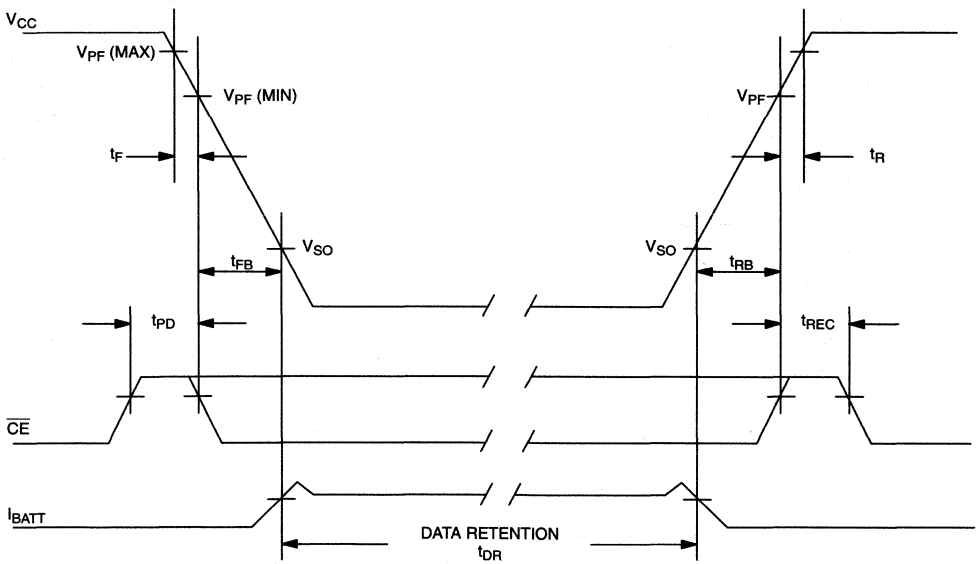
DS1642 READ CYCLE TIMING



DS1642 WRITE CYCLE TIMING



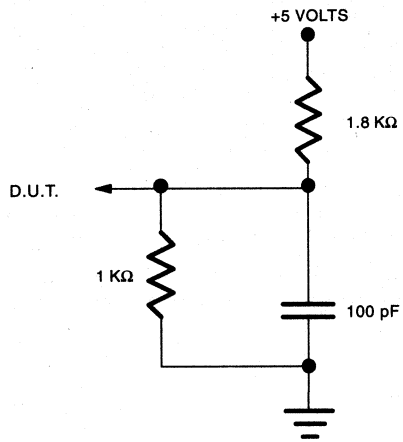
POWER DOWN/POWER UP TIMING



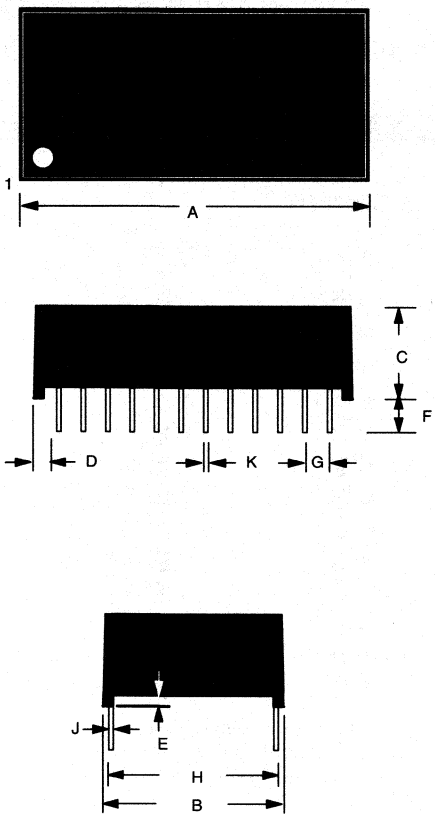
NOTES:

1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Data retention time is at 25°C and is calculated from the date code on the device packag. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225, would mean the 25th week of 1992.

OUTPUT LOAD



DS1642 24–PIN PACKAGE



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.270	1.290
MM	37.34	37.85
B IN.	0.675	0.700
MM	17.15	17.78
C IN.	0.315	0.335
MM	8.00	8.51
D IN.	0.075	0.105
MM	1.91	2.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.140	0.180
MM	3.56	4.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.010	0.018
MM	0.25	0.45
K IN.	0.015	0.025
MM	0.43	0.58

3

DALLAS SEMICONDUCTOR

DS1643/DS1643LPM
Nonvolatile Timekeeping RAM

FEATURES

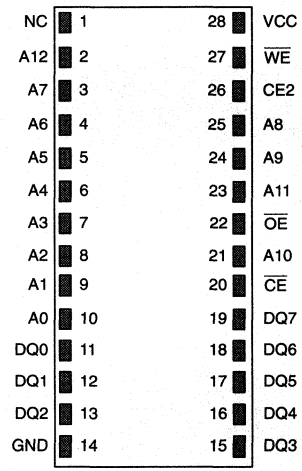
- Form, fit, and function compatible with the MK48T08 Timekeeping RAM
- Integrated NV SRAM, real time clock, crystal, power fail control circuit and lithium energy source
- Standard JEDEC bytewide 8K x 8 static RAM pinout
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 120 ns and 150 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds
- Power fail write protection allows for ±10% V_{CC} power supply tolerance
- Optional Low Profile Module (LPM)
  - Fits into standard 52–pin PLCC surface mountable socket
  - 225 mil package height

ORDERING INFORMATION

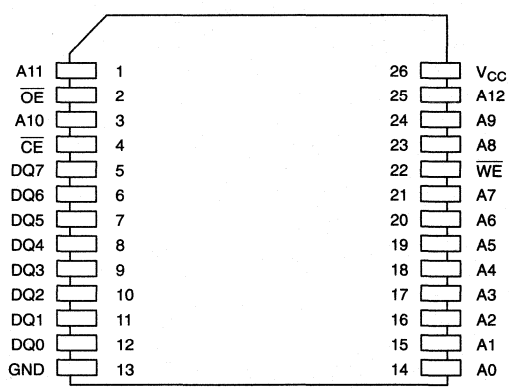
DS1643–XX (28–pin DIP module)
- –12 120 ns access
- –15 150 ns access

DS1643L–XX (Low Profile Module)
- –12 120 ns access
- –15 150 ns access

PIN ASSIGNMENT



28-Pin Encapsulated Package
(700 Mil Extended)



26–Pin Low Profile Module

DESCRIPTION

The DS1643 is an 8K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is pin and function equivalent to any JEDEC standard 8K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The DS1643LPM is a Low Profile Module that fits into a standard 52–pin PLCC surface mountable socket and is functionally equivalent to the DS1643. The

real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1643 also contains its own power fail circuitry which deselects the device when the V_{CC} supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

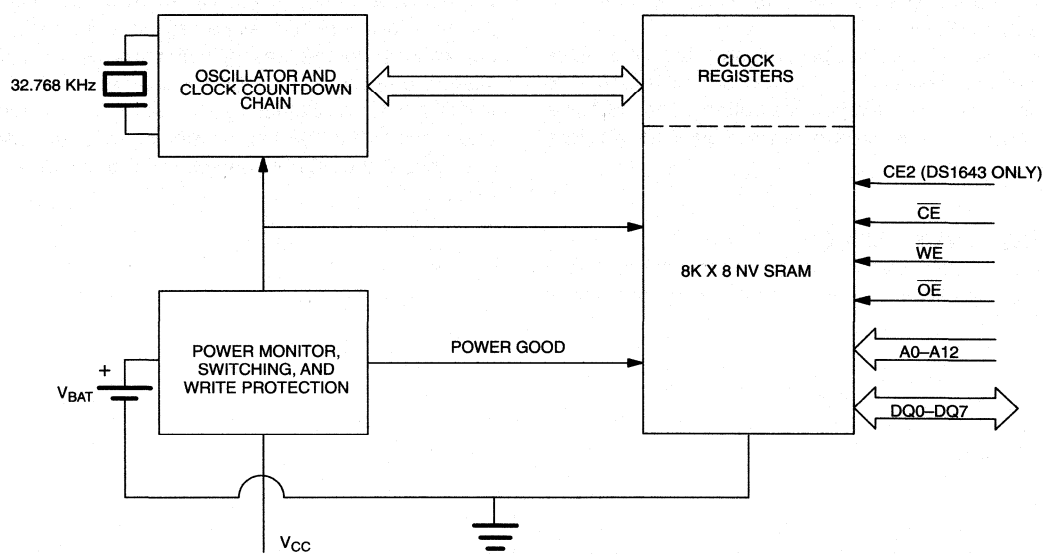
PIN DESCRIPTION

A0-A12	-	Address Input
$\overline{CE}$	-	Chip Enable
CE2	-	Chip Enable 2 (DS1643 only)
$\overline{OE}$	-	Output Enable
$\overline{WE}$	-	Write Enable
NC	-	No Connection
V_{CC}	-	+5 Volts
GND	-	Ground
DQ0-DQ7	-	Data Input/Output

CLOCK OPERATIONS-READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1643 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1643 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

DS1643 BLOCK DIAGRAM Figure 1



DS1643 TRUTH TABLE Table 1

V_{CC}	$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5 VOLTS ± 10%	V_{IH}	X	X	X	DESELECT	HIGH Z	STANDBY
	X	V_{IL}	X	X	DESELECT	HIGH Z	STANDBY
	V_{IL}	V_{IH}	X	V_{IL}	WRITE	DATA IN	ACTIVE
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	READ	DATA OUT	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V_{BAT}	X	X	X	X	DESELECT	HIGH Z	CMOS STANDBY
<V_{BAT}	X	X	X	X	DESELECT	HIGH Z	DATA RETENTION MODE

SETTING THE CLOCK

The eighth bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1643 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume. Note that both the read bit and write bit perform similar functions and setting both bits during the same access cycle will prevent the clock registers from updating.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, CE2 high, and address for seconds register remain valid and stable).

CLOCK ACCURACY

The DS1643 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1643 does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary. Attempts to calibrate the clock that may be used with similar device types (MK48T08 family) will not have any effect even though the DS1643 appears to accept calibration data.

DS1643 REGISTER MAP - BANK1 Table 2

ADDRESS	DATA								FUNCTION	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1FFF	-	-	-	-	-	-	-	-	YEAR	00-99
1FFE	X	X	X	-	-	-	-	-	MONTH	01-12
1FFD	X	X	-	-	-	-	-	-	DATE	01-31
1FFC	X	FT	X	X	X	-	-	-	DAY	01-07
1FFB	X	X	-	-	-	-	-	-	HOUR	00-23
1FFA	X	-	-	-	-	-	-	-	MINUTES	00-59
1FF9	$\overline{OSC}$	-	-	-	-	-	-	-	SECONDS	00-59
1FF8	W	R	-	-	-	-	-	-	CONTROL	A

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

NOTES:

"X" bits are unused but must be set to zero during write cycle to insure proper clock operation.
Bits 0 through 5 of control register A are not dedicated to any particular function and can be used as normal RAM bits.

RETRIEVING DATA FROM RAM OR CLOCK

The DS1643 is in the read mode whenever $\overline{WE}$ (write enable) is high, $\overline{CE}$ (chip enable) is low and CE2 (chip enable 2) is high. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$, CE2 and $\overline{OE}$ access times are satisfied. If $\overline{CE}$, CE2, or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$, CE2, and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$, CE2, and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1643 is in the write mode whenever $\overline{WE}$, $\overline{CE}$, and CE2 are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$, $\overline{CE}$, or CE2. The addresses must be held valid throughout the cycle. $\overline{CE}$, CE2, or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CC} is within nominal limits (V_{CC} > 4.5 volts) the DS1643 can be accessed as described above by read or write cycles. However, when V_{CC} is below the power fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ and CE2 signals. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level.

INTERNAL BATTERY LONGEVITY

The DS1643 has a self contained lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1643 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. The DS1643 is shipped from Dallas Semiconductor with the clock oscillator turned off, so the expected life should be considered to start from the time the clock oscillator is first turned on. Actual life expectancy of the DS1643 will be much longer than 10 years since no internal lithium battery energy is consumed when V_{CC} is present. In fact, in most applications, the life expectancy of the DS1643 will be approximately equal to the shelf life (expected useful life of the lithium battery with no load attached) of the lithium battery which may prove to be as long as 20 years.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-20°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC}+0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C $\leq t_A \leq$ 70°C; V_{CC} =5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		30	55	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH}, CE2 = V_{IL})	I_{CC2}		3	6	mA	2, 3
CMOS Standby Current ($\overline{CE}$=V_{CC}-0.2V, CE2=GND+0.2V)	I_{CC3}		2	4.0	mA	2, 3
Input Leakage Current (any input)	I_{IL}	-1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Write Protection Voltage	V_{TP}	4.0	4.25	4.5	V	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	DS1643-12		DS1643-15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Address Access Time	t_{AA}		120		150	ns	
$\overline{CE}$ and CE2 Access Time	t_{CEA}		120		150	ns	
$\overline{CE}$ and CE2 Data Off Time	t_{CEZ}		40		50	ns	
Output Enable Access Time	t_{OEA}		100		120	ns	
Output Enable Data Off Time	t_{OEZ}		35		45	ns	
Output Enable to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{CE}$ and CE2 to DQ Low-Z	t_{CEL}	5		5		ns	
Output Hold from Address	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Address Setup Time	t_{AS}	0		0		ns	
$\overline{CE}$ and CE2 Pulse Width	t_{CEW}	100		120		ns	
Address Hold from End of Write	t_{AH}	15		20		ns	
Write Pulse Width	t_{WEW}	120		150		ns	
$\overline{WE}$ Data Off Time	t_{WEZ}		40		50	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10		15		ns	
Data Setup Time	t_{DS}	85		110		ns	
Data Hold Time High	t_{DH}	15		20		ns	

AC TEST CONDITIONS

Input Levels: 0V to 3V
Transition Times: 5 ns

CAPACITANCE

(t_A = 25°C)

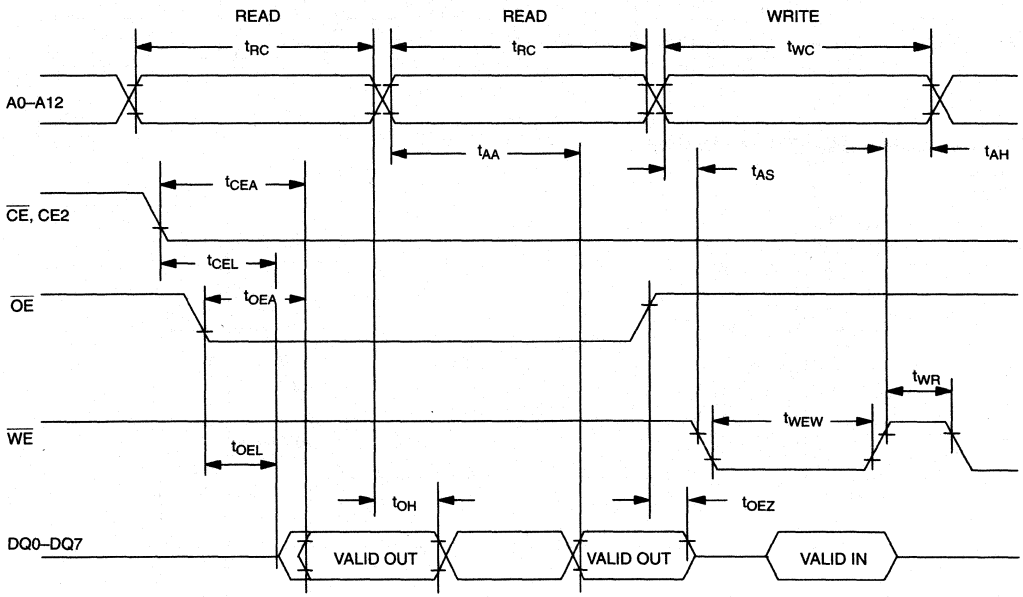
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	C_I			7	pF	
Capacitance on DQ pins	C_{DQ}			10	pF	

AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE2, $\overline{CE}$ or $\overline{WE}$ at V_{IH} before Power Down	t_{PD}	0			µs	
V_{PF} (Max) to V_{PF} (Min) V_{CC} Fall Time	t_F	300			µs	
V_{PF} (Min) to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{SO} to V_{PF} (Min) V_{CC} Rise Time	t_{RB}	1			µs	
V_{PF} (Min) to V_{PF} (Max) V_{CC} Rise Time	t_R	0			µs	
Power Up	t_{REC}	15	25	35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4

3

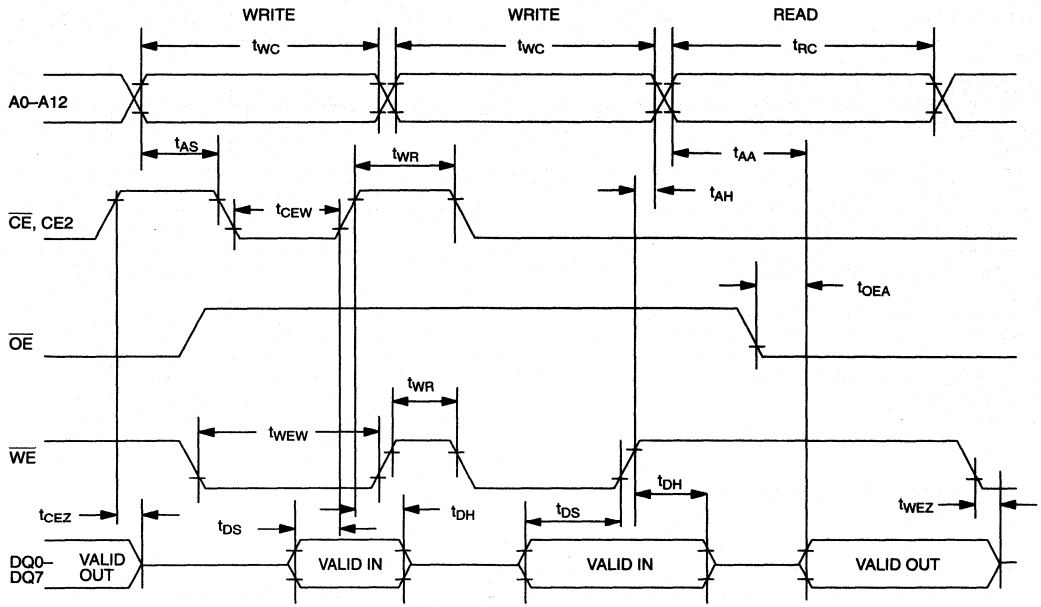
DS1643 READ CYCLE TIMING



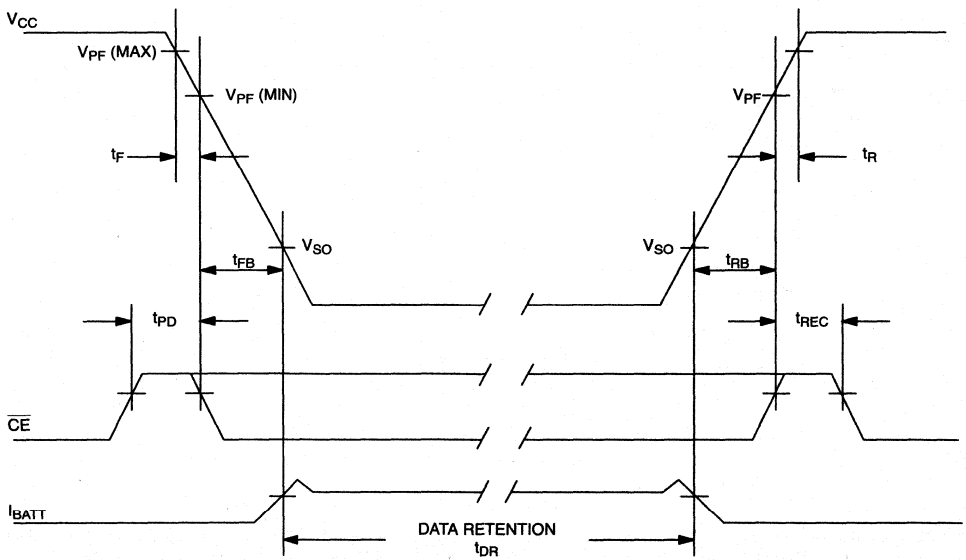
NOTE:

The CE2 control signal functions exactly the same as the $\overline{CE}$ signal except that the logic for active and inactive levels are exactly opposite. All parameters dimensioned to $\overline{CE}$ apply to CE2 with the opposite active state.

DS1643 WRITE CYCLE TIMING



POWER DOWN/POWER UP TIMING

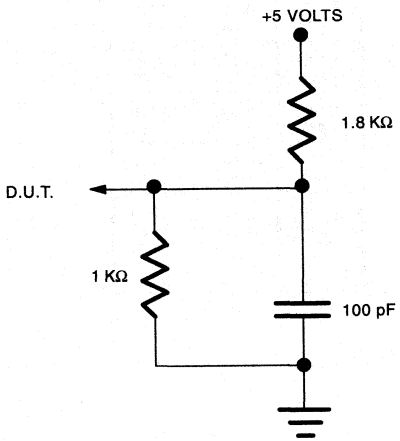


NOTE:
The CE2 control signal functions exactly the same as the $\overline{CE}$ signal except that the logic for active and inactive levels are exactly opposite. All parameters dimensioned to $\overline{CE}$ apply to CE2 with the opposite active state.

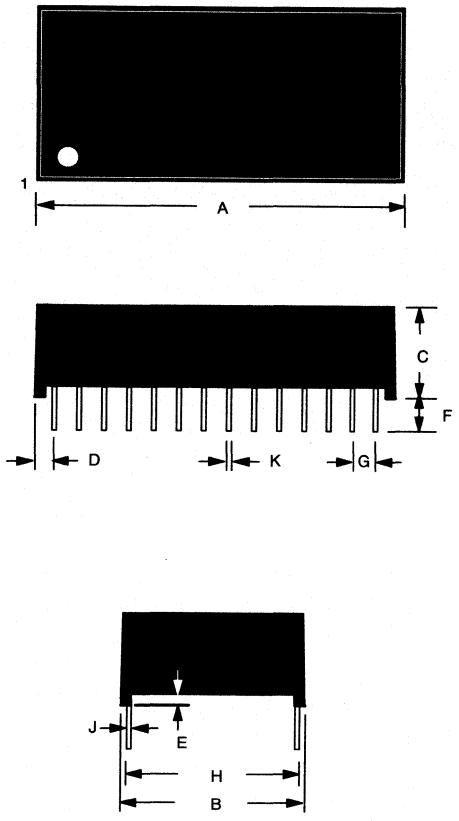
NOTES:

1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Data retention time is at 25°C and is calculated from the date code on the device package. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225, would mean the 25th week of 1992.

OUTPUT LOAD

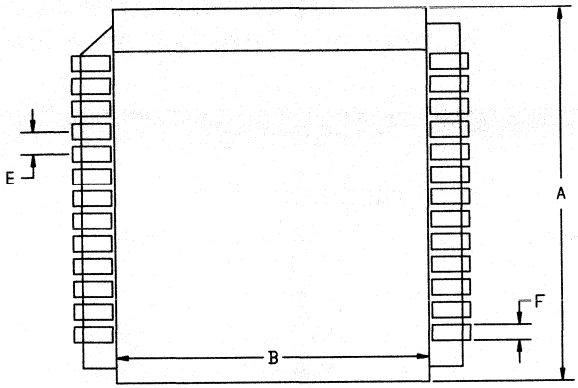


DS1643 28–PIN PACKAGE

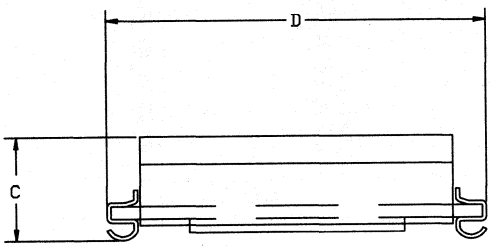


PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.470	1.490
MM	37.34	37.85
B IN.	0.715	0.740
MM	18.16	18.80
C IN.	0.335	0.355
MM	8.51	9.02
D IN.	0.075	0.105
MM	1.91	2.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.140	0.180
MM	3.56	4.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.010	0.018
MM	0.25	0.45
K IN.	0.015	0.025
MM	0.43	0.58

DS1643LPM 26–PIN LOW PROFILE MODULE



PKG	INCHES	
DIM	MIN	MAX
A	0.755	0.780
B	0.640	0.660
C	0.210	0.230
D	0.775	0.795
E	0.047	0.053
F	0.015	0.025



NOTE:
The recommended 52–pin PLCC surface mountable socket to be used with this 26–pin module is: McKenzie P/N# 26P–SMT–3.

DALLAS SEMICONDUCTOR

DS1644/DS1644LPM
Nonvolatile Timekeeping RAM

FEATURES

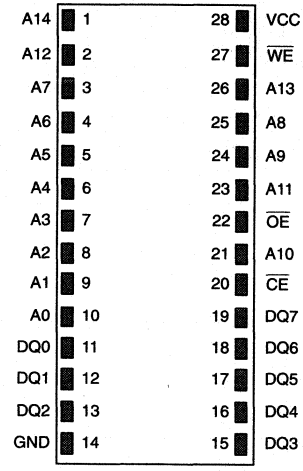
- Upward compatible with the DS1643 Timekeeping RAM
- Integrated NV SRAM, real time clock, crystal, power fail control circuit and lithium energy source
- Optional low profile socketable module
  - Fits into a standard 68–pin PLCC surface mountable socket
  - 255 mil package height
- Standard JEDEC bytewide 32K x 8 static RAM pinout
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access time of 120 ns and 150 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds
- Power fail write protection allows for ±10% V_{CC} power supply tolerance

ORDERING INFORMATION

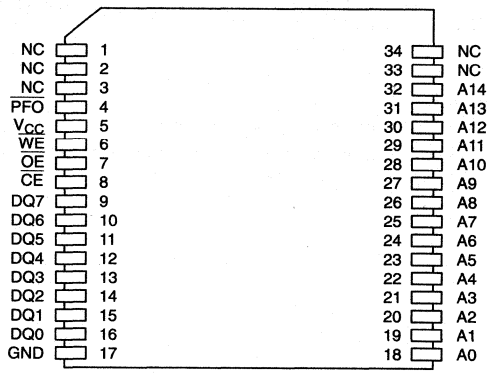
DS1644–XX (28–pin DIP module)
- –12 120 ns access
- –15 150 ns access

DS1644L–XX (Low Profile Module)
- –12 120 ns access
- –15 150 ns access

PIN ASSIGNMENT



28-Pin Encapsulated Package
(720 Mil Extended)



34–Pin Low Profile Module

PIN DESCRIPTION

A0-A14	– Address Input
$\overline{CE}$	– Chip Enable
$\overline{OE}$	– Output Enable
$\overline{WE}$	– Write Enable
V_{CC}	– +5 Volts
GND	– Ground
DQ0-DQ7	– Data Input/Output
NC	– No Connection
$\overline{PFO}$	– Power Fail Output (DS1644LPM only)

DESCRIPTION

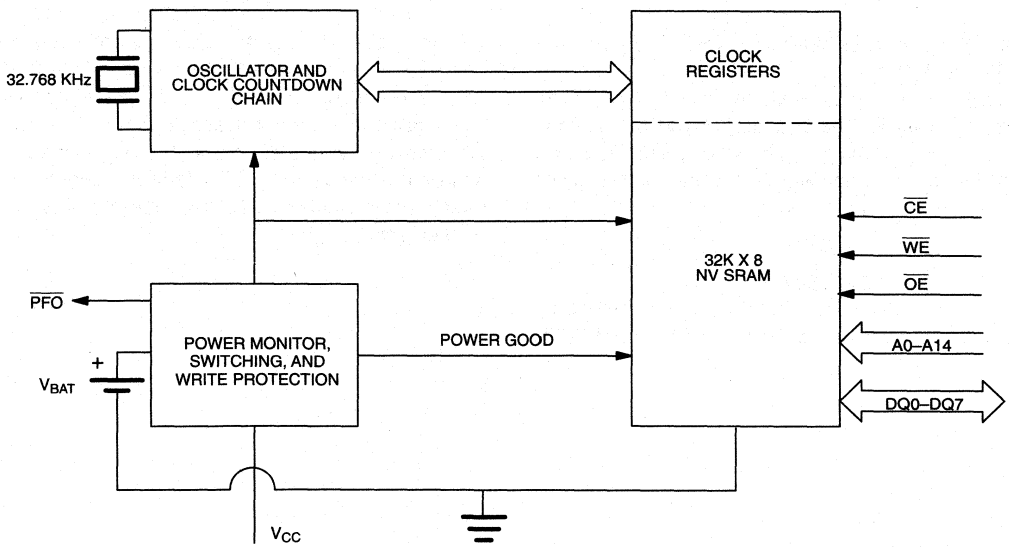
The DS1644LPM is a low profile module that fits into a standard 68–pin PLCC surface mountable socket and is functionally equivalent to the DS1644. The DS1644 is a 32K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a bytewide format. The nonvolatile timekeeping RAM is pin and function equivalent to any JEDEC standard 32K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1644 also contains its own power fail circuitry which deselects the device when the V_{CC} supply is in an out–of–tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

CLOCK OPERATIONS - READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1644 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1644 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

3

DS1644 BLOCK DIAGRAM Figure 1



DS1644 TRUTH TABLE Table 1

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5 VOLTS ± 10%	V_{IH}	X	X	DESELECT	HIGH Z	STANDBY
	X	X	X	DESELECT	HIGH Z	STANDBY
	V_{IL}	X	V_{IL}	WRITE	DATA IN	ACTIVE
	V_{IL}	V_{IL}	V_{IH}	READ	DATA OUT	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V_{BAT}	X	X	X	DESELECT	HIGH Z	CMOS STANDBY
<V_{BAT}	X	X	X	DESELECT	HIGH Z	DATA RETENTION MODE

SETTING THE CLOCK

The eighth bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1644 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume. Note that both the read bit and write bit perform similar functions and setting both bits during the same access cycle will prevent the clock registers from updating.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, and address for seconds register remain valid and stable).

CLOCK ACCURACY

The DS1644 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1644 does not require additional calibration, and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary. Attempts to calibrate the clock that may be used with similar device types (MK48T08 family) will not have any effect even though the DS1644 appears to accept calibration data.

DS1644 REGISTER MAP - BANK1 Table 2

ADDRESS	DATA								FUNCTION	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
7FFF	-	-	-	-	-	-	-	-	YEAR	00-99
7FFE	X	X	X	-	-	-	-	-	MONTH	01-12
7FFD	X	X	-	-	-	-	-	-	DATE	01-31
7FFC	X	FT	X	X	X	-	-	-	DAY	01-07
7FFB	X	X	-	-	-	-	-	-	HOUR	00-23
7FFA	X	-	-	-	-	-	-	-	MINUTES	00-59
7FF9	$\overline{OSC}$	-	-	-	-	-	-	-	SECONDS	00-59
7FF8	W	R	-	-	-	-	-	-	CONTROL	A

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

NOTES:
"X" bits are unused but must be set to zero during write cycle to insure proper clock operation.

Bits 0 through 5 of control register A are not dedicated to any particular function and can be used as normal RAM bits.

RETRIEVING DATA FROM RAM OR CLOCK

The DS1644 is in the read mode whenever $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1644 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring high to low transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CC} is within nominal limits (V_{CC} > 4.5 volts) the DS1644 can be accessed as described above with read or write cycles. However, when V_{CC} is below the power fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM are blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. At this time the power fail output signal ($\overline{PFO}$) will be driven active low and will remain active until V_{CC} returns to nominal levels. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level.

INTERNAL BATTERY LONGEVITY

The DS1644 has a self contained lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1644 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. The DS1644 is shipped from Dallas Semiconductor with the clock oscillator turned off, so the expected life should be considered to start from the time the clock oscillator is first turned on. Actual life expectancy of the DS1644 will be much longer than 10 years since no internal lithium battery energy is consumed when V_{CC} is present. In fact, in most applications, the life expectancy of the DS1644 will be approximately equal to the shelf life (expected useful life of the lithium battery with no load attached) of the lithium battery which may prove to be as long as 20 years.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–20°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC}+0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS (0°C $\leq t_A \leq$ 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}			60	mA	3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC2}			6	mA	3
CMOS Standby Current ($\overline{CE}$=V_{CC}-0.2V)	I_{CC3}			4.0	mA	3
Input Leakage Current (any input)	I_{IL}	-1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Write Protection Voltage	V_{PF}	4.0	4.25	4.5	V	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	DS1644-12		DS1644-15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Address Access Time	t_{AA}		120		150	ns	
$\overline{CE}$ Access Time	t_{CEA}		120		150	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		40		50	ns	
Output Enable Access Time	t_{OEA}		100		120	ns	
Output Enable Data Off Time	t_{OEZ}		40		50	ns	
Output Enable to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns	
Output Hold from Address	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Address Setup Time	t_{AS}	0		0		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	100		120		ns	
Address Hold from End of Write	t_{AH}	15		20		ns	
Write Pulse Width	t_{WEW}	120		150		ns	
$\overline{WE}$ Data Off Time	t_{WEZ}		40		50	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10		15		ns	
Data Setup Time	t_{DS}	85		110		ns	
Data Hold Time High	t_{DH}	15		20		ns	

AC TEST CONDITIONS

Input Levels: 0V to 3V
Transition Times: 5 ns

CAPACITANCE

(t_A = 25°C)

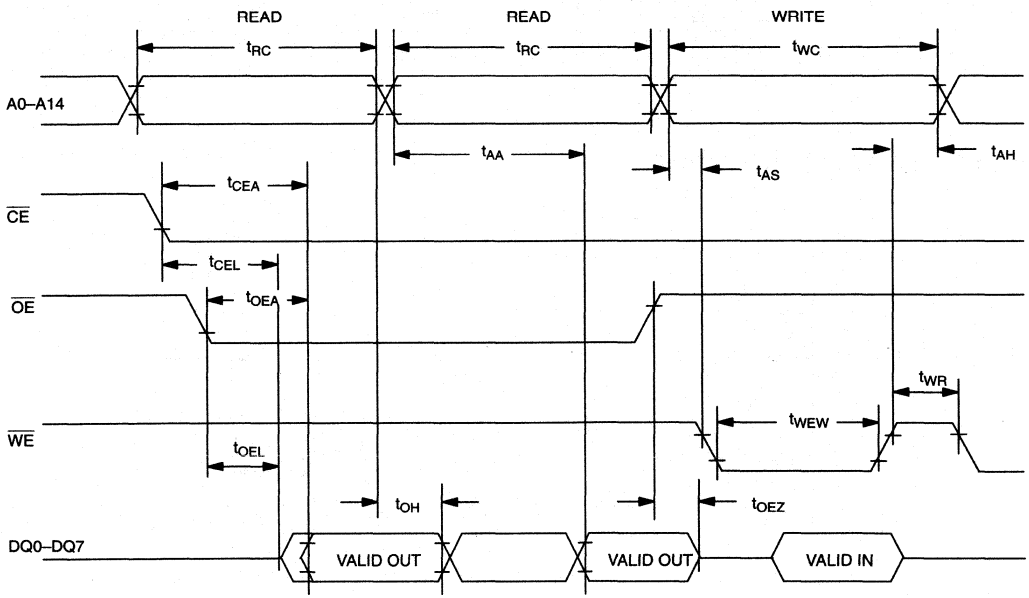
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	C_I			7	pF	
Capacitance on DQ pins	C_{DQ}			10	pF	

AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C to 70°C)

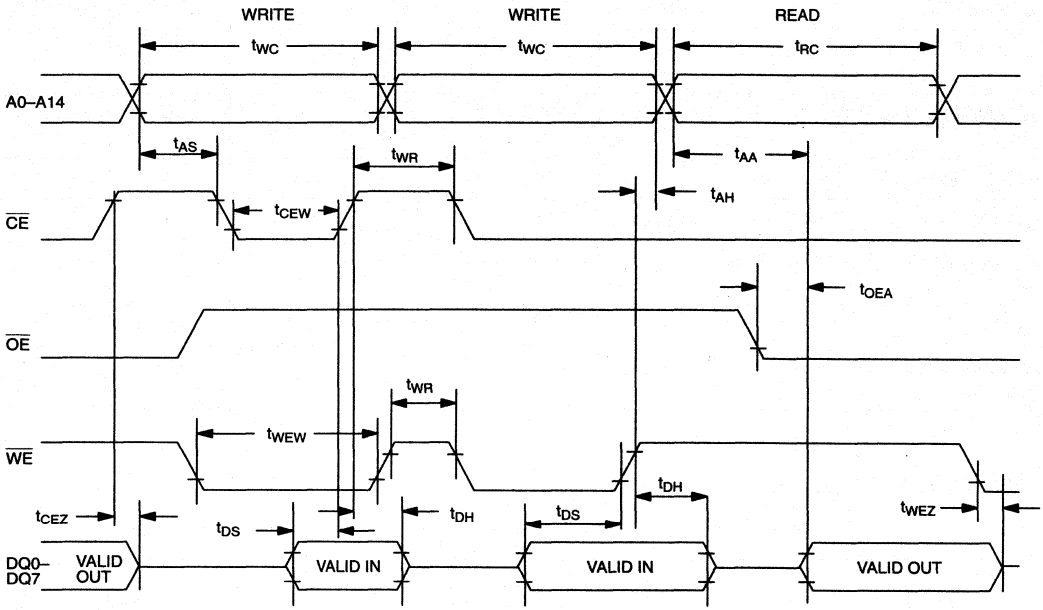
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} before Power Down	t_{PD}	0			µs	
V_{PF} (Max) to V_{PF} (Min) V_{CC} Fall Time	t_F	300			µs	
V_{PF} (Min) to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{SO} to V_{PF} (Min) V_{CC} Rise Time	t_{RB}	1			µs	
V_{PF} (Min) to V_{PF} (Max) V_{CC} Rise Time	t_R	0			µs	
Power Up	t_{REC}	15	25	35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4

3

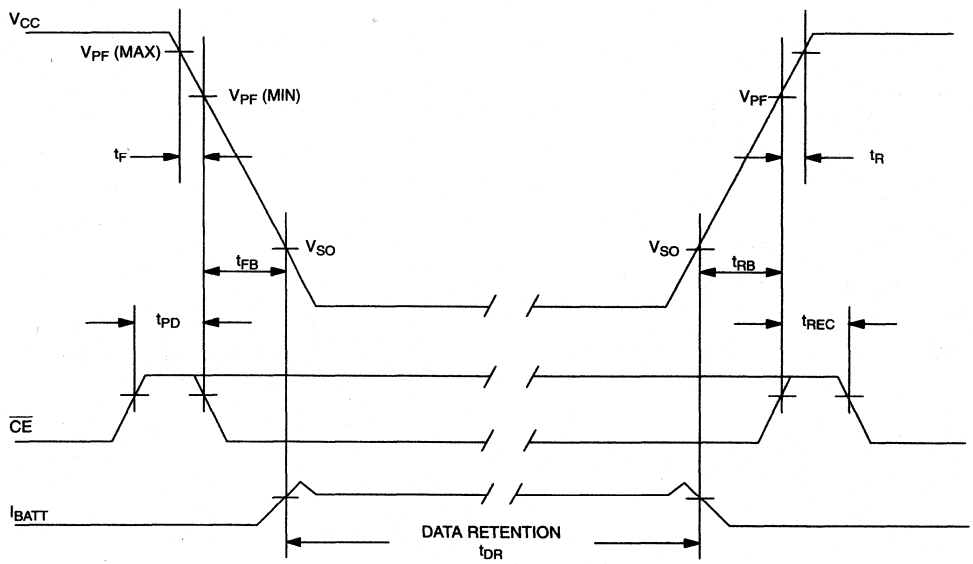
DS1644 READ CYCLE TIMING



DS1644 WRITE CYCLE TIMING



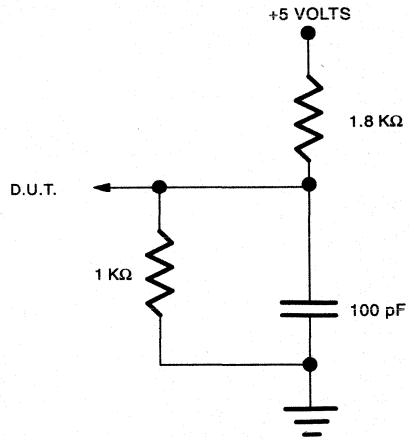
POWER DOWN/POWER UP TIMING



NOTES:

1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Data retention time is at 25°C and is calculated from the date code on the device package. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225, would mean the 25th week of 1992.

OUTPUT LOAD



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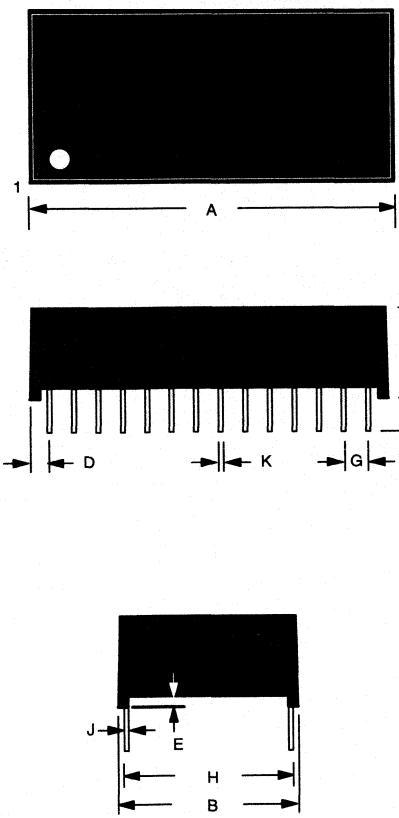
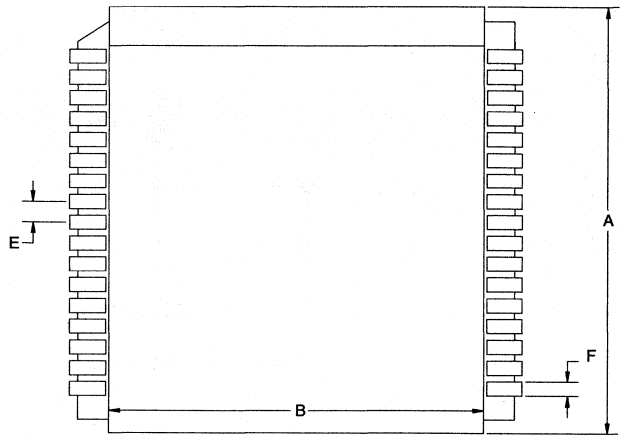
DS1644 28–PIN PACKAGE

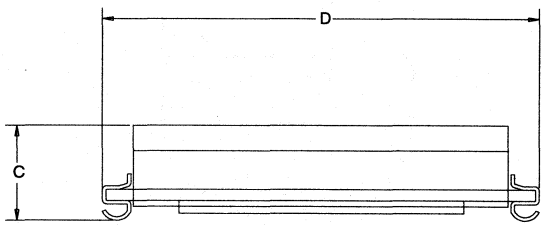


PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.470	1.490
MM	37.34	37.85
B IN.	0.715	0.740
MM	18.16	18.80
C IN.	0.335	0.365
MM	8.51	9.27
D IN.	0.075	0.105
MM	1.91	2.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.140	0.180
MM	3.56	4.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.010	0.018
MM	0.25	0.45
K IN.	0.015	0.025
MM	0.38	0.64

DS1644LPM 34–PIN LOW PROFILE MODULE



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.047	0.053
F	0.015	0.025



NOTE:
The recommended 68–pin PLCC surface mountable socket to be used with this 34–pin module is: McKenzie P/N# 34P–SMT–3. The McKenzie socket plus the DS1644LPM has the following approximate dimensions: length, width = 1.22", height = 0.255".

DALLAS SEMICONDUCTOR

DS1646/DS1646LPM
Nonvolatile Timekeeping RAM

3

FEATURES

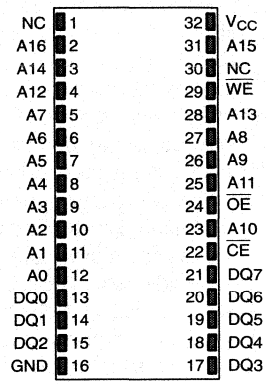
- Optional low profile socketable module
  - Fits into a standard 68–pin PLCC surface mountable socket
  - 250 mil package height
- Integrated NV SRAM, real time clock, crystal, power fail control circuit and lithium energy source
- Standard JEDEC bytewide 128K x 8 static RAM pin-out
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 120 ns and 150 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds
- Power fail write protection allows for ±10% V_{CC} power supply tolerance

ORDERING INFORMATION

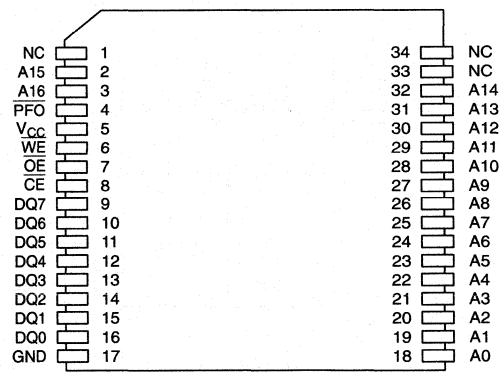
DS1646–XX (32–pin DIP module)
- –12 120 ns access
- –15 150 ns access

DS1646L–XX (Low Profile Module)
- –12 120 ns access
- –15 150 ns access

PIN ASSIGNMENT



128K X 8
32-Pin Encapsulated Package



34–Pin Low Profile Module
(Scheduled Availability is QTR 3 1994)

PIN DESCRIPTION

A0-A16	–	Address Input
$\overline{CE}$	–	Chip Enable
$\overline{OE}$	–	Output Enable
$\overline{WE}$	–	Write Enable
V_{CC}	–	+5 Volts
GND	–	Ground
DQ0-DQ7	–	Data Input/Output
NC	–	No Connect
$\overline{PFO}$	–	Power Fail Output (DS1646LPM only)

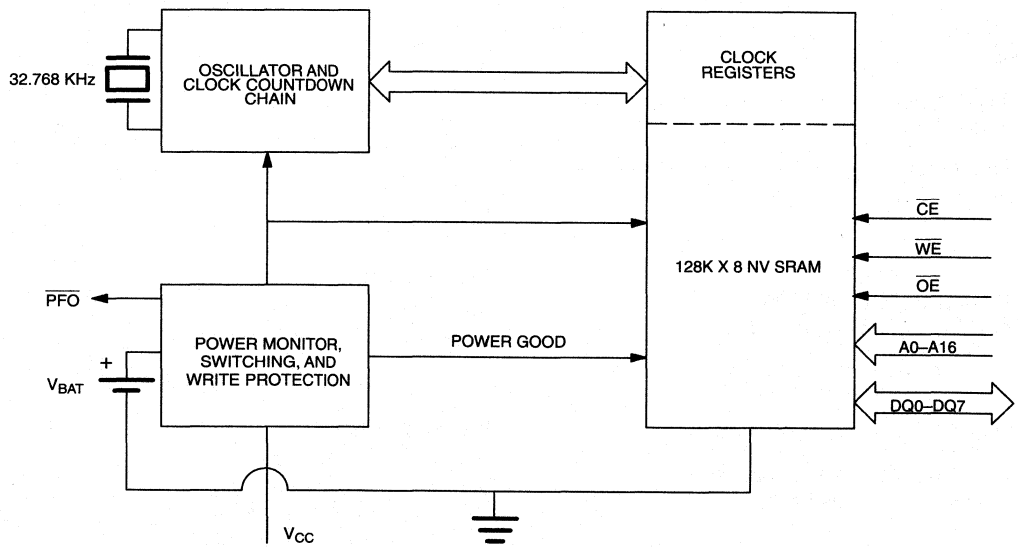
DESCRIPTION

The DS1646LPM is a low profile module that fits into a standard 68–pin PLCC surface mountable socket and is functionally equivalent to the DS1646. The DS1646 is a 128K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is pin and function equivalent to any JEDEC standard 128K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1646 also contains its own power fail circuitry which deselects the device when the V_{CC} supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

CLOCK OPERATIONS-READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1646 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1646 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

BLOCK DIAGRAM DS1646 Figure 1



TRUTH TABLE DS1646 Table 1

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5 VOLTS ± 10%	V_{IH}	X	X	DESELECT	HIGH Z	STANDBY
	X	X	X	DESELECT	HIGH Z	STANDBY
	V_{IL}	X	V_{IL}	WRITE	DATA IN	ACTIVE
	V_{IL}	V_{IL}	V_{IH}	READ	DATA OUT	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V_{BAT}	X	X	X	DESELECT	HIGH Z	CMOS STANDBY
<V_{BAT}	X	X	X	DESELECT	HIGH Z	DATA RETENTION MODE

SETTING THE CLOCK

The eighth bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1646 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume. Note that both the read bit and write bit perform similar functions and setting both bits during the same access cycle will prevent the clock registers from updating.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, and address for seconds register remain valid and stable).

CLOCK ACCURACY

The DS1646 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1646 does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary.

DS1646 REGISTER MAP - BANK1 Table 2

ADDRESS	DATA								FUNCTION	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1FFFF	-	-	-	-	-	-	-	-	YEAR	00-99
1FFFE	X	X	X	-	-	-	-	-	MONTH	01-12
1FFFD	X	X	-	-	-	-	-	-	DATE	01-31
1FFFC	X	FT	X	X	X	-	-	-	DAY	01-07
1FFFB	X	X	-	-	-	-	-	-	HOUR	00-23
1FFFA	X	-	-	-	-	-	-	-	MINUTES	00-59
1FFF9	$\overline{OSC}$	-	-	-	-	-	-	-	SECONDS	00-59
1FFF8	W	R	-	-	-	-	-	-	CONTROL	A

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

NOTES:

"X" bits are unused but must be set to zero during write cycle to insure proper clock operation.

Bits 0 through 5 of control register A are not dedicated to any particular function and can be used as normal RAM bits.

RETRIEVING DATA FROM RAM OR CLOCK

The DS1646 is in the read mode whenever $\overline{WE}$ (write enable) is high, $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1646 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring high to low transition of $\overline{WE}$ and $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CC} is within nominal limits (V_{CC} > 4.5 volts) the DS1646 can be accessed as described above with read or write cycles. However, when V_{CC} is below the power fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. At this time the power fail output signal ($\overline{PFO}$) will be driven active low and will remain active until V_{CC} returns to nominal levels. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level.

INTERNAL BATTERY LONGEVITY

The DS1646 has a self contained lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1646 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. The DS1646 is shipped from Dallas Semiconductor with the clock oscillator turned off, so the expected life should be considered to start from the time the clock oscillator is first turned on. Actual life expectancy of the DS1646 will be much longer than 10 years since no internal lithium battery energy is consumed when V_{CC} is present. In fact, in most applications, the life expectancy of the DS1646 will be approximately equal to the shelf life (expected useful life of the lithium battery with no load attached) of the lithium battery which may prove to be as long as 20 years.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–20°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC}+0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C $\leq t_A \leq$ 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		30	55	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC2}		3	6	mA	2, 3
CMOS Standby Current ($\overline{CE}$=V_{CC}-0.2V)	I_{CC3}		2	4.0	mA	2, 3
Input Leakage Current (any input)	I_{IL}	-1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Write Protection Voltage	V_{PF}	4.0	4.25	4.5	V	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V + 10%)

PARAMETER	SYMBOL	DS1646-12		DS1646-15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Address Access Time	t_{AA}		120		150	ns	
$\overline{CE}$ Access Time	t_{CEA}		120		150	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		40		50	ns	
Output Enable Access Time	t_{OEA}		100		120	ns	
Output Enable Data Off Time	t_{OEZ}		40		50	ns	
Output Enable to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns	
Output Hold from Address	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Address Setup Time	t_{AS}	0		0		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	100		120		ns	
Address Hold from End of Write	t_{AH}	15		20		ns	
Write Pulse Width	t_{WEW}	120		150		ns	
$\overline{WE}$ Data Off Time	t_{WEZ}		40		50	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10		15		ns	
Data Setup Time	t_{DS}	85		110		ns	
Data Hold Time High	t_{DH}	15		20		ns	

AC TEST CONDITIONS

Input Levels: 0V to 3V
Transition Times: 5 ns

CAPACITANCE

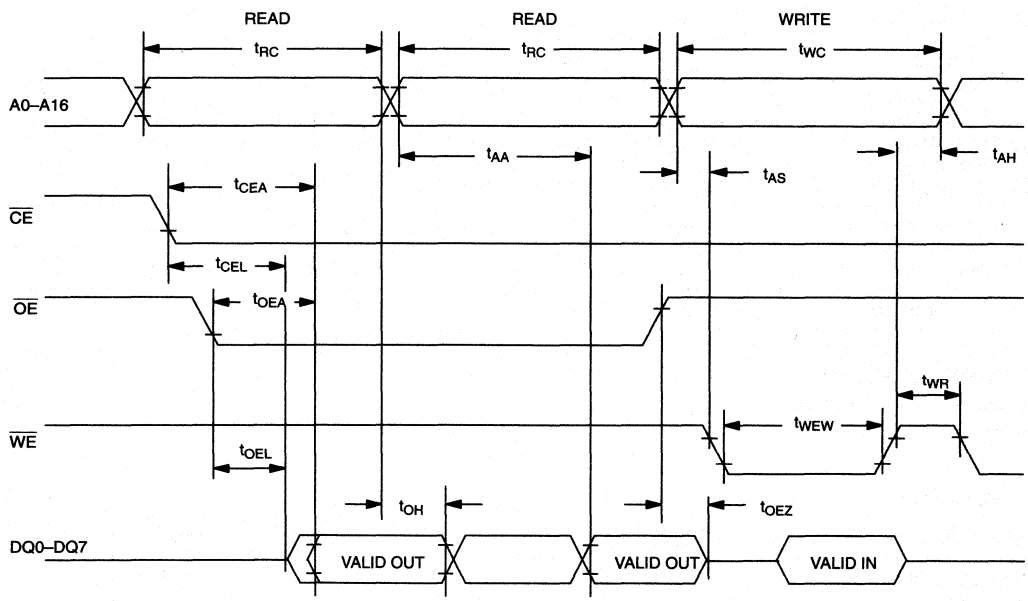
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	C_I			7	pF	
Capacitance on DQ pins	C_{DQ}			10	pF	

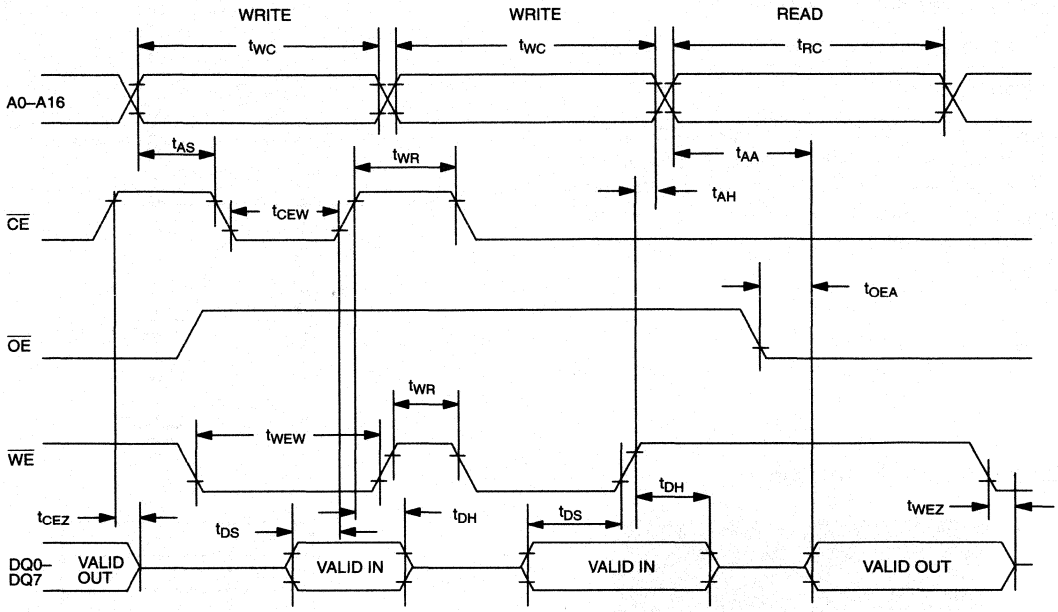
AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} before Power Down	t_{PD}	0			µs	
V_{PF} (Max) to V_{PF} (Min) V_{CC} Fall Time	t_F	300			µs	
V_{PF} (Min) to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{SO} to V_{PF} (Min) V_{CC} Rise Time	t_{RB}	1			µs	
V_{PF} (Min) to V_{PF} (Max) V_{CC} Rise Time	t_R	0			µs	
Power Up	t_{REC}	15	25	35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4

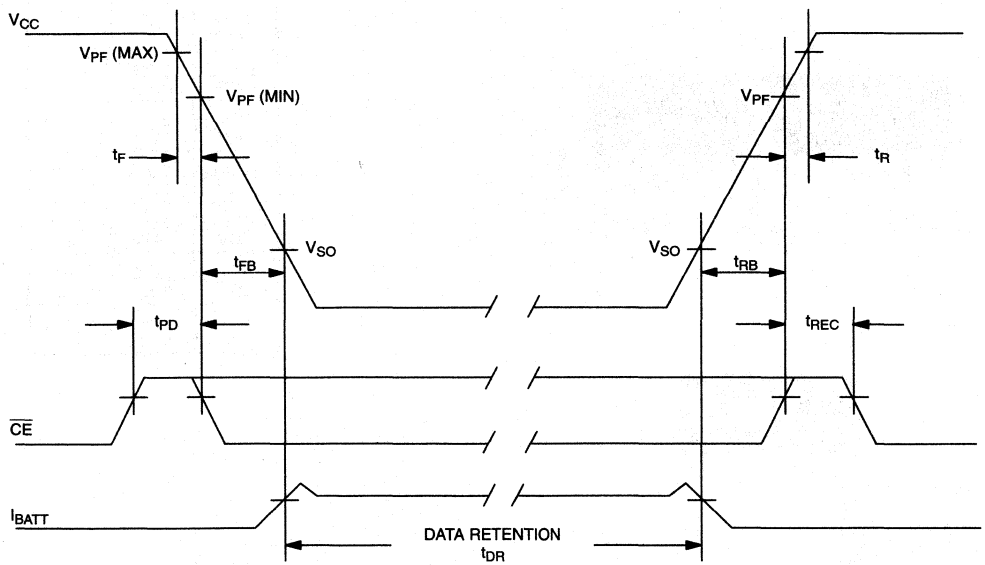
DS1646 READ CYCLE TIMING



DS1646 WRITE CYCLE TIMING



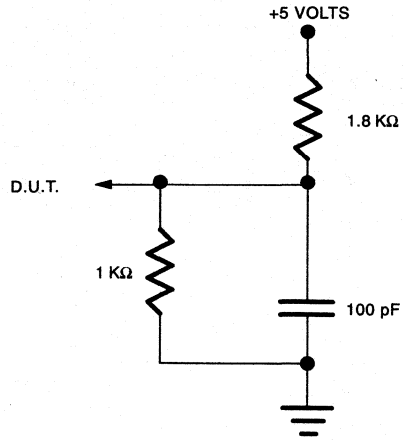
POWER DOWN/POWER UP TIMING



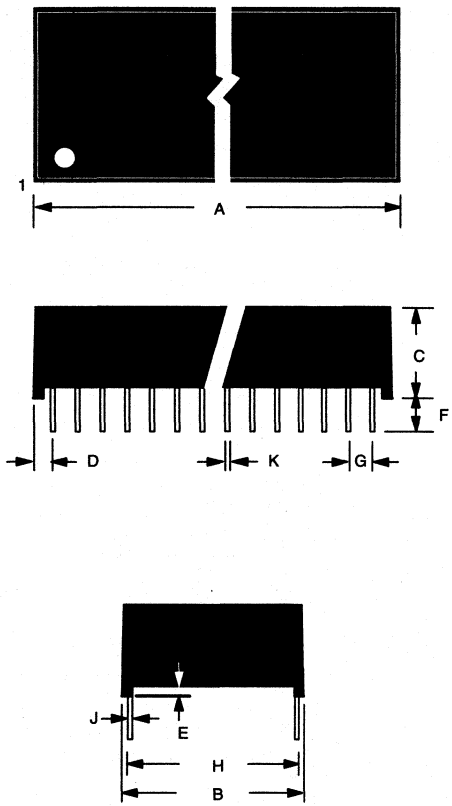
NOTES:

1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Data retention time is at 25°C and is calculated from the date code on the device package. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225, would mean the 25th week of 1992.

OUTPUT LOAD

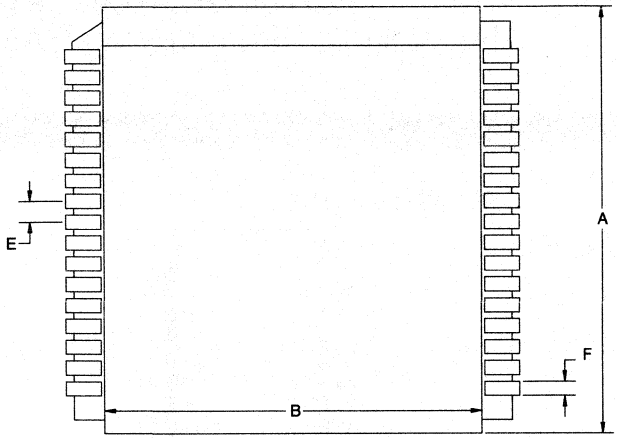


DS1646 32–PIN PACKAGE

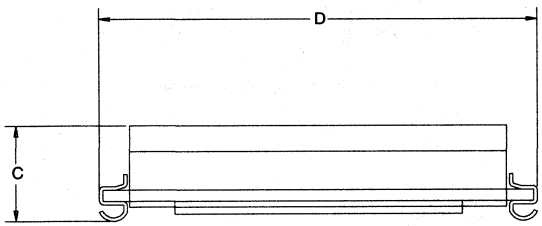


PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.670	1.690
MM	38.42	38.93
B IN.	0.715	0.740
MM	18.16	18.80
C IN.	0.335	0.365
MM	8.51	9.27
D IN.	0.075	0.105
MM	1.91	0.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.140	0.180
MM	3.56	4.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.010	0.018
MM	0.25	0.45
K IN.	0.015	0.025
MM	0.38	0.64

DS1646LPM 34–PIN LOW PROFILE MODULE



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.970
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.047	0.053
F	0.015	0.025



NOTE:
The recommended 68–pin PLCC surface mountable socket to be used with this 34–pin module is: McKenzie P/N# 34P–SMT–3. The McKenzie socket plus the DS1646LPM has the following approximate dimensions: length, width = 1.22", height = 0.255".

PRELIMINARY

DALLAS SEMICONDUCTOR

DS1647/DS1647LPM
Nonvolatile Timekeeping RAM

FEATURES

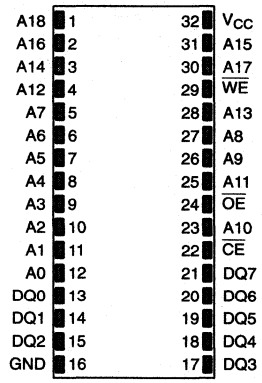
- Integrated NV SRAM, real time clock, crystal, power fail control circuit and lithium energy source
- Optional low profile socketable module
  - Fits into a standard 68–pin PLCC surface mountable socket
  - 255 mil package height
- Standard JEDEC bytewide 512K x 8 static RAM pin-out
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 120 ns and 150 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds
- Power fail write protection allows for ±10% V_{CC} power supply tolerance

ORDERING INFORMATION

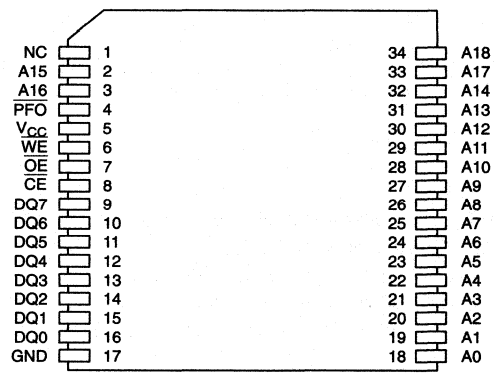
DS1647–XX (32–pin DIP Module)
- –12 120 ns access
- –15 150 ns access

DS1647L–XX (Low Profile Module)
- –12 120 ns access
- –15 150 ns access

PIN ASSIGNMENT



512K X 8
32-Pin Encapsulated Package



34–Pin Low Profile Module

PIN DESCRIPTION

A0-A18	-	Address Input
$\overline{CE}$	-	Chip Enable
$\overline{OE}$	-	Output Enable
$\overline{WE}$	-	Write Enable
V_{CC}	-	+5 Volts
GND	-	Ground
DQ0-DQ7	-	Data Input/Output
NC	–	No Connection
$\overline{PFO}$	–	Power Fail Output (DS1647LPM only)

DESCRIPTION

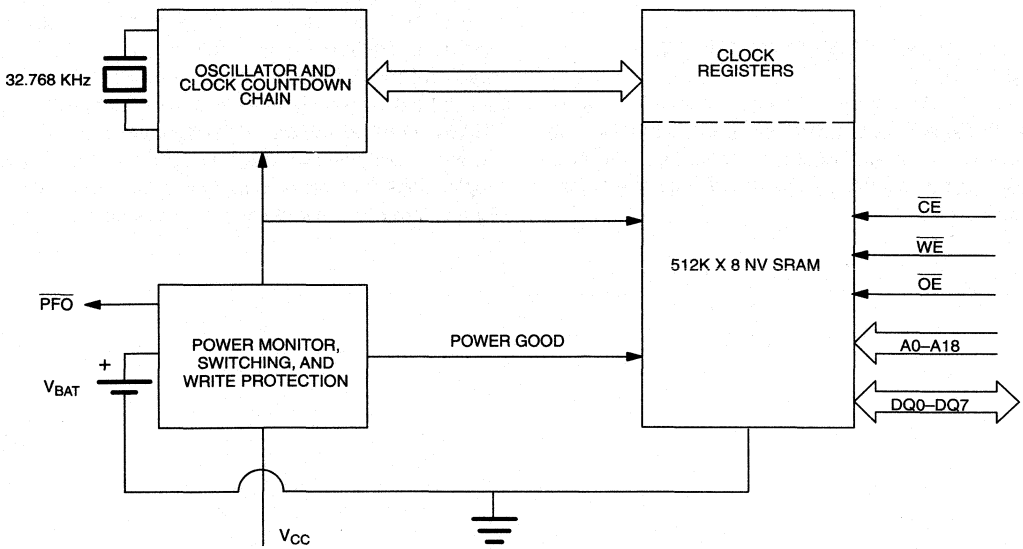
The DS1647LPM is a low profile module that fits into a standard 68–pin PLCC surface mountable socket and is functionally equivalent to the DS1647. The DS1647 is a 512K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is pin and function equivalent to any JEDEC standard 512K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1647 also contains its own power fail circuitry which deselects the device when the V_{CC} supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

CLOCK OPERATIONS-READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1647 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1647 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

3

BLOCK DIAGRAM DS1647 Figure 1



TRUTH TABLE DS1647 Table 1

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5 VOLTS ± 10%	V_{IH}	X	X	DESELECT	HIGH Z	STANDBY
	X	X	X	DESELECT	HIGH Z	STANDBY
	V_{IL}	X	V_{IL}	WRITE	DATA IN	ACTIVE
	V_{IL}	V_{IL}	V_{IH}	READ	DATA OUT	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V_{BAT}	X	X	X	DESELECT	HIGH Z	CMOS STANDBY
<V_{BAT}	X	X	X	DESELECT	HIGH Z	DATA RETENTION MODE

SETTING THE CLOCK

The eighth bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1647 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume. Note that both the read bit and write bit perform similar functions and setting both bits during the same access cycle will prevent the clock registers from updating.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, and address for seconds register remain valid and stable).

CLOCK ACCURACY

The DS1647 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1647 does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary.

DS1647 REGISTER MAP - BANK1 Table 2

ADDRESS	DATA								FUNCTION	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
7FFFF	-	-	-	-	-	-	-	-	YEAR	00-99
7FFFE	X	X	X	-	-	-	-	-	MONTH	01-12
7FFFD	X	X	-	-	-	-	-	-	DATE	01-31
7FFFC	X	FT	X	X	X	-	-	-	DAY	01-07
7FFFB	X	X	-	-	-	-	-	-	HOUR	00-23
7FFFA	X	-	-	-	-	-	-	-	MINUTES	00-59
7FFF9	$\overline{OSC}$	-	-	-	-	-	-	-	SECONDS	00-59
7FFF8	W	R	-	-	-	-	-	-	CONTROL	A

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

NOTES

"X" bits are unused but must be set to zero during write cycle to insure proper clock operation.

Bits 0 through 5 of control register A are not dedicated to any particular function and can be used as normal RAM bits.

RETRIEVING DATA FROM RAM OR CLOCK

The DS1647 is in the read mode whenever $\overline{WE}$ (write enable) is high, $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1647 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring high to low transition of $\overline{WE}$ and $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CCI} is within nominal limits (V_{CC} > 4.5 volts) the DS1647 can be accessed as described above with read or write cycles. However, when V_{CC} is below the power fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. At this time the power fail output signal ($\overline{PFO}$) will be driven active low and will remain active until V_{CC} returns to nominal levels. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level.

INTERNAL BATTERY LONGEVITY

The DS1647 has a self contained lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1647 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 7 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. The DS1647 is shipped from Dallas Semiconductor with the clock oscillator turned off, so the expected life should be considered to start from the time the clock oscillator is first turned on. Actual life expectancy of the DS1647 will be much longer than 7 years since no internal lithium battery energy is consumed when V_{CC} is present. In fact, in most applications, the life expectancy of the DS1647 will be approximately equal to the shelf life (expected useful life of the lithium battery with no load attached) of the lithium battery which may prove to be as long as 20 years.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–20°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

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RECOMMENDED DC OPERATING CONDITIONS

(0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC}+0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C $\leq t_A \leq$ +70°C; V_{CC} =5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		30	55	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC2}		3	6	mA	2, 3
CMOS Standby Current ($\overline{CE}$=V_{CC}-0.2V)	I_{CC3}		2	4.0	mA	2, 3
Input Leakage Current (any input)	I_{IL}	-1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Write Protection Voltage	V_{PF}	4.0	4.25	4.5	V	

AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C; V_{CC} = 5.0V + 10%)

PARAMETER	SYMBOL	DS1647-12		DS1647-15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Address Access Time	t_{AA}		120		150	ns	
$\overline{CE}$ Access Time	t_{CEA}		120		150	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		40		50	ns	
Output Enable Access Time	t_{OEA}		100		120	ns	
Output Enable Data Off Time	t_{OEZ}		40		50	ns	
Output Enable to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns	
Output Hold from Address	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Address Setup Time	t_{AS}	0		0		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	100		120		ns	
Address Hold from End of Write	t_{AH}	15		20		ns	
Write Pulse Width	t_{WEW}	120		150		ns	
$\overline{WE}$ Data Off Time	t_{WEZ}		40		50	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10		15		ns	
Data Setup Time	t_{DS}	85		110		ns	
Data Hold Time High	t_{DH}	15		20		ns	

AC TEST CONDITIONS

Input Levels: 0V TO 3V
Transition Times: 5 ns

CAPACITANCE

(t_A = 25°C)

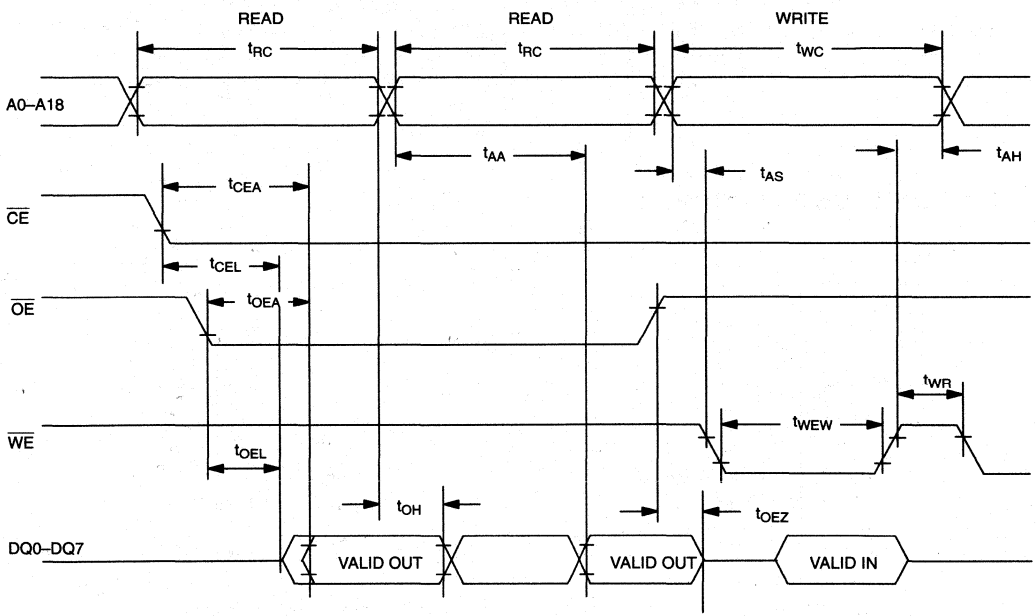
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	C_I			7	pF	
Capacitance on DQ pins	C_{DQ}			10	pF	

AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C to +70°C)

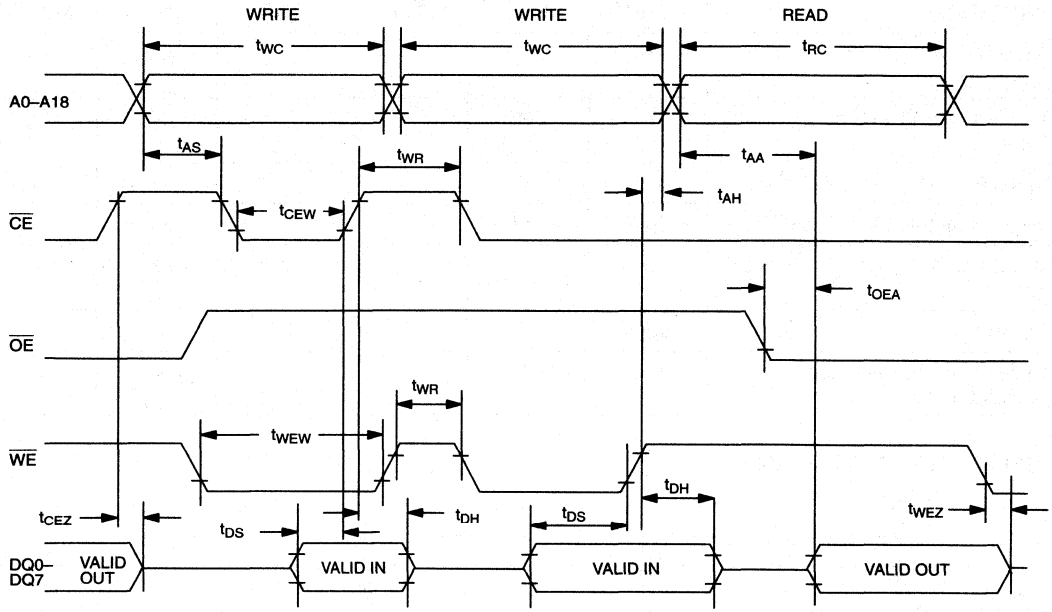
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} before Power Down	t_{PD}	0			µs	
V_{PF} (Max) to V_{PF} (Min) V_{CC} Fall Time	t_F	300			µs	
V_{PF} (Min) to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{SO} to V_{PF} (Min) V_{CC} Rise Time	t_{RB}	1			µs	
V_{PF} (Min) to V_{PF} (Max) V_{CC} Rise Time	t_R	0			µs	
Power Up	t_{REC}	15	25	35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	7			years	4

3

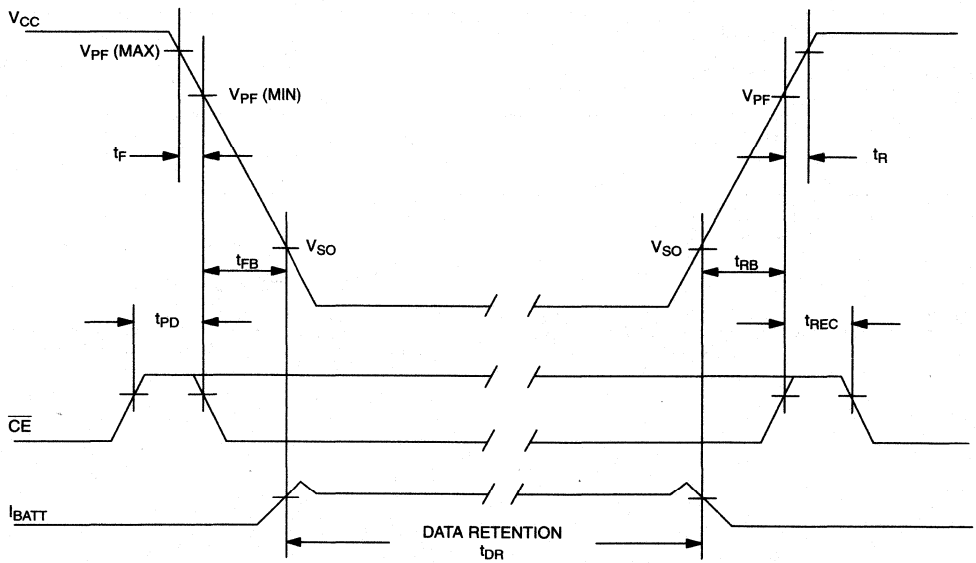
DS1647 READ CYCLE TIMING



DS1647 WRITE CYCLE TIMING



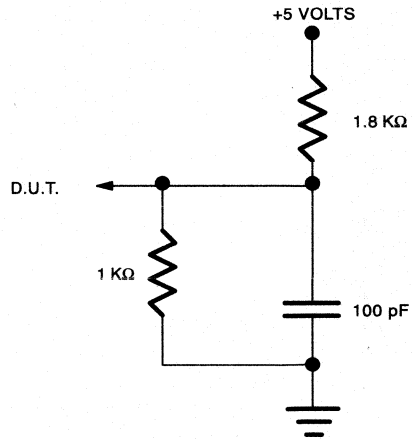
POWER DOWN/POWER UP TIMING



NOTES

1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Data retention time is at 25°C and is calculated from the date code on the device package plus one year. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225, would mean the 25th week of 1992.

OUTPUT LOAD



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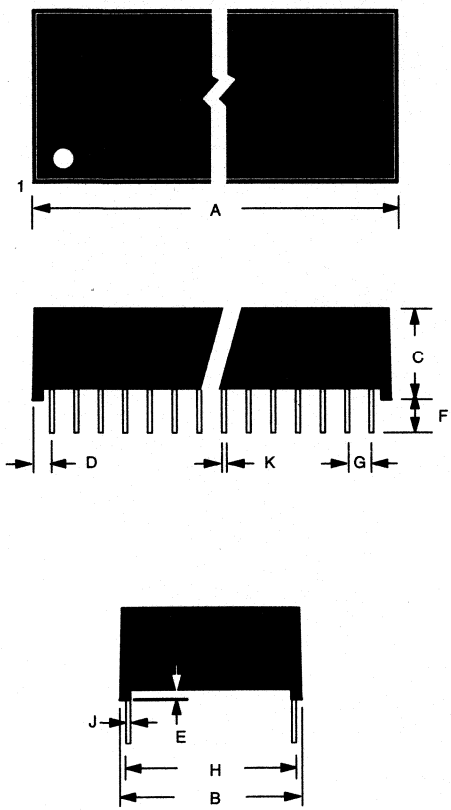
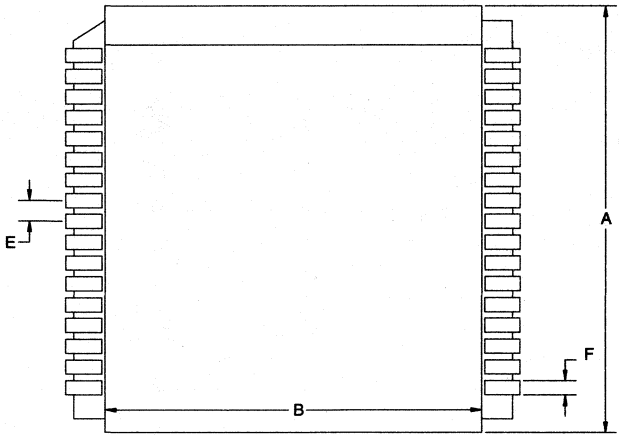
DS1647 32 PIN PACKAGE

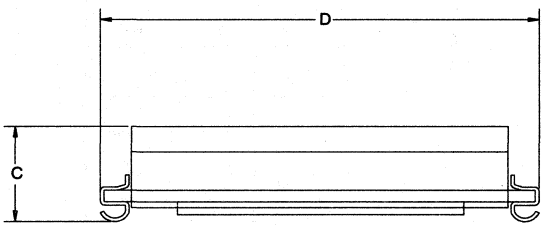


PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.670	1.690
MM	38.42	38.93
B IN.	0.715	0.740
MM	18.16	18.80
C IN.	0.335	0.355
MM	8.51	9.02
D IN.	0.075	0.105
MM	1.91	2.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.120	0.170
MM	3.05	4.32
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.025
MM	0.38	0.64

DS1647LPM 34–PIN LOW PROFILE MODULE



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.970
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.047	0.053
F	0.015	0.025



NOTE:
The recommended 68–pin PLCC surface mountable socket to be used with this 34–pin module is:

McKenzie P/N# 34P–SMT–3

The McKenzie socket plus the DS1647LPM has the following approximate dimensions: length, width = 1.22", height = 0.255".

DALLAS SEMICONDUCTOR

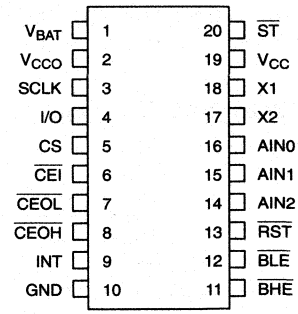
DS1670
Portable System Controller

3

FEATURES

- Provides real time clock:
  - Counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation
  - Power control circuitry supports system power on from day/time alarm
- Microprocessor monitor:
  - Halts microprocessor during power fail
  - Automatically restarts microprocessor after power failure
  - Monitors pushbutton for external override
  - Halts and resets an out of control microprocessor
- NVRAM control:
  - Automatic battery backup and write protection to external SRAM
- 3–channel, 8–bit analog–to–digital converter
- Simple three–wire interface
- 3.3 volt operation

PIN ASSIGNMENT



20–PIN TSSOP

DESCRIPTION

The Portable System Controller is a circuit which incorporates many of the functions necessary for low power portable products integrated into one chip. The DS1670 provides a Real Time Clock, NVRAM controller, microprocessor monitor, and a 3–channel 8–bit analog–to–digital converter. Communication with the DS1670 is established through a simple 3–wire interface.

The Real Time Clock (RTC) provides seconds, minutes, hours, day, date, month, and year information with leap year compensation. The RTC also provides an alarm interrupt. This interrupt works when the DS1670 is powered by the system power supply or when in battery backup operation so the alarm can be used to wake up a system that is powered down.

Automatic backup and write protection of external SRAM is provided through the V_{CCO}, $\overline{CEOL}$, and $\overline{CEOH}$ pins. The backup energy source used to power the RTC is also used to retain RAM data in the absence of V_{CC} through the V_{CCO} pin. The chip enable outputs to RAM ($\overline{CEOL}$ and $\overline{CEOH}$) are controlled during power transients to prevent data corruption.

The microprocessor monitor circuitry of the DS1670 provides three basic functions. First, a precision temperature–compensated reference and comparator circuit monitors the status of V_{CC}. When an out–of–tolerance condition occurs, an internal power fail signal is generated which forces the reset to the active state. When V_{CC} returns to an in–tolerance condition, the

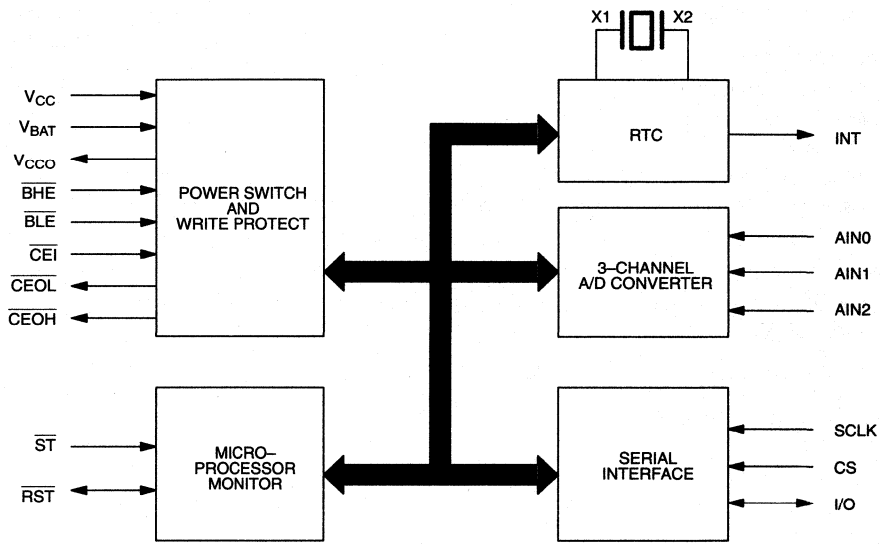
reset signals are kept in the active state for 250 ms to allow the power supply and processor to stabilize. The second microprocessor monitor function is pushbutton reset control. The DS1670 debounces a pushbutton input and guarantees an active reset pulse width of 250 ms. The third function is a watchdog timer. The DS1670 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to watchdog time–out.

The DS1670 also provides a 3–channel 8–bit successive approximation analog–to–digital converter. The converter has an internal 2.55 volt (typical) reference voltage generated by an on–board band–gap circuit. The A/D converter is monotonic (no missing codes) and has an internal analog filter to reduce high frequency noise.

OPERATION

The block diagram in Figure 1 shows the main elements of the DS1670. The following paragraphs describe the function of each pin.

DS1670 BLOCK DIAGRAM Figure 1



SIGNAL DESCRIPTIONS

V_{CC}, GND – DC power is provided to the device on these pins. V_{CC} is the +3.3 volt input. When 3.3 volts are applied within nominal limits, the device is fully accessible and data can be written and read. When V_{CC} drops below 2.88 volts (typical) access to the device is prohibited. When V_{CC} drops below the lower of V_{BAT} and 2.7 volts (typical), the device is switched over to the backup power supply.

V_{BAT} (Backup Power Supply) – Battery input for standard 3 volt lithium cell or other energy source.

SCLK (Serial Clock Input) – SCLK is used to synchronize data movement on the serial interface.

I/O (Data Input/Output) – The I/O pin is the bi–directional data pin for the 3–wire interface.

CS (Chip Select) – The Chip Select signal must be asserted high during a read or a write for communication over the 3–wire serial interface.

V_{CCO} (External SRAM Power Supply Output) – This pin is internally connected to V_{CC} when V_{CC} is within nominal limits. However, during power fail V_{CCO} is internally connected to the V_{BAT} pin. Switchover occurs when V_{CC} drops below the lower of V_{BAT} or 2.7 volts.

INT (Interrupt Output) – The INT pin is an active high output of the DS1670 that can be used as an interrupt input to a microprocessor. The INT output remains high as long as the status bit causing the interrupt is present and the corresponding interrupt–enable bit is set. The INT pin operates when the DS1670 is powered by V_{CC} or V_{BAT}.

$\overline{CEI}$ (RAM Chip Enable In) – $\overline{CEI}$ must be driven low to enable the external RAM.

$\overline{BLE}$ (Byte Low Enable input) – This pin when driven low activates the $\overline{CEOL}$ output if $\overline{CEI}$ is also driven low.

$\overline{BHE}$ (Byte High Enable input) – This pin when driven low activates the $\overline{CEOH}$ output if $\overline{CEI}$ is also driven low.

$\overline{CEOL}$ (RAM Chip Enable Out Low) – Chip enable output for low order SRAM byte.

$\overline{CEOH}$ (RAM Chip Enable Out High) – Chip enable output for high order SRAM byte.

$\overline{ST}$ (Strobe Input) – The Strobe input pin is used in conjunction with the watchdog timer. If the $\overline{ST}$ pin is not driven low within the watchdog time period, the $\overline{RST}$ pin is driven low.

$\overline{RST}$ (Reset) – The $\overline{RST}$ pin functions as a microprocessor reset signal. This pin is driven low 1) when V_{CC} is outside of nominal limits; 2) when the watchdog timer has "timed out"; 3) during the power up reset period; and 4) in response to a pushbutton reset. The $\overline{RST}$ pin also functions as a pushbutton reset input. When the $\overline{RST}$ pin is driven low, the signal is debounced and timed such that a $\overline{RST}$ signal of at least 250 ms is generated. This pin has an internal 47KΩ pull up resistor.

AIN0, AIN1, AIN2 (Analog Inputs) – These pins are the three analog inputs for the 3–channel analog–to–digital converter.

X1, X2 – Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT–26S or equivalent. For greatest accuracy, the DS1670 must be used with a crystal that has a specified load capacitance of 6pF. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks."

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POWER–UP/POWER–DOWN CONSIDERATIONS

The DS1670 was designed to operate with a power supply of 3.3 volts. When 3.3 volts are applied within nominal limits, the device becomes fully accessible after t_{RPU} (250ms typical). Before t_{RPU} elapses, all inputs are disabled. When V_{CC} drops below 2.88 volts (typical), the $\overline{RST}$ pin is driven low. When V_{CC} drops below the lower of 2.7 volts (typical) or the battery voltage, the device is switched over to the backup power supply.

During power up, when V_{CC} returns to an in–tolerance condition, the $\overline{RST}$ pin is kept in the active state for 250ms (typical) to allow the power supply and microprocessor to stabilize.

ADDRESS/COMMAND BYTE

The command byte for the DS1670 is shown in Figure 2. Each data transfer is initiated by a command byte. Bits zero through six specify the address of the registers to be accessed. The MSB (bit 7) is the Read/Write bit. This bit specifies whether the accessed byte will be read or written. A read operation is selected if bit 7 is a zero and a write operation is selected if bit 7 is a one. The address map for the DS1670 is shown in Figure 3.

ADDRESS/COMMAND BYTE Figure 2

7	6	5	4	3	2	1	0
$\overline{RD}$/$\overline{WR}$	A6	A5	A4	A3	A2	A1	A0

DS1670 ADDRESS MAP Figure 3

	BIT7							BIT0
00	0	10 SECONDS			SECONDS			
01	0	10 MINUTES			MINUTES			
02	0	12/24	10 HR A/P	10 HR	HOURS			
03	0	0	0	0	0	DAY		
04	0	0	10 DATE		DATE			
05	0	0	0	10 MO.	MONTH			
06	10 YEAR				YEAR			
07	M	10 SEC ALARM			SECONDS ALARM			
08	M	10 MIN ALARM			MINUTES ALARM			
09	M	12/24	10 HA A/P	10 HA	HOUR ALARM			
0A	M	0	0	0	DAY ALARM			
0B	CONTROL REGISTER							
0C	STATUS REGISTER							
0D	WATCHDOG REGISTER							
0E	ADC REGISTER							
0F	RESERVED							
7F								

CLOCK, CALENDAR AND ALARM

The time and calendar information is accessed by reading/writing the appropriate register bytes. Note that some bits are set to zero. These bits will always read zero regardless of how they are written. Also note that registers 0Fh to 7Fh are reserved. These registers will always read 0 regardless of how they are written. The contents of the time, calendar, and alarm registers are in the Binary–Coded Decimal (BCD) format.

The DS1670 can run in either 12–hour or 24–hour mode. Bit 6 of the hours register is defined as the 12– or 24–hour mode select bit. When high, the 12–hour mode is selected. In the 12–hour mode, bit 5 is the AM/PM bit with logic one being PM. In the 24–hour mode, bit 5 is the second 10–hour bit (20–23 hours).

The DS1670 also contains a time of day alarm. The alarm registers are located in registers 07h to 0Ah. Bit 7 of each of the alarm registers are mask bits (see Table 1). When all of the mask bits are logic 0, an alarm will occur once per week when the values stored in timekeeping registers 00h to 03h match the values stored in the time of day alarm registers. An alarm will be generated every day when mask bit of the day alarm register is set to 1. An alarm will be generated every hour when the day and hour alarm mask bits are set to 1. Similarly, an alarm will be generated every minute when the day, hour, and minute alarm mask bits are set to 1. When day, hour, minute, and seconds alarm mask bits are set to 1, an alarm will occur every second.

3

TIME OF DAY ALARM BITS Table 1

ALARM REGISTER MASK BITS (BIT 7)				
SECONDS	**MINUTES**	**HOURS**	**DAYS**	
1	1	1	1	Alarm once per second.
0	1	1	1	Alarm when seconds match.
0	0	1	1	Alarm when minutes and seconds match.
0	0	0	1	Alarm when hours, minutes and seconds match.
0	0	0	0	Alarm when day, hours, minutes and seconds match.

SPECIAL PURPOSE REGISTERS

The DS1670 has two additional registers (control register and status register) that control the real time clock and interrupts.

CONTROL REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{EOSC}$	WP	AIS1	AIS0	0	0	0	AIE

$\overline{EOSC}$ (Enable oscillator) – This bit, when set to logic 0 will start the oscillator. When this bit is set to a logic 1, the oscillator is stopped and the DS1670 is placed into a low–power standby mode with a current drain of less than 200 nanoamps when in battery back–up mode. When the DS1670 is powered by V_{CC}, the oscillator is always on regardless of the status of the $\overline{EOSC}$ bit; however, the real time clock is incremented only when $\overline{EOSC}$ is a logic 0.

WP (Write Protect) – Before any write operation to the real time clock or any other registers, this bit must be logic 0. When high, the write protect bit prevents a write operation to any register.

AIS0–AIS1 (Analog Input Select) – These two bits are used to determine the analog input for the analog–to–digital conversion. Table 2 lists the specific analog input that is selected by these two bits.

AIE (Alarm Interrupt Enable) – When set to a logic 1, this bit permits the Interrupt Request Flag (IRQF) bit in the status register to assert INT. When the AIE bit is set to logic 0, the IRQF bit does not initiate the INT signal.

ANALOG INPUT SELECTION Table 2

AIS1	AIS0	ANALOG INPUT
0	0	NONE
0	1	AIN0
1	0	AIN1
1	1	AIN2

STATUS REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CU	LOBAT	0	0	0	0	0	IRQF

CU (Conversion Update In Progress) – When this bit is a one, an update to the ADC Register (register 0Eh) will occur within 488 µs. When this bit is a zero, an update to the ADC Register will not occur for at least 244 µs.

LOBAT (Low Battery Flag) – This bit reflects the status of the backup power source connected to the V_{BAT} pin. When V_{BAT} is greater than 2.5 volts, LOBAT is set to a logic 0. When V_{BAT} is less than 2.3 volts, LOBAT is set to a logic 1.

IRQF (Interrupt Request Flag) – A logic 1 in the Interrupt Request Flag bit indicates that the current time has matched the time of day Alarm registers. If the AIE bit is also a logic 1, the INT pin will go high. IRQF is cleared by reading or writing to any of the alarm registers.

NONVOLATILE SRAM CONTROLLER

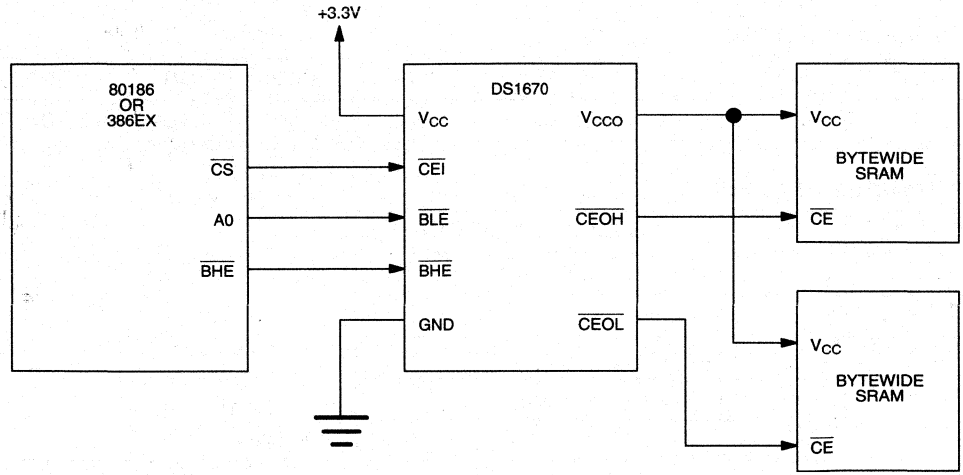
The DS1670 provides automatic backup and write protection for external SRAM. This function is provided by gating the chip enable signals and by providing a constant power supply through the V_{CCO} pin. The DS1670 was specifically designed with the Intel 80186 and 386EX microprocessors in mind. As such, the DS1670 has the capability to provide access to the external SRAM in either byte–wide or word–wide format. This capability is provided by the chip enable scheme. Three input signals and two output signals are used for enabling the external SRAM(s) (see Figure 4). $\overline{CEI}$ (chip enable in), $\overline{BHE}$ (byte high enable), and $\overline{BLE}$ (byte low enable) are used for enabling either one or two external SRAMs through the $\overline{CEOL}$ (chip enable low) and the $\overline{CEOH}$ (chip enable high) outputs. Table 3 illustrates the function of these pins.

The DS1670 nonvolatizes the external SRAM(s) by write protecting the SRAM(s) and by providing a back–up power supply in the absence of V_{CC}. When V_{CC} falls below 2.88 volts (typical), access to the external SRAM(s) are prohibited by forcing $\overline{CEOL}$ and $\overline{CEOH}$ high regardless of the level of $\overline{CEI}$, $\overline{BLE}$, and $\overline{BHE}$. Also at this point, the SRAM power supply (V_{CCO}) is switched from V_{CC} to V_{BAT}. Upon power up, access is prohibited until the end of t_{RPU}.

EXTERNAL SRAM CHIP ENABLE Table 3

$\overline{CEI}$	$\overline{BHE}$	$\overline{BLE}$	$\overline{CEOL}$	$\overline{CEOH}$	FUNCTION
0	0	0	0	0	Word Transfer
0	0	1	1	0	Byte Transfer in upper half of data bus (D15–D8)
0	1	0	0	1	Byte Transfer in lower half of data bus (D7–D0)
0	1	1	1	1	External SRAMs disabled
1	X	X	1	1	External SRAMs disabled

EXTERNAL SRAM INTERFACE (WORD WIDE) TO THE DS1670 Figure 4



MICROPROCESSOR MONITOR

The DS1670 monitors three vital conditions for a microprocessor: power supply, software execution, and external override.

First, a precision temperature–compensated reference and comparator circuit monitors the status of V_{CC}. When an out–of–tolerance condition occurs, an internal power fail signal is generated which forces the $\overline{RST}$ pin to the active state thus warning a processor–based system of impending power failure. The power fail trip point is 2.88 volts (typical). When V_{CC} returns to an in–tolerance condition upon power up, the reset signal is kept in the active state for 250ms (typical) to allow the power supply and microprocessor to stabilize. Note however that if the $\overline{EOSC}$ bit is set to a logic 1 (to disable the oscillator during battery back–up mode), the reset signal will be kept in an active state for 250 ms plus the start–up time of the oscillator.

The second monitoring function is pushbutton reset control. The DS1670 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1670 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge is detected, the DS1670 will debounce the switch by pulling the $\overline{RST}$ line low. After the internal 250 ms timer has expired, the DS1670 will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1670 will continue to monitor the line looking for a rising edge. Upon detecting release, the DS1670 will force the $\overline{RST}$ line low and hold it low for 250 ms.

The third microprocessor monitoring function provided by the DS1670 is a watchdog timer. The watchdog timer function forces $\overline{RST}$ to the active state when the $\overline{ST}$ input is not stimulated within the predetermined time period. The time period is set by the Time Delay (TD) bits in the Watchdog Register. The time delay can be set to 250ms, 500ms, or 1000ms (see Figure 5). If TD0 and TD1 are both set to zero, the watchdog timer is disabled. When enabled, the watchdog timer starts timing out from the set time period as soon as $\overline{RST}$ is inactive. The default setting is for the watchdog timer to be enabled with 1000ms time delay. If a high–to–low transition occurs on the $\overline{ST}$ input pin prior to time–out, the watchdog timer is reset and begins to time–out again. If the watchdog timer is allowed to time–out, then the $\overline{RST}$ signal is driven to the active state for 250ms (typical). The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. To guarantee that the watchdog timer does not time–out, a high–to–low transition must occur at or less than the minimum period.

WATCHDOG TIME–OUT CONTROL Figure 5

WATCHDOG REGISTER

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	0	0	0	0	0	TD1	TD0

WATCHDOG TIME–OUT

TD1	TD0	WATCHDOG TIME–OUT
0	0	Watchdog disabled
0	1	250 ms
1	0	500 ms
1	1	1000 ms

ANALOG–TO–DIGITAL CONVERTER

The DS1670 provides a 3–channel 8–bit analog–to–digital converter. The A/D reference voltage (2.55V typical) is derived from an on–chip band–gap circuit. Three multiplexed analog inputs are provided through the AIN0, AIN1, and AIN2 pins. The A/D converter is monotonic (no missing codes) and uses a successive approximation technique to convert the analog signal into a digital code.

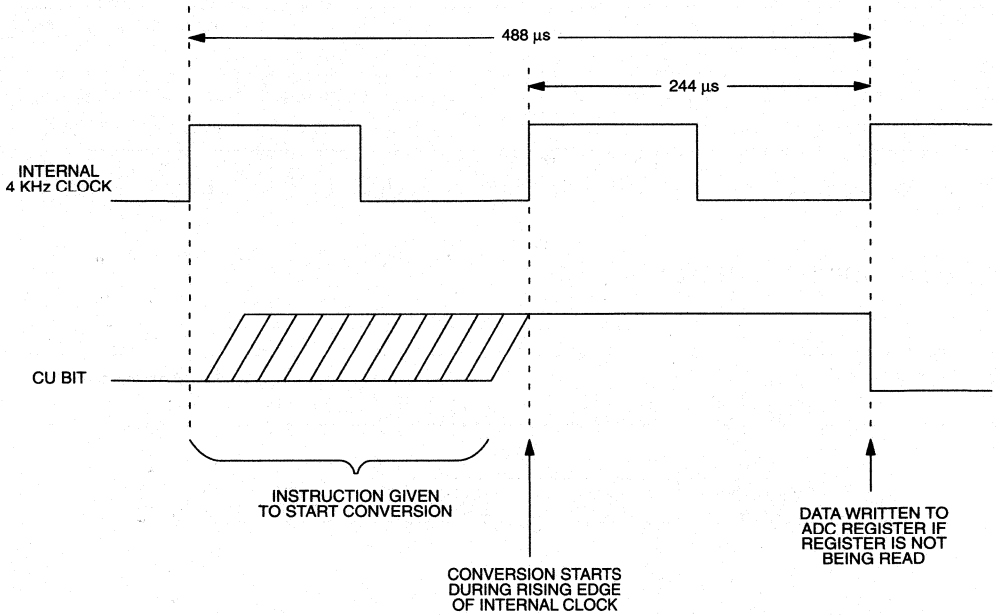
An A/D conversion is the process of assigning a digital code to an analog input voltage. This code represents the input value as a fraction of the full scale voltage (FSV) range. Thus the FSV range is then divided by the A/D converter into 256 codes (8 bits). The FSV range is bounded by an upper limit equal to the reference voltage and the lower limit which is ground. The DS1670 has a FSV of 2.55V (typical) which provides a resolution of 10 mV. An input voltage equal to the reference voltage converts to FFh while an input voltage equal to ground converts to 00h. The relative linearity of the A/D converter is ±0.5 LSB.

The A/D converter selects from one of three different analog inputs (AIN0 – AIN2). The input that is selected is determined by the Analog Input Select (AIS) bits in the Control Register. Table 2 lists the specific analog input that is selected by these two bits. Note also that the converter can be turned off by these bits to reduce power. When the A/D is turned on by setting AIS0 and AIS1 to any value other than 0,0 the analog input voltage is converted and written to the ADC Register within 488 µs. An internal analog filter at the input reduces high frequency noise. Subsequent updates occur approximately every 10ms. If AIS0 and/or AIS1 are changed, updates will occur at the next 10ms conversion time.

The Conversion Update In Progress (CU) bit in the Status Register indicates when the ADC Register can be read. When this bit is a one, an update to the ADC Register will occur within 488 µs maximum. However, when this bit is zero an update will not occur for at least 244 µs. The CU bit should be polled before reading the ADC Register to insure that the contents are stable during a read cycle. Once a read cycle to the ADC Register has been started, the DS1670 will not update that register until the read cycle has been completed. It should also be mentioned that taking CS low will abort the read cycle and will allow the ADC Register to be updated.

Figure 6 illustrates the timing of the CU bit relative to an instruction to begin conversion and the completion of that conversion.

CU BIT TIMING Figure 6



3

3–WIRE SERIAL INTERFACE

Communication with the DS1670 is accomplished through a simple 3–wire interface consisting of the Chip Select (CS), Serial Clock (SCLK) and Input/Output (I/O) pins.

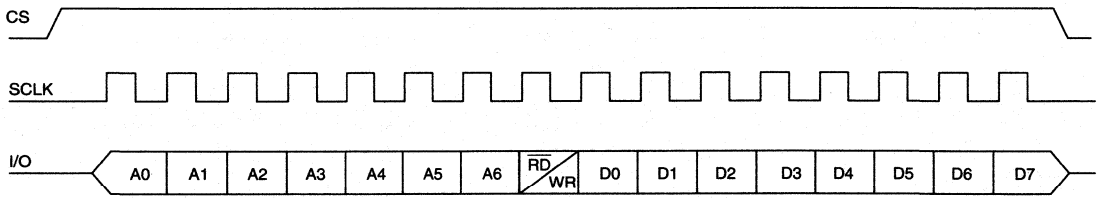
All data transfers are initiated by driving the CS input high. The CS input serves two functions. First, CS turns on the control logic which allows access to the shift register for the address/command sequence. Second, the CS signal provides a method of terminating either single byte or multiple byte (burst) data transfer. A clock cycle is a sequence of a rising edge followed by a falling edge. For data input, data must be valid during the rising edge of the clock and data bits are output on the falling edge of the clock. If the CS input goes low, all data transfer terminates and the I/O pin goes to a high impedance state.

Address and data bytes are always shifted LSB first into the I/O pin. Any transaction requires the address/command byte to specify a read or write to a specific register followed by one or more bytes of data. The address byte is always the first byte entered after CS is driven high. The most significant bit ($\overline{RD}$/WR) of this byte determines if a read or write will take place. If this bit is 0, one or more read cycles will occur. If this bit is 1, one or more write cycles will occur.

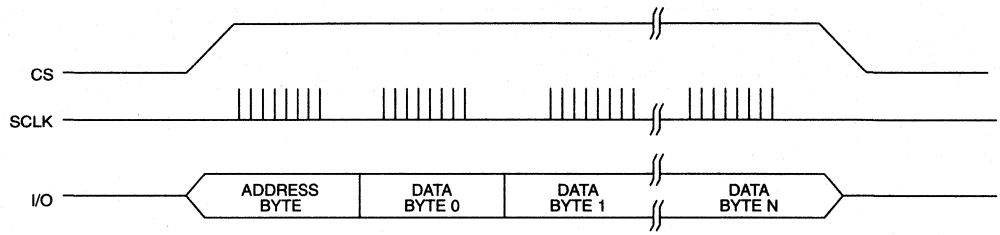
Data transfers can occur one byte at a time or in multiple byte burst mode. After CS is driven high an address is written to the DS1670. After the address, one or more data bytes can be read or written. For a single byte transfer one byte is read or written and then CS is driven low. For a multiple byte transfer, multiple bytes can be read or written to the DS1670 after the address has been written. Each read or write cycle causes the register address to automatically increment. Incrementing continues until the device is disabled. After accessing register 0Eh, the address wraps to 00h.

Data transfer for single byte transfer and multiple byte burst transfer is illustrated in Figures 7 and 8.

SINGLE BYTE DATA TRANSFER Figure 7



MULTIPLE BYTE BURST TRANSFER Figure 8



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +6V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.97	3.3	3.63	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	–0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	–1		+1	µA	
CS Leakage	I_{LO}			150	µA	7
Logic 1 Output	V_{OH}	2.4			V	2
Logic 0 Output	V_{OL}			0.4	V	3
Active Supply Current ($CS=V_{CC}-0.2$)	I_{CCA}		5	10	mA	4
A/D Converter Current	I_{ADC}			200	µA	5
Standby Current ($CS=V_{IL}$)	I_{CCS}			100	µA	6
Oscillator Current	I_{OSC}		300	500	nA	
Battery Standby Current (Oscillator Off)	I_{BAT}			200	nA	
Internal RST Pull–Up Resistor	R_P	35	47	60	KΩ	
V_{CC} Trip Point	V_{CCTP}	2.80	2.88	2.97	V	
V_{CC} Switchover	V_{CCSW}	2.62	2.70	2.78	V	12
A/D Reference Voltage	V_{ADC}	2.47	2.55	2.63	V	
Pushbutton Detect	PB_{DV}	0.8		2.0	V	
Pushbutton Release	PB_{RD}		0.3	0.8	V	
Output Voltage	V_{CCO}	V_{CC}–0.3			V	11
V_{CCO} Output Current (Source=V_{CC})	I_{CCO1}			100	mA	13
V_{CCO} Output Current (Source=V_{BAT})	I_{CCO2}			150	µA	14

CAPACITANCE

(t_A=25°C)

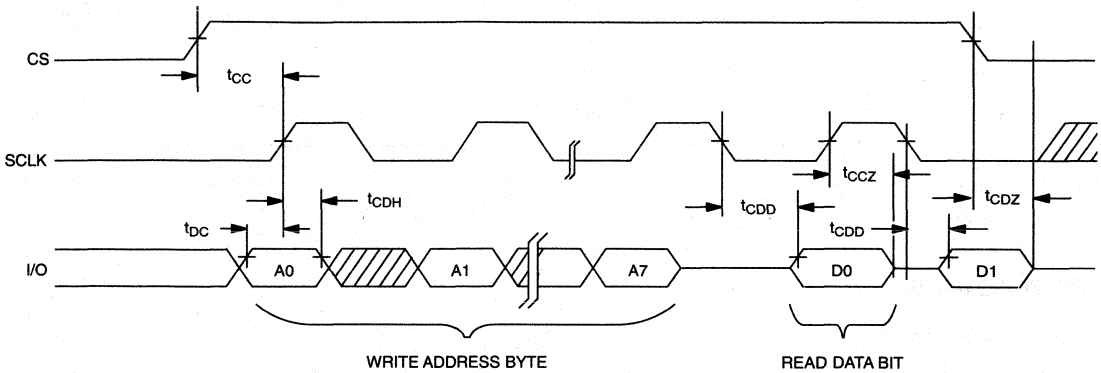
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		10		pF	
I/O Capacitance	$C_{I/O}$		15		pF	
Crystal Capacitance	C_X		6		pF	

AC ELECTRICAL CHARACTERISTICS

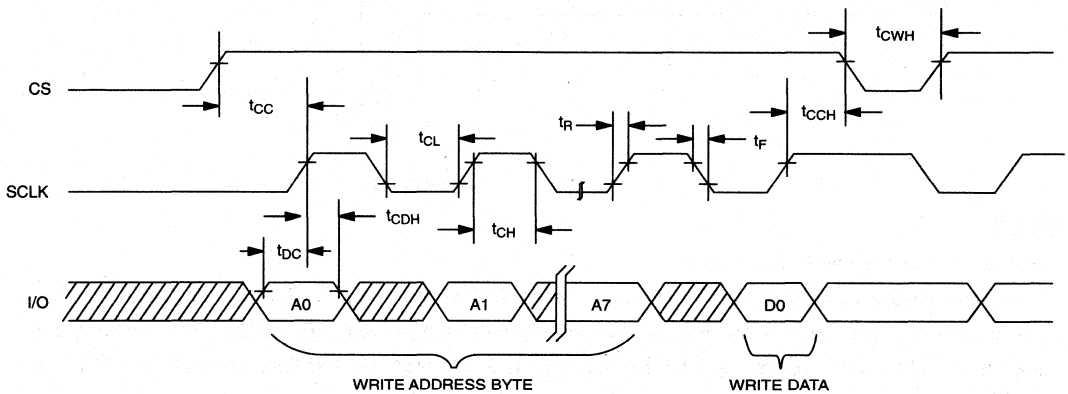
(0°C to 70°C; V_{CC}=3.3V ± 10%))

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to Clock Setup	t_{DC}	100			ns	8
CLK to Data Hold	t_{CDH}	140			ns	8
CLK to Data Delay	t_{CDD}			400	ns	8, 9, 10
CLK to Low Time	t_{CL}	500			ns	8
CLK to High Time	t_{CH}	500			ns	8
CLK Frequency	t_{CLK}			1.0	MHz	8
CLK Rise and Fall	t_R, t_F			1000	ns	
CS to CLK Setup	t_{CC}	2			µs	8
CLK to CS Hold	t_{CCH}	120			ns	8
CS Inactive Time	t_{CWH}	2			µs	8
CS to I/O High Z	t_{CDZ}			140	ns	8
SCLK to I/O High Z	t_{CCZ}			140	ns	8
V_{CC} Slew Rate (2.85V to 2.3V)	t_F	300			µs	
V_{CC} Slew Rate (2.3V to 2.85V)	t_R	0			ns	
V_{CC} Detect to $\overline{RST}$ (V_{CC} Falling)	t_{RPD}			100	ns	
Reset Active Time	t_{RST}		250		ms	15
Pushbutton Debounce	PB_{DB}		250		ms	15
V_{CC} Detect to $\overline{RST}$ (V_{CC} Rising)	t_{RPU}		250		ms	15, 16
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	
Chip Enable Propagation Delay to External SRAM	t_{CED}		8	15	ns	
Nominal Voltage to V_{CC} Switchover Fall Time	t_{FB}	200			µs	

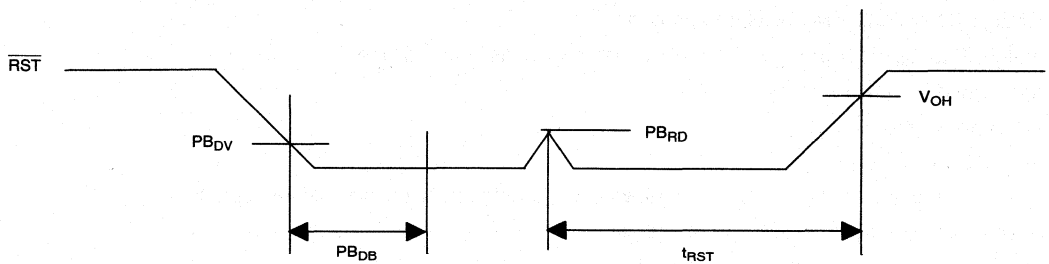
TIMING DIAGRAM: READ DATA Figure 9



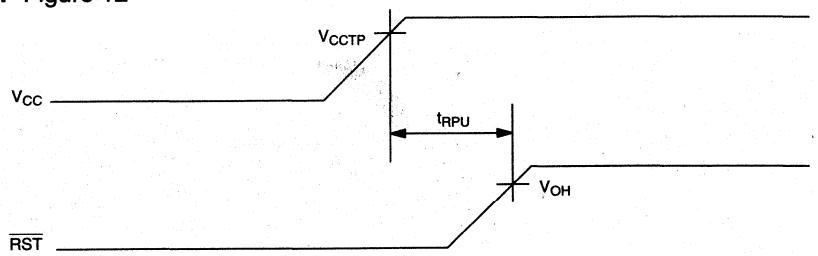
TIMING DIAGRAM: WRITE DATA Figure 10



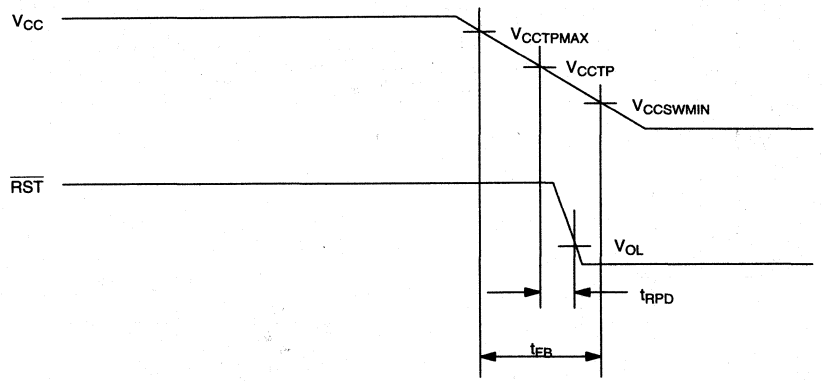
PUSHBUTTON RESET Figure 241



POWER UP Figure 12



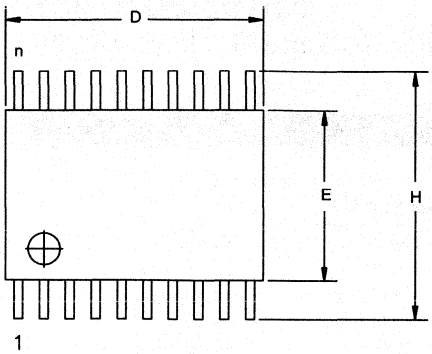
POWER DOWN Figure 13

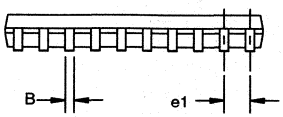


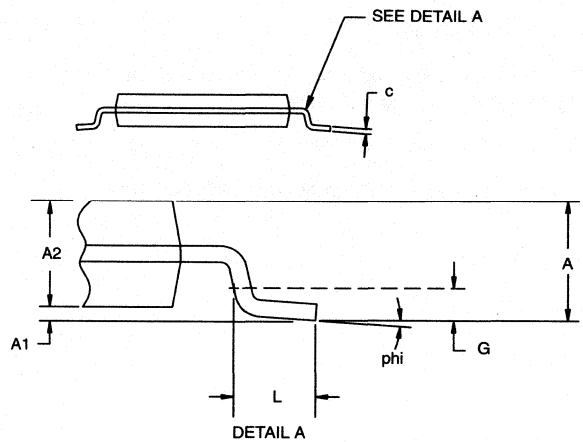
NOTES:

1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 0.4 mA at V_{CC}=3.3V, V_{OH}=V_{CC} for capacitive loads.
3. Logic zero voltages are specified at a sink current of 1.5 mA at V_{CC}=3.3V, V_{OL}=GND for capacitive loads.
4. I_{CCA} is specified with outputs open, CS set to a logic 1, SCLK=500 KHz, oscillator enabled, and D/A converter enabled.
5. I_{ADC} is specified with CS, V_{CCO} open and I/O, SCLK at logic zero. A/D converter is enabled.
6. I_{CCS} is specified with CS, V_{CCO} open and I/O, SCLK at logic zero. A/D converter is disabled.
7. CS has a 40 KΩ pulldown resistor to ground.
8. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10 ns maximum rise and fall time.
9. Measured at V_{OH}=2.4V or V_{OL}=0.4V.
10. Load capacitance = 50 pF.
11. I_{CCO}=100 mA, V_{CC} > V_{CCTP}.
12. V_{CCO} switchover from V_{CC} to V_{BAT} occurs when V_{CC} drops below the lower of V_{CCSW} and V_{BAT}.
13. Current from V_{CC} input pin to V_{CCO} output pin.
14. Current from V_{BAT} input pin to V_{CCO} output pin.
15. Timebase is generated by very accurate crystal oscillator. Accuracy of this time period is based on the crystal that is used. A typical crystal with a specified load capacitance of 6 pF will provide an accuracy within ±100 ppm over the 0°C to 70°C temperature range.
16. If the $\overline{EOSC}$ bit in the Control Register is set to a logic 1, t_{RPU} is equal to 250 ms plus the start–up time of the crystal oscillator.

20-PIN TSSOP (PRELIMINARY)







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

PRELIMINARY

DALLAS SEMICONDUCTOR

DS1685/DS1687
3 Volt/5 Volt Real Time Clock

FEATURES

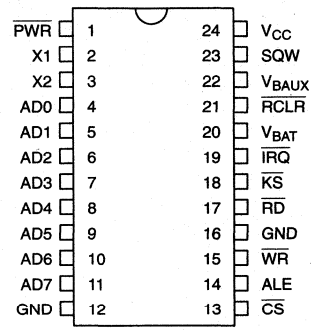
Incorporates industry standard DS1287 PC clock plus enhanced features:

- +3 or +5 volt operation
- 64–bit silicon serial number
- Power control circuitry supports system power on from date/time alarm or key closure
- 32 KHz output for power management
- Crystal select bit allows RTC to operate with 6 pF or 12.5 pF crystal
- SMI Recovery Stack
- 242 bytes user NVRAM
- Auxiliary battery input
- RAM clear input
- Century register
- Date alarm register
- Compatible with existing BIOS for original DS1287 functions
- Available as chip (DS1685) or standalone module with embedded battery and crystal (DS1687)

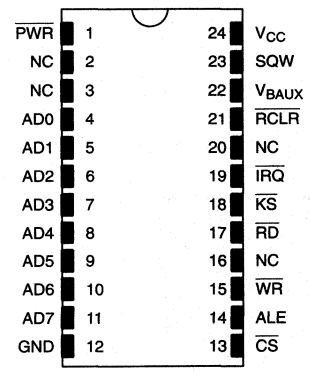
ORDERING INFORMATION

PART #	DESCRIPTION
DS1685–X	RTC Chip; 24–pin DIP
DS1685E–X	RTC Chip; 24–pin TSSOP
DS1685S–X	RTC Chip; 24–pin SOIC
DS1685Q–X	RTC Chip; 28–pin PLCC
DS1687–X	RTC Module; 24–pin DIP
	–3 +3 volt device
	–5 +5 volt device

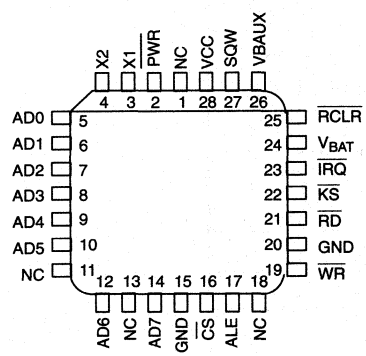
PIN ASSIGNMENT



DS1685 24–PIN DIP
DS1685S 24–PIN SOIC
DS1685E 24–PIN TSSOP



DS1687 24–PIN ENCAPSULATED PACKAGE



DS1685Q 28–PIN PLCC

PIN DESCRIPTION

X1	–	Crystal Input
X2	–	Crystal Output
$\overline{RCLR}$	–	RAM Clear Input
AD0-AD7	–	Mux'ed Address/Data Bus
$\overline{PWR}$	–	Power–on Interrupt Output (open drain)
$\overline{KS}$	–	Kickstart Input
$\overline{CS}$	–	RTC Chip Select Input
ALE	–	RTC Address Strobe
$\overline{WR}$	–	RTC Write Data Strobe
$\overline{RD}$	–	RTC Read Data Strobe
$\overline{IRQ}$	–	Interrupt Request Output (open drain)
SQW	–	Square Wave Output
V_{CC}	–	+3 or +5 Volt Main Supply
GND	–	Ground
V_{BAT}	–	Battery + Supply
V_{BAUX}	–	Auxiliary Battery Supply
NC	–	No Connection

DESCRIPTION

The DS1685/DS1687 is a real time clock (RTC) designed as a successor to the industry standard DS1285, DS1385, DS1485, and DS1585 PC real time clocks. This device provides the industry standard DS1285 clock function with either +3.0 or +5.0 volt operation. The DS1685 also incorporates a number of enhanced features including a silicon serial number, power on/off control circuitry, 242 bytes of user NVSRAM and 32.768 KHz output for sustaining power management activities.

The DS1685/DS1687 power control circuitry allows the system to be powered on via an external stimulus, such as a keyboard or by a time and date (wake up) alarm. The $\overline{PWR}$ output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS1685 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time–of–day and memory status in the absence of power. The DS1687 incorporates the DS1685 chip, a 32.768 KHz crystal, and a lithium battery in a complete, self–contained timekeeping module. The entire unit is fully tested at Dallas Semiconductor such that a minimum of 10 years of timekeeping and data retention in the absence of V_{CC} is guaranteed.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1685/DS1687. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +3 volt or +5 volt input.

SQW (Square Wave Output) - The SQW pin will provide a 32 KHz square wave output, t_{REC}, after a power–up condition has been detected. This condition sets the following bits, enabling the 32 KHz output; DV1=1, and E32K=1. A square wave will be output on this pin if either SQWE=1 or E32K=1. If E32K=1, then 32 KHz will be output regardless of the other control bits. If E32K=0, then the output frequency is dependent on the control bits in register A. The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in register B or the E32K bit in extended register 4Bh. A 32 KHz SQW signal is output when the Enable 32 KHz (E32K) bit in extended register 4Bh is a logic one, and V_{CC} is above V_{PF}. A 32 KHz square wave is also available when V_{CC} is less than V_{PF} if E32K=1, ABE=1, and voltage is applied to the V_{BAUX} pin.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1685 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, at which time the DS1685/DS1687 latches the address. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ pulse. In a read cycle the DS1685/DS1687 outputs 8 bits of data during the latter portion of the $\overline{RD}$ pulse. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high. The address/data bus also serves as a bidirectional data path for the external extended RAM.

ALE (RTC Address Strobe Input; active high) - A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1685/DS1687.

$\overline{RD}$ (RTC Read Input; active low) - $\overline{RD}$ identifies the time period when the DS1685/DS1687 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

$\overline{WR}$ (RTC Write Input; active low) -The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed register.

$\overline{CS}$ (RTC Chip Select Input; active low) - The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1685/DS1687 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place with ALE asserted but without asserting $\overline{CS}$ will latch addresses. However, no data transfer will occur.

$\overline{IRQ}$ (Interrupt Request Output; open drain, active low) - The $\overline{IRQ}$ pin is an active low output of the DS1685/DS1687 that can be tied to the interrupt input of a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application software must clear all enabled flag bits contributing to $\overline{IRQ}$'s active state.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ pin is an open drain output and requires an external pull-up resistor.

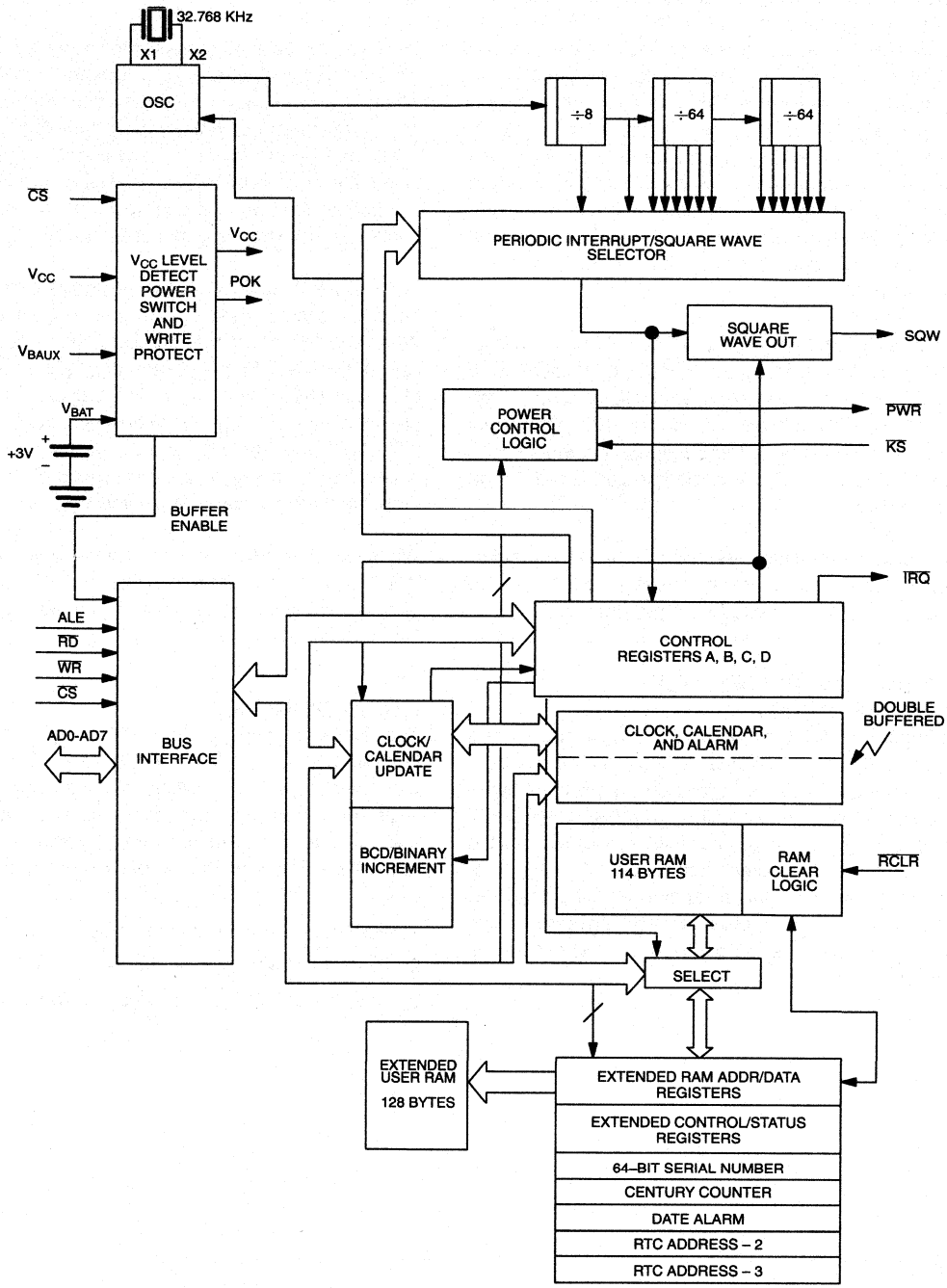
$\overline{PWR}$ (Power On Output; open drain, active low) - The $\overline{PWR}$ pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the DS1685/DS1687, $\overline{PWR}$ may be automatically activated from a Kickstart input via the $\overline{KS}$ pin or from a Wake Up interrupt. Once the system is powered on, the state of $\overline{PWR}$ can be controlled via bits in the Dallas registers.

$\overline{KS}$ (Kickstart Input; active low) - When V_{CC} is removed from the DS1685/DS1687, the system can be powered on in response to an active low transition on the $\overline{KS}$ pin, as might be generated from a key closure. V_{BAUX} must be present and Auxiliary Battery Enable bit (ABE) must be set to 1 if the kickstart function is used, and the $\overline{KS}$ pin must be pulled up to the V_{BAUX} supply. While V_{CC} is applied, the $\overline{KS}$ pin can be used as an interrupt input.

$\overline{RCLR}$ (RAM Clear Input; active low) - If enabled by software, taking $\overline{RCLR}$ low will result in the clearing of the 242 bytes of user RAM. When enabled, $\overline{RCLR}$ can be activated whether or not V_{CC} is present.

V_{BAUX} - Auxiliary battery input required for kickstart and wake up features. This input also supports clock/calendar and user RAM if V_{BAT} is at lower voltage or is not present. A standard +3 volt lithium cell or other energy source can be used. Battery voltage must be held between +2.5 and +3.7 volts for proper operation. If V_{BAUX} is not going to be used it should be grounded and auxiliary battery enable bit bank 1, register 4BH, should=0.

DS1685/DS1687 BLOCK DIAGRAM Figure 1



DS1685 ONLY

X1, X2 - Connections for a standard 32.768 KHz quartz crystal. For greatest accuracy, the DS1685 must be used with a crystal that has a specified load capacitance of either 6 pF or 12.5 pF. The Crystal Select (CS) bit in Extended Control Register 4B is used to select operation with a 6 pF or 12.5 pF crystal. The crystal is attached directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area.

For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks". The DS1685 can also be driven by an external 32.768 KHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

V_{BAT} - Battery input for any standard 3 Volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation.

POWER–DOWN/POWER–UP CONSIDERATIONS

The real-time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS1685/DS1687 and reaches a level of greater than V_{PF} (power fail trip point), the device becomes accessible after t_{REC}, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied.

The DS1685/DS1687 is available in either a 3 volt or a 5 volt device.

The 5 volt device is fully accessible and data can be written and read only when V_{CC} is greater than 4.5 volts. When V_{CC} is below 4.5 volts, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below the greater of V_{BAT} and V_{BAUX}, the RAM and timekeeper are switched over to a lithium battery connected either to the V_{BAT} pin or V_{BAUX} pin.

The 3 volt device is fully accessible and data can be written or read only when V_{CC} is greater than 2.7 volts. When V_{CC} falls below V_{PF}, access to the device is inhibited. If V_{PF} is less than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply (the greater of V_{BAT} and V_{BAUX}) when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply when V_{CC} drops below the larger of V_{BAT} and V_{BAUX}.

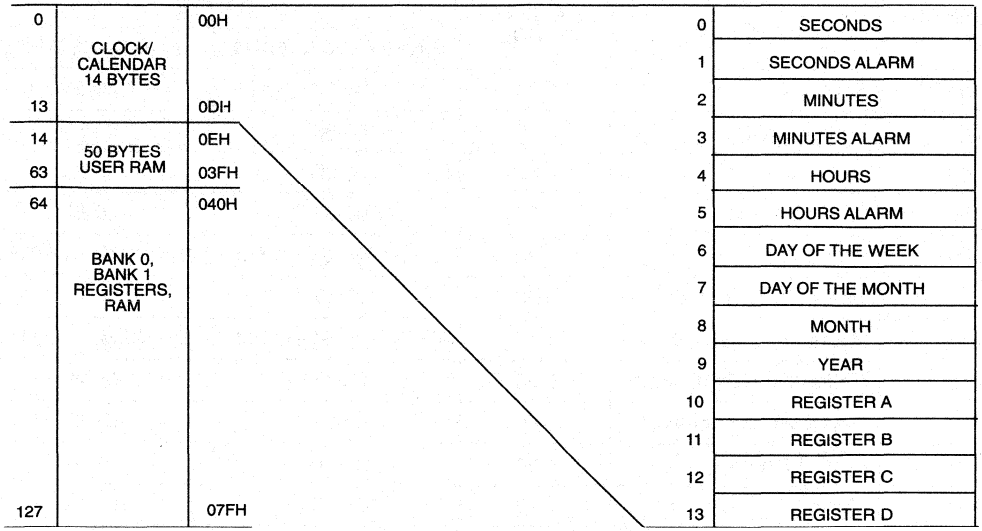
When V_{CC} falls below V_{PF}, the chip is write-protected. With the possible exception of the $\overline{KS}$, $\overline{PWR}$, and SQW pins, all inputs are ignored and all outputs are in a high impedance state.

RTC ADDRESS MAP

The address map for the RTC registers of the DS1685/DS1687 is shown in Figure 2. The address map consists of the 14 clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and four bytes are used for control and status. All registers can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

DS1685 REAL TIME CLOCK ADDRESS MAP Figure 2



3

TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching will be explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The four alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second use condition is to insert a "don't care" state in one or more of the four alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second. The three alarm bytes may be used in conjunction with the date alarm as described in the Wakeup/Kickstart section. The century counter will be discussed later in this text.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
00H	Seconds	0-59	00-3B	00-59
01H	Seconds Alarm	0-59	00-3B	00-59
02H	Minutes	0-59	00-3B	00-59
03H	Minutes Alarm	0-59	00-3B	00-59
04H	Hours 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours 24-Hour Mode	0-23	00-17	00-23
05H	Hours Alarm 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92 PM
	Hours Alarm 24-hr. Mode	0-23	00-17	00-23
06H	Day of Week Sunday=1	1-7	01-07	01-07
07H	Date of Month	1-31	01-1F	01-31
08H	Month	1-12	01-0C	01-12
09H	Year	0-99	00-63	00-99
BANK 1, 48H	Century	0-99	00-63	00-99
BANK 1, 49H	Date Alarm	1-31	01-1F	01-31

CONTROL REGISTERS

The four control registers; A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

NONVOLATILE RAM - RTC

The 242 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1685/DS1687. They can be used by the application program as nonvolatile memory and are fully available during the update cycle.

The user RAM is divided into two separate memory banks. When the bank 0 is selected, the 14 real time clock registers and 114 bytes of user RAM are accessible. When bank 1 is selected, an additional 128 bytes of user RAM are accessible through the extended RAM address and data registers.

INTERRUPT CONTROL

The DS1685/DS1687 includes six separate, fully automatic sources of interrupt for a processor:

1. Alarm interrupt
2. Periodic interrupt
3. Update-ended interrupt
4. Wake up interrupt
5. Kickstart interrupt
6. RAM clear interrupt

The conditions which generate each of these independent interrupt conditions are described in greater detail elsewhere in this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are a total of six bits including three bits in Register B and three bits in Extended Register B which enable the interrupts. The extended register locations are described later. Writing a logic 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ will immediately be set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As

a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits which are set remain stable throughout the read cycle. All bits which were set are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the $\overline{IRQ}$ line will be driven low when an interrupt flag bit is set and its corresponding enable bit is also set. $\overline{IRQ}$ will be held low as long as at least one of the six possible interrupt sources has it s flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS1685/DS1687 initiated an interrupt is accomplished by reading Register C and finding IRQF=1. IRQF will remain set until all enabled interrupt flag bits are cleared to 0.

SQUARE WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768 KHz crystal tied to X1 and X2. The square wave output is enabled and disabled via the SQWE bit in Register B or the E32K bit in extended register 4Bh. If the square wave is enabled (SQWE=1 or E32K=1), then the output frequency will be determined by the settings of the E32K bit in Extended Register 4Bh and by the RS3-0 bits in Register A. If E32K=1, then a 32.768 KHz square wave will be output on the SQW pin regardless of the settings of RS3-0 and SQWE.

If E32K = 0, then the square wave output frequency is determined by the RS3-0 bits. These bits control a 1-of-15 decoder which selects one of thirteen taps that divide the 32.768 KHz frequency. The RS3-0 bits establish the SQW output frequency as shown in Table 2. In addition, RS3-0 bits control the periodic interrupt selection as described below.

If E32K=1, and the Auxiliary Battery Enable bit (ABE, bank 1; register 04BH) is enabled, and voltage is applied to V_{BAUX} then the 32 KHz square wave output signal will be output on the SQW pin in the absence of V_{CC}. This facility is provided to clock external power management circuitry. If any of the above requirements are not met, no square wave output signal will be generated on the SQW pin in the absence of V_{CC}.

A pattern of 01X in the DV2, DV1, and DV0, bits respectively, will turn the oscillator on and enable the countdown chain. Note that this is different than the DS1287, which required a pattern of 010 in these bits. DV0 is now a "don't care" because it is used for selection between register banks 0 and 1.

A pattern of 11X will turn the oscillator on, but the oscillator's countdown chain will be held in reset, as it was in the DS1287. Any other bit combination for DV2 and DV1 will keep the oscillator off.

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3-0 bits in Register A which select the square wave frequency (see Table 2). Changing the bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE and E32K bits control the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The Serialized RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, alarm and elapsed time byte is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows the time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all alarm locations.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

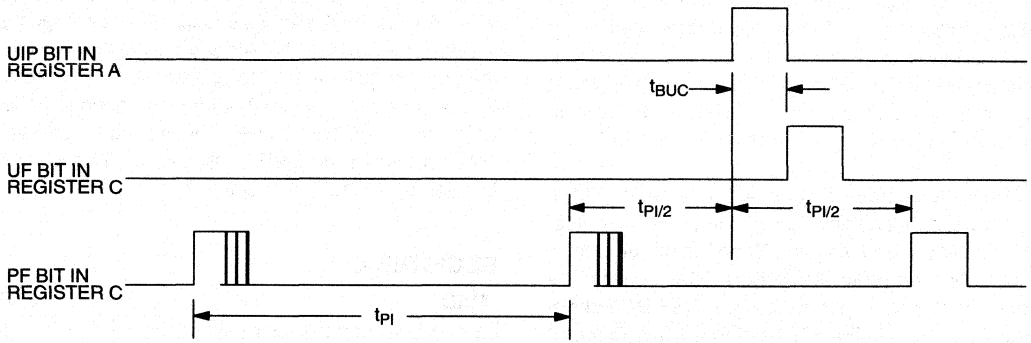
PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

EXT. REG. B	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
E32K	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625 ms	256 Hz
0	0	0	1	0	7.8125 ms	128 Hz
0	0	0	1	1	122.070 µs	8.192 KHz
0	0	1	0	0	244.141 µs	4.096 KHz
0	0	1	0	1	488.281 µs	2.048 KHz
0	0	1	1	0	976.5625 µs	1.024 KHz
0	0	1	1	1	1.953125 ms	512 Hz
0	1	0	0	0	3.90625 ms	256 Hz
0	1	0	0	1	7.8125 ms	128 Hz
0	1	0	1	0	15.625 ms	64 Hz
0	1	0	1	1	31.25 ms	32 Hz
0	1	1	0	0	62.5 ms	16 Hz
0	1	1	0	1	125 ms	8 Hz
0	1	1	1	0	250 ms	4 Hz
0	1	1	1	1	500 ms	2 Hz
1	X	X	X	X	*	32.768 KHz

*RS3-RS0 determine periodic interrupt rates as listed for E32K=0.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within (t_{PI} / 2+t_{BUC}) to ensure that data is not read during the update cycle.

UPDATE–ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1
t_{BUC} = DELAY TIME BEFORE UPDATE CYCLE = 244 µs

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These bits are defined as follows:

DV2 = Countdown Chain
- 1 - resets countdown chain only if DV1=1
- 0 - countdown chain enabled

DV1 = Oscillator Enable
- 0 - oscillator off
- 1 - oscillator on

DV0 = Bank Select
- 0 - original bank
- 1 - extended registers

A pattern of 01X is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 01X is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

Enable the interrupt with the PIE bit;

Enable the SQW output pin with the SQWE or E32K bits;

Enable both at the same time and the same rate; or

Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1685/DS1687.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1685/DS1687 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1685/DS1687 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one and E32K=0, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to zero and E32K=0, the SQW pin is held low. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 WF = WIE = 1
AF = AIE = 1 KF = KSE = 1
UF = UIE = 1 RF = RIE = 1

i.e., $IRQF = (PF \bullet PIE) + (AF \bullet AIE) + (UF \bullet UIE) + (WF \bullet WIE) + (KF \bullet KSE) + (RF \bullet RIE)$

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 3 THROUGH BIT 0 - These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit indicates the condition of the battery connected to the V_{BAT} pin or the battery connected to V_{BAUX}, whichever is at a higher voltage. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

EXTENDED FUNCTIONS

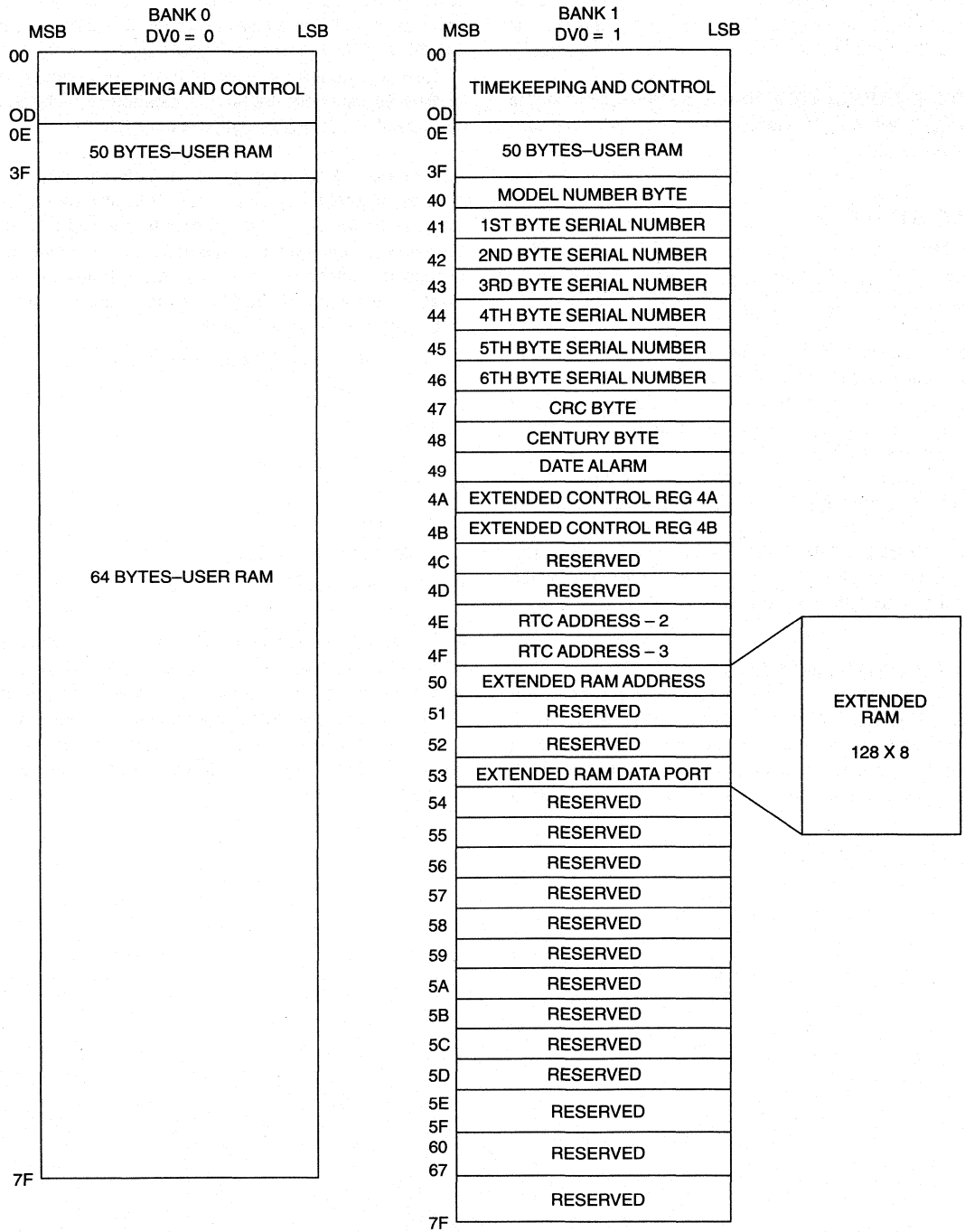
The extended functions provided by the DS1685/DS1687 that are new to the RAMified RTC family are accessed via a software controlled bank switching scheme, as illustrated in Figure 4. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS1685/DS1687 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers which provide control and status for the extended functions will be accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

1. 64–bit Silicon Serial Number
2. Century counter
3. Date Alarm
4. Auxiliary Battery Control/Status
5. Wake Up
6. Kickstart
7. RAM Clear Control/Status
8. 128 bytes Extended RAM Access

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and will return a 0 if read.

DS1685/DS1687 EXTENDED REGISTER BANK DEFINITION Figure 4



SILICON SERIAL NUMBER

A unique 64–bit lasered serial number is located in bank 1, registers 40h – 47h. This serial number is divided into three parts. The first byte in register 40h contains a model number to identify the device type and revision of the DS1685/DS1687. Registers 41h – 46h contain a unique binary number. Register 47h contains a CRC byte used to validate the data in registers 40h – 46h. All eight bytes of the serial number are read–only registers.

The DS1685/DS1687 is manufactured such that no two devices will contain an identical number in locations 41h – 47h. Blocks of numbers for these locations can be reserved by the customer. Contact Dallas Semiconductor for special ordering information for DS1685/DS1687's with reserved blocks of serial numbers.

CENTURY COUNTER

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

128 X 8 EXTENDED RAM

The DS1685/DS1687 provides 128 x 8 of on–chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power–up, the RAM is taken out of write protect status by the internal power OK signal (POK) generated from the write protect circuitry.

The on–chip 128 x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7 to AD0. Access to the SRAM is controlled by two on–chip latch registers. One register is used to hold the SRAM address, and the other register is used to hold read/write data. The SRAM address space is from 00h to 7Fh.

Access to the extended 128 x 8 RAM is controlled via two of the Dallas registers shown in Figure 4. The Dallas registers in bank 1 must first be selected by setting the DV0 bit in register A to a logic 1. The 7–bit address of the RAM location to be accessed must be loaded into the extended RAM address register located at 50h. Data in the addressed location may be read by performing a read operation from location 53h, or written to by performing a write operation to location 53h. Data in any addressed location may be read or written repeatedly without changing the address in location 50h.

AUXILIARY BATTERY

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS1685/DS1687 kickstart, wake up, and SQW output features in the absence of V_{CC}. This power source must be available in order to use these auxiliary features when no V_{CC} is applied to the device.

The Auxiliary Battery Enable (ABE; bank 1, register 04BH) bit in extended control register B is used to turn on and off the auxiliary battery for the above functions in the absence of V_{CC}. When set to a 1, V_{BAUX} battery power is enabled, and when cleared to 0, V_{BAUX} battery power is disabled to these functions.

In the DS1685/DS1687, this auxiliary battery may be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended external RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS1685 is to be backed-up using a single battery with the auxiliary features enabled, then V_{BAUX} should be used and connected to V_{BAT}. If V_{BAUX} is not to be used, it should be grounded and ABE should be cleared to 0.

WAKE UP/KICKSTART

The DS1685/DS1687 incorporates a wake up feature which can power the system on at a pre-determined date through activation of the $\overline{PWR}$ output pin. In addition, the kickstart feature can allow the system to be powered up in response to a low going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin. As a result, system power may be applied upon such events as a key closure, or modem ring detect signal. In order to use either the wake up or the kickstart features, the DS1685/DS1687 must have an auxiliary battery connected to the V_{BAUX} pin and the oscillator must be running and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the $\overline{PWR}$ pin will not be driven low in response to a kickstart or wakeup condition, while in battery-backed mode.

The wake up feature is controlled through the Wake up Interrupt Enable bit in extended control register B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake up feature, clearing WIE to 0 disables it. Similarly, the kickstart feature is controlled through the Kickstart Interrupt Enable bit in extended control register B (KSE, bank 1, 04BH).

A wake up sequence will occur as follows: When wake up is enabled via WIE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar will monitor the current date for a match condition with the date alarm register (bank 1, register 049H). In conjunction with the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake up will occur at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm will occur regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the $\overline{PWR}$ pin will automatically be driven low. This output can be used to turn on the main system power supply which provides V_{CC} voltage to the DS1685/DS1687 as well as the other major components in the system. Also at this time, the Wake Up flag (WF, bank 1, register 04AH) will be set, indicating that a wake up condition has occurred.

A kickstart sequence will occur when kickstarting is enabled via KSE = 1. While the system is powered down, the $\overline{KS}$ input pin will be monitored for a low going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line will be pulled low, as it is for a wake up condition. Also at this time, the Kickstart Flag (KF, bank 1, register 04AH) will be set, indicating that a kickstart condition has occurred.

The timing associated with both the wake up and kickstarting sequences is illustrated in the Wake Up / Kickstart Timing Diagram in the Electrical Specifications section of this data sheet. The timing associated with these functions is divided into 5 intervals, labeled 1-5 on the diagram.

The occurrence of either a kickstart or wake up condition will cause the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS1685/DS1687 V_{CC} pin rises above the 3 volt power fail level before the power on timeout period (t_{POTO}) expires, then $\overline{PWR}$ will remain at the active low level. If V_{CC} does not rise above the 3 volt power fail voltage in this time, then the $\overline{PWR}$ output pin will be turned off and will return to its high impedance level. In this event, the $\overline{IRQ}$ pin will also remain tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power on sequence will remain set until cleared by software during a subsequent system power on.

If V_{CC} is applied within the timeout period, then the system power on sequence will continue as shown in intervals 2-5 in the timing diagram. During interval 2, $\overline{PWR}$ will remain active and $\overline{IRQ}$ will be driven to its active low level, indicating that either WF or KF was set in initiating the power on. In the diagram $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit will be automatically cleared to 0 in response to a successful power on. The $\overline{PWR}$ line will remain active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing zeroes to both of these control bits. As long as no other interrupt within the DS1685/DS1687 is pending, the $\overline{IRQ}$ line will be taken inactive once these bits are reset. Execution of the application software may proceed. During this time, both the wake up and kickstart functions may be used to generate status and interrupts. WF will be set in response to a date, hours, minutes, and seconds match condition. KF will be set in response to a low going transition on $\overline{KS}$. If the associated interrupt enable bit is set (WIE and/or KSE) then the $\overline{IRQ}$ line will driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS1685/DS1687 may cause $\overline{IRQ}$ to be driven low. While system power is applied, the on chip logic will always attempt to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake up or kickstart.

The system may be powered down under software control by setting the PAB bit to a logic 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ}$ output pin will be placed in a high impedance state when V_{CC} goes below V_{PF}. If the system is to be again powered on in response to a wake up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and nonvolatile RAM is in effect and $\overline{IRQ}$ is tri-stated, and monitoring of wake up and kickstart takes place. If PRS=1, $\overline{PWR}$ stays active, otherwise if PRS=0 $\overline{PWR}$ is tri–stated.

RAM CLEAR

The DS1685/DS1687 provides a RAM clear function for the 242 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V_{CC} pin.

The RAM clear function is enabled or disabled via the RAM Clear Enable bit (RCE; bank 1, register 04BH). When this bit is set to a logic 1, the 242 bytes of user RAM will be cleared (all bits set to 1) when an active low transition is sensed on the $\overline{RCLR}$ pin. This action will have no effect on either the clock/calendar settings or upon the contents of the extended RAM. The RAM clear Flag (RF, bank 1, register 04AH) will be set when the RAM clear operation has been completed. If V_{CC} is present at the time of the RAM clear and RIE=1, the $\overline{IRQ}$ line will also be driven low upon completion. The interrupt condition can be cleared by writing a zero to the RF bit. The $\overline{IRQ}$ line will then return to its inactive high level provided there are no other pending interrupts. Once the $\overline{RCLR}$ pin is activated, all read/write accesses are locked out for a minimum recover time, specified as t_{REC} in the Electrical Characteristics section.

When RCE is cleared to zero, the RAM clear function is disabled. The state of the $\overline{RCLR}$ pin will have no effect on the contents of the user RAM, and transitions on the $\overline{RCLR}$ pin have no effect on RF.

EXTENDED CONTROL REGISTERS

Two extended control registers are provided to supply controls and status information for the extended features offered by the DS1685/DS1687. These are designated as extended control registers A and B and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows.

EXTENDED CONTROL REGISTER 4A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	*	*	PAB	RF	WF	KF

VRT2 - This status bit gives the condition of the auxiliary battery. It is set to a logic 1 condition when the external lithium battery is connected to the V_{BAUX}. If this bit is read as a logic 0, the external battery should be replaced.

INCR - Increment in Progress status bit. This bit is set to a 1 when an increment to the time/date registers is in progress and the alarm checks are being made. INCR will be set to a 1 at 122 µs before the update cycle starts and will be cleared to 0 at the end of each update cycle.

PAB - Power Active Bar control bit. When this bit is 0, the $\overline{PWR}$ pin is in the active low state. When this bit is 1, the $\overline{PWR}$ pin is in the high impedance state. This bit can be written to a logic 1 or 0 by the user. If either WF AND WIE = 1 OR KF AND KSE = 1, the PAB bit will be cleared to 0.

RF - Ram Clear Flag. This bit will be set to a logic 1 when a high to low transition occurs on the $\overline{RCLR}$ input if RCE=1. The RF bit is cleared by writing it to a logic 0. This bit can also be written to a logic 1 to force an interrupt condition.

WF - Wake up Alarm Flag - This bit is set to 1 when a wake up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

KF - Kickstart Flag - This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

EXTENDED CONTROL REGISTER 4B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32K	CS	RCE	PRS	RIE	WIE	KSE

ABE - Auxiliary Battery Enable. This bit when written to a logic 1 will enable the V_{BAUX} pin for extended functions.

E32K - Enable 32.768 KHz output. This bit when written to a logic 1 will enable the 32.768 KHz oscillator frequency to be output on the SQW pin.

CS – Crystal Select Bit. When CS is set to a 0, the oscillator is configured for operation with a crystal that has a 6 pF specified load capacitance. When CS=1, the oscillator is configured for a 12.5 pF crystal.

RCE - RAM Clear Enable bit. When set to a 1, this bit enables a low level on $\overline{RCLR}$ to clear all 242 bytes of user RAM. When RCE = 0, $\overline{RCLR}$ and the RAM clear function are disabled.

PRS – PAB Reset Select Bit. When set to a 0 the $\overline{PWR}$ pin will be set hi–Z when the DS1685 goes into power fail. When set to a 1, the $\overline{PWR}$ pin will remain active upon entering power fail.

RIE - Ram Clear Interrupt Enable. When RIE is set to a 1, the $\overline{IRQ}$ pin will be driven low when a RAM clear function is completed.

WIE - Wake Up Alarm Interrupt Enable. When V_{CC} voltage is absent and WIE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a wake up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If WIE is set while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to WF being set to 1. When WIE is cleared to a 0, the WF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

KSE - Kickstart Interrupt Enable. When V_{CC} voltage is absent and KSE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If KSE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to KF being set to 1. When KSE is cleared to a 0, the KF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

* Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no effect on operation.

SYSTEM MAINTENANCE INTERRUPT (SMI) RECOVERY STACK

An SMI recovery register stack is located in the extended register bank, locations 4Eh and 4Fh. This register stack, shown below, can be used by the BIOS to recover from an SMI occurring during an RTC read or write.

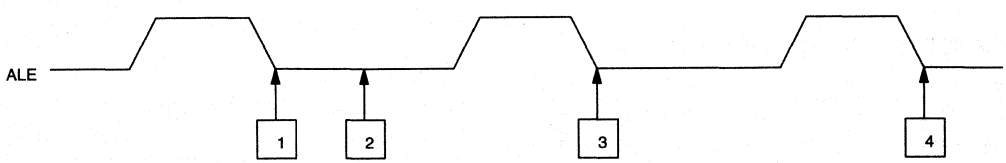
	RTC ADDRESS
	RTC ADDRESS – 1
4Eh	RTC ADDRESS – 2
4Fh	RTC ADDRESS – 3

SMI RECOVERY STACK

7	6	5	4	3	2	1	0
DV0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

REGISTER BIT DEFINITION

The RTC address is latched on the falling edge of the ALE signal. Each time an RTC address is latched, the register address stack is pushed. The stack is only four registers deep, holding the three previous RTC addresses in addition to the current RTC address being accessed. The following waveform illustrates how the BIOS could recover the RTC address when an SMI occurs.



1. The RTC address is latched.
2. An SMI is generated before an RTC read or write occurs.
3. RTC address 0Ah is latched and the address from "1" is pushed to the "RTC Address – 1" stack location. This step is necessary to change the bank select bit, DV0=1.
4. RTC address 4Eh is latched and the address from "" is pushed to location 4Eh, "RTC Address – 2" while 0Ah is pushed to the "RTC Address – 1" location. The data in this register, 4Eh, is the RTC address lost due to the SMI.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature DS1685	–55°C to +125°C
Storage Temperature DS1687	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage 5 Volt Operation	V_{CC}	4.5	5.0	5.5	V	1
Power Supply Voltage 3 Volt Operation	V_{CC}	2.7	3.0	3.3	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		0.6	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	1
Auxiliary Battery Voltage	V_{BAUX}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		7	15	mA	2, 3
CMOS Standby Current ($\overline{CS}$=V_{CC}-0.2V)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
Output Leakage Current	I_{OL}	–1		+1	µA	6
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Power Fail Trip Point	V_{PF}	4.25	4.37	4.5	V	4
Battery Switch Voltage	V_{SW}		V_{BAT}, V_{BAUX}		V	9

DC ELECTRICAL CHARACTERISTICS (cont'd)

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Leakage OSC ON	I_{BAT1}			1000	nA	
Battery Leakage OSC OFF	I_{BAT2}			100	nA	
I/O Leakage	I_{LO}	–1		+1	µA	5
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			10.0	mA	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=3.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		5	10	mA	2, 3
CMOS Standby Current ($\overline{CS}$=V_{CC}-0.2)	I_{CC2}		0.5	2	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
Output Leakage Current	I_{OL}	–1		+1	µA	6
Output Logic 1 Voltage @ 0.4 mA	V_{OH}	2.4			V	
Output Logic 0 Voltage @ 0.8 mA	V_{OL}			0.4	V	
Power Fail Trip Point	V_{PF}	2.5	2.6	2.7	V	4
Battery Leakage OSC ON	I_{BAT1}			1000	nA	
Battery Leakage OSC OFF	I_{BAT2}			100	nA	
I/O Leakage	I_{LO}	–1		+1	µA	5
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			4	mA	1

RTC AC TIMING CHARACTERISTICS

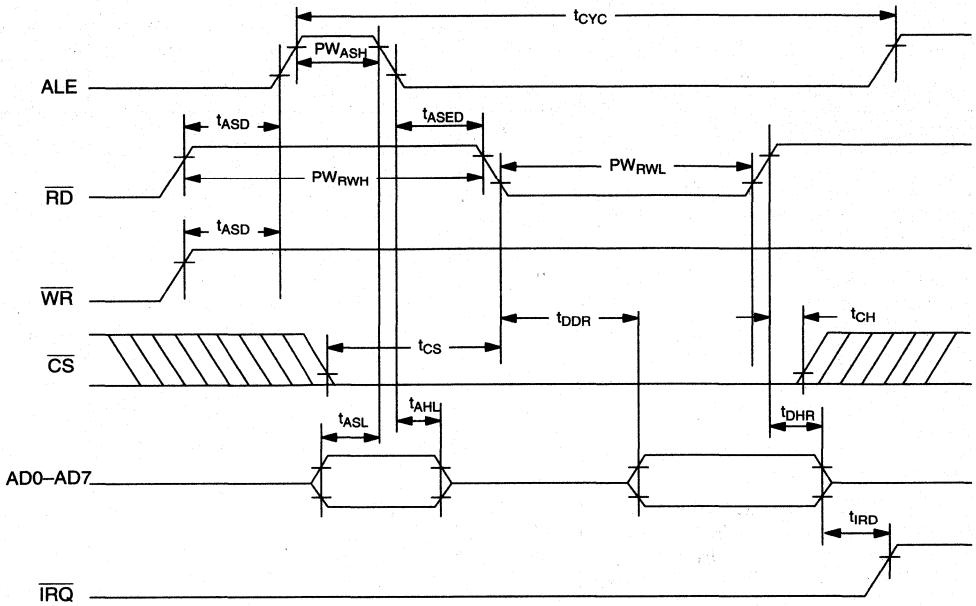
(0°C to 70°C; V_{CC} = 3.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	915		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{RWL}	375			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{RWH}	450			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	75			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		120	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	90			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	30			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	30			ns	
Pulse Width ALE High	PW_{ASH}	180			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	120			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		370	ns	7
Data Setup Time	t_{DSW}	180			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

AC TEST CONDITIONS

Output Load: 50 pF
Input Pulse Levels: 0–3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS1685/DS1687 BUS TIMING FOR READ CYCLE TO RTC

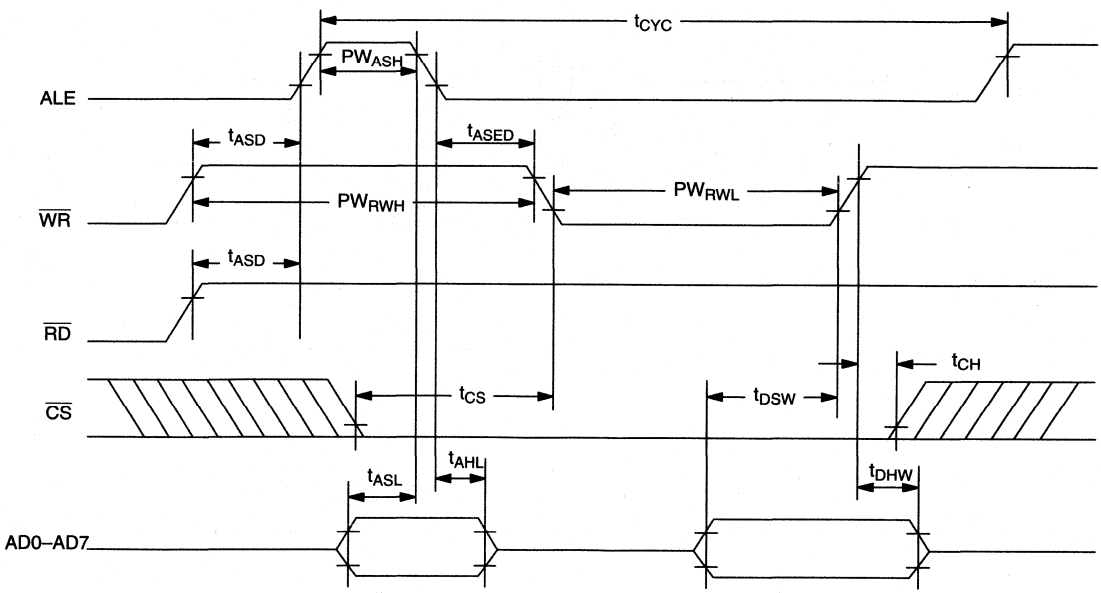


RTC AC TIMING CHARACTERISTICS

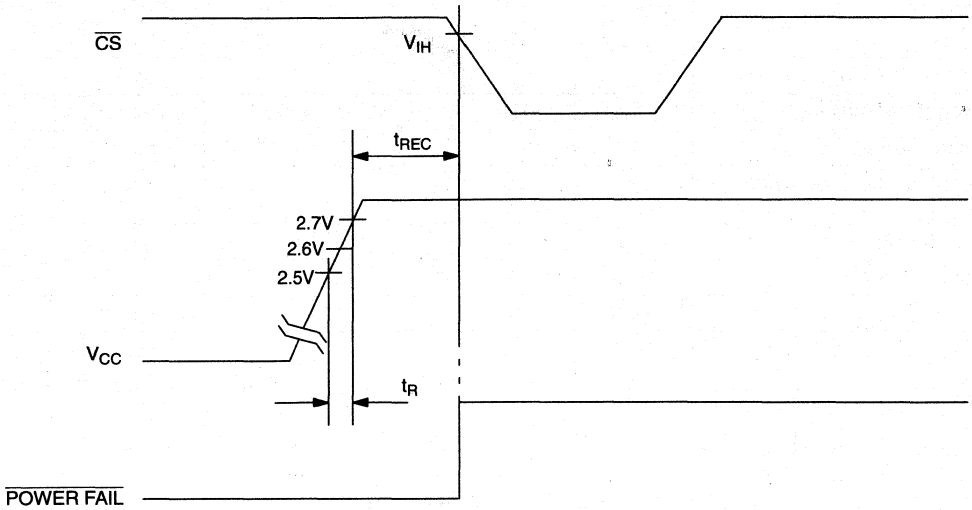
(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{RWL}	125			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{RWH}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	7
Data Setup Time	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

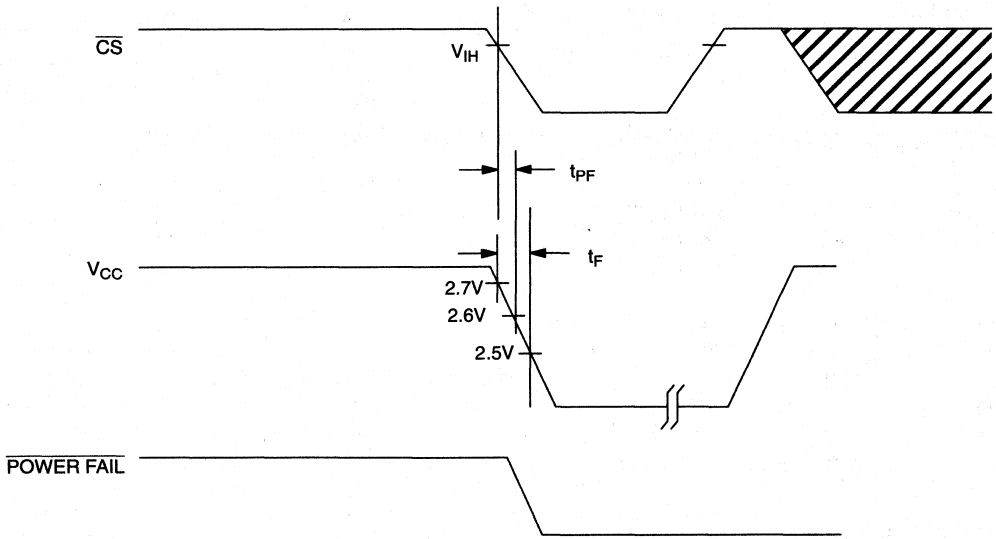
DS1685/DS1687 BUS TIMING FOR WRITE CYCLE TO RTC AND RTC REGISTERS



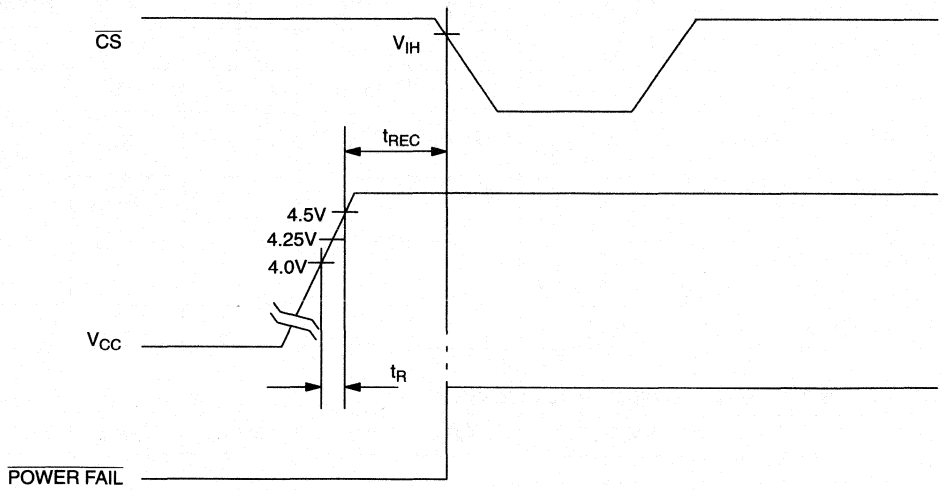
POWER–UP CONDITION 3 VOLT DEVICE



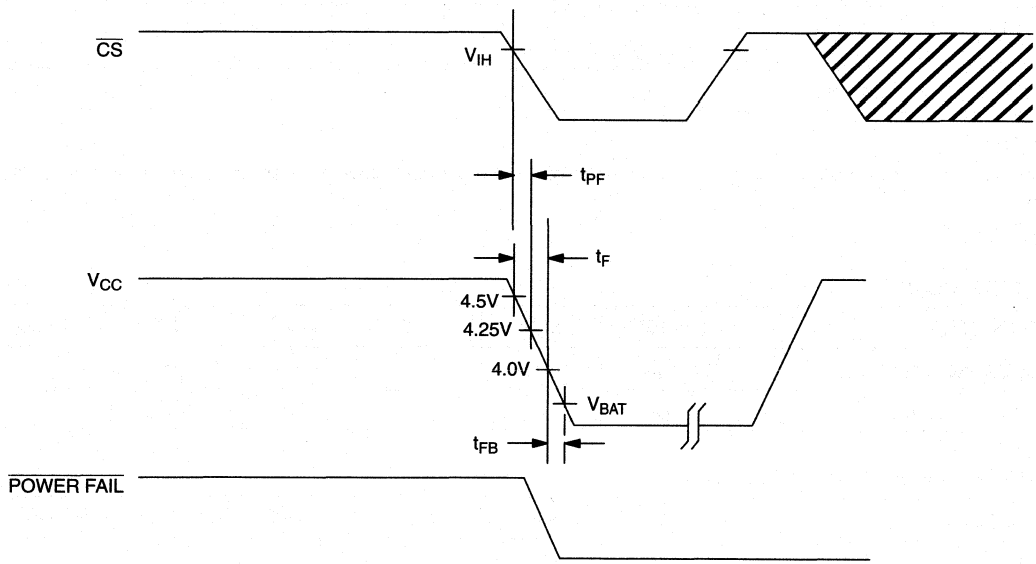
POWER–DOWN CONDITION 3 VOLT DEVICE



POWER–UP CONDITION 5.0 VOLT DEVICE



POWER–DOWN CONDITION 5.0 VOLT DEVICE



POWER-UP POWER-DOWN TIMING 5 VOLT DEVICE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	10, 11

POWER-UP POWER-DOWN TIMING 3 VOLT DEVICE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $2.6 \le V_{CC} \le 2.7V$	300			µs	
V_{CC} Slew Rate Power Up	t_R $2.7V \ge V_{CC} \ge 2.6V$	0			µs	
Expected Data Retention	t_{DR}	10			years	10, 11

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

(t_A = 25°C)

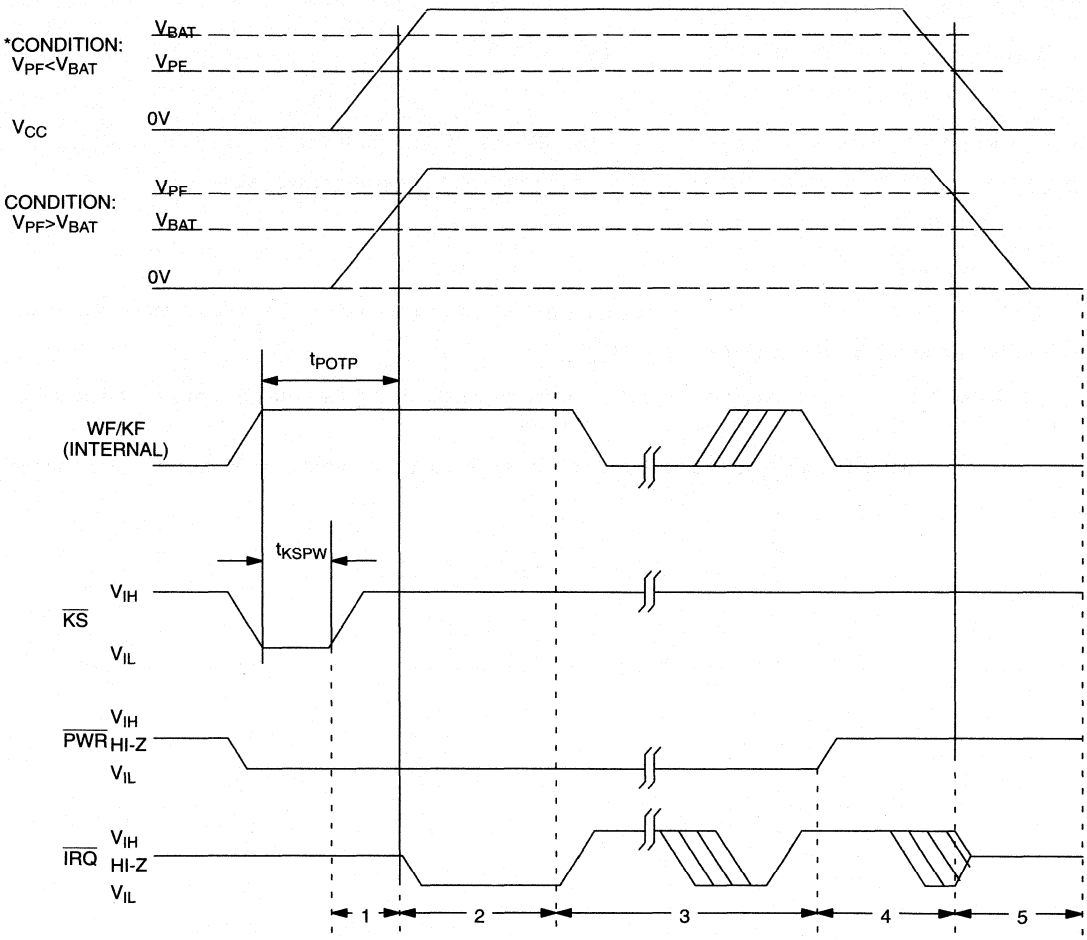
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

WAKE UP/KICKSTART TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t_{KSPW}	2			µs	
Wake up/Kickstart Power On Timeout	t_{POTO}	2			seconds	8

WAKE UP/KICKSTART TIMING



NOTE:

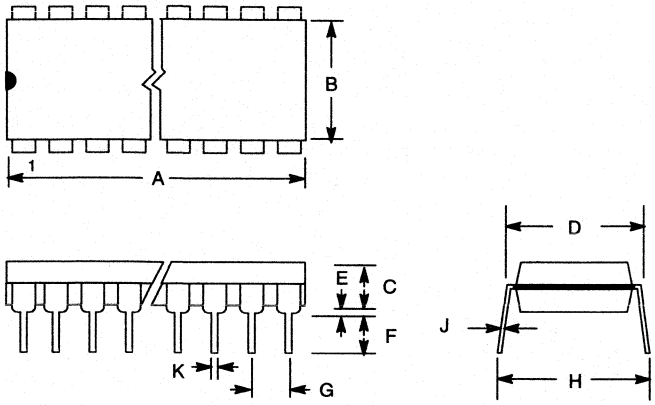
Time intervals shown above are referenced in Wake up/Kickstart section.

* This condition can occur with the 3 volt device.

NOTES:

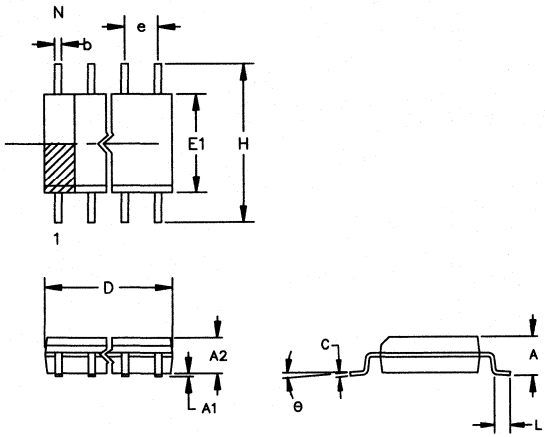
1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Write protection trip point occurs during power fail prior to switchover from V_{CC} to V_{BAT}.
5. Applies to the AD0–AD7 pins, and the SQW pin when each is in a high impedance state.
6. The $\overline{IRQ}$ and $\overline{PWR}$ pins are open drain outputs.
7. Measured with a load of 50 pF + 1 TTL gate.
8. Wakeup kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.
9. V_{SW} is determined by the larger of V_{BAT} and V_{BAUX}.
10. The DS1687 will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
11. t_{DR} is the amount of time that the internal battery can power the internal oscillator and internal registers of the DS1687.

DS1685 24–PIN DIP



PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	1.245 31.62	1.270 32.25
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.380	0.050 1.27
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.625 15.88	0.675 17.15
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

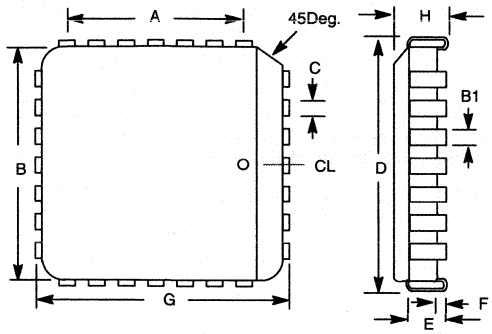
DS1685 24–PIN SOIC



The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

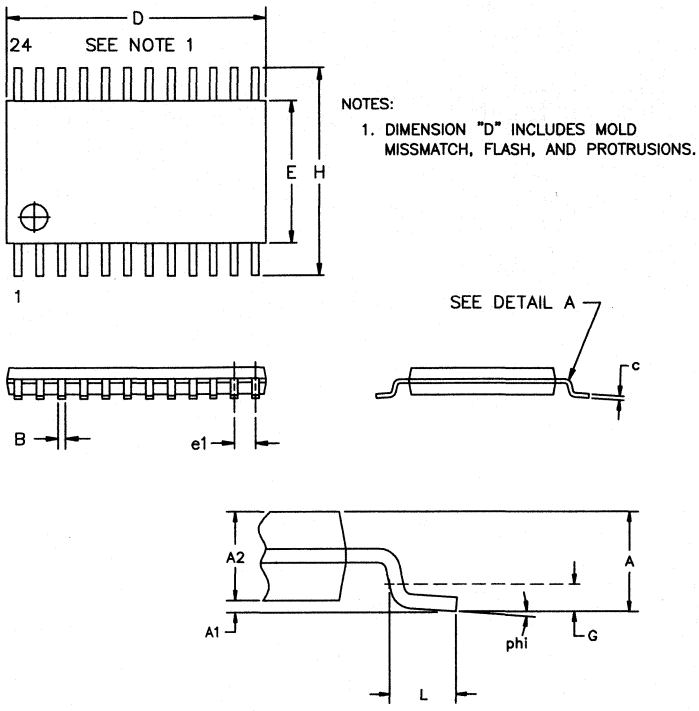
PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33
D IN. MM	0.598 15.19	0.612 15.54
e IN. MM	.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02
Θ	0°	8°

DS1685Q 28–PIN PLCC



PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	0.300 BSC 7.62	
B IN. MM	0.445 11.30	0.460 11.68
B1 IN MM	0.013 0.33	0.021 0.53
C IN MM	0.027 0.68	0.33 0.84
D IN. MM	0.480 12.19	0.500 12.70
D2 IN. MM	0.390 9.91	0.430 10.92
E IN. MM	0.090 2.29	0.120 3.05
E2 IN. MM	0.390 9.91	0.430 10.92
F IN. MM	0.020 0.51	
G IN MM	0.480 12.19	0.500 12.70
H IN MM	0.165 4.19	0.180 4.57

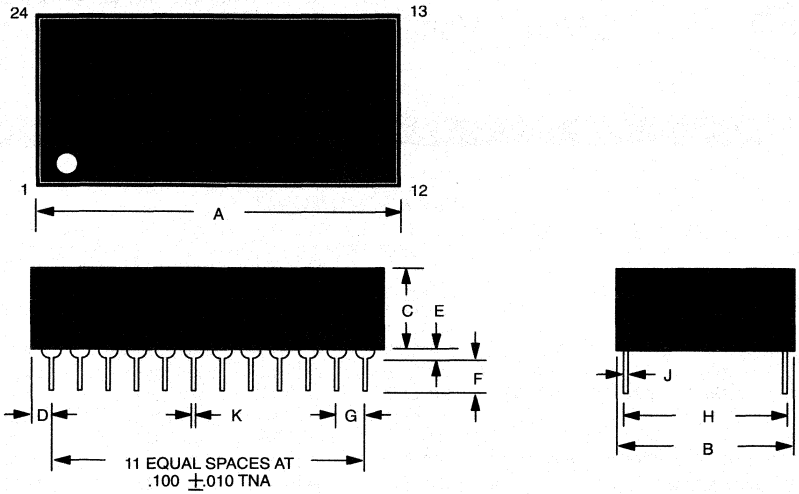
DS1685E 24-PIN TSSOP



DIMENSIONS ARE IN MILLIMETERS

DIM	MIN	MAX
A	–	1.10
A1	0.05	–
A2	0.75	1.05
c	0.09	0.18
phi	0°	8°
L	0.50	0.70
e1	0.65 BSC	
B	0.18	0.30
D	7.55	8.00
E	4.40 NOM	
G	0.25 REF	
H	6.25	6.55

DS1687 REAL TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.675 17.15	0.700 17.78
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

DS1688/DS1691
3 Volt/5 Volt Serialized Real Time Clock with NVRAM Control

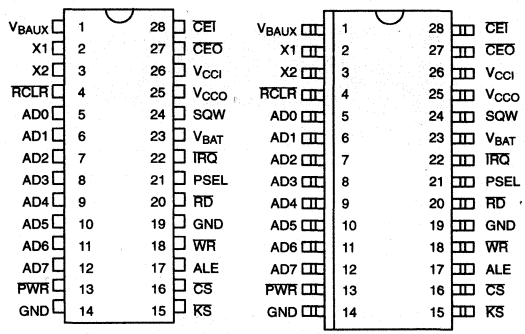
FEATURES
Incorporates industry standard DS1287 PC clock plus enhanced features:

- +3 or +5 volt operation
- 64–bit Silicon serial number
- 64–bit customer specific ROM or additional serial number available
- Power control circuitry supports system power on from date/time alarm or key closure
- Automatic battery backup and write protection to external SRAM
- Crystal select bit allows RTC to operate with 6 pF or 12.5 pF crystal
- 114 bytes user NVRAM
- Auxiliary battery input
- RAM clear input
- Century register
- 32 KHz output for power management
- 32–bit V_{CC} powered elapsed time counter
- 32–bit V_{BAT} powered elapsed time counter
- 16–bit power cycle counter
- Compatible with existing BIOS for original DS1287 functions
- Available as chip (DS1688) or stand–alone module with embedded battery and crystal (DS1691)

ORDERING INFORMATION

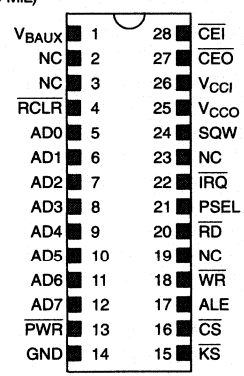
PART #	DESCRIPTION
DS1688	RTC Chip, 28–pin DIP
DS1688S	RTC Chip, 28–pin SOIC
DS1691	RTC Module;28–pin DIP

PIN ASSIGNMENT



DS1688 28-PIN DIP (600 MIL)

DS1688S 28-PIN SOIC (330 MIL)



DS1691 28-PIN ENCAPSULATED PACKAGE (740 MIL)

PIN DESCRIPTION

X1	-	Crystal Input
X2	-	Crystal Output
RCLR	-	RAM Clear Input
AD0-AD7	-	Mux'ed Address/Data Bus
PWR	-	Power–on Interrupt Output
KS	-	Kickstart Input
CS	-	RTC Chip Select Input
ALE	-	RTC Address Strobe
WR	-	RTC Write Data Strobe
RD	-	RTC Read Data Strobe
V_{CCO}	-	RAM Power Supply Output

$\overline{IRQ}$	-	Interrupt Request Output
SQW	-	Square Wave Output
V_{CCI}	-	+3 or +5 Volt Main Supply
GND	-	Ground
V_{BAT}	-	Battery + Supply
V_{BAUX}	-	Auxiliary Battery Supply
PSEL	–	+3 or +5 Volt Power Select
$\overline{CEI}$	–	RAM Chip Enable In
$\overline{CEO}$	–	RAM Chip Enable Out

DESCRIPTION

The DS1688/DS1691 is a real time clock (RTC) designed as a successor to the industry standard DS1285, DS1385, DS1485, and DS1585 PC real time clocks. This device provides the industry standard DS1285 clock function with the new feature of either +3.0 or +5.0 volt operation and automatic backup and write protection to an external SRAM. The DS1688 also incorporates a number of enhanced features including a silicon serial number, power on/off control circuitry, 114 bytes of user NVSRAM, power on elapsed timer, and power cycle counter.

Each DS1688/DS1691 is individually manufactured with a unique 64-bit serial number as well as an additional 64–bit customer specific ROM or serial number. The serial number is programmed and tested at Dallas to insure that no two devices are alike. The serial number can be used to electronically identify a system for purposes such as establishment of a network node address or for maintenance tracking. Blocks of available numbers from Dallas Semiconductor can be reserved by the customer.

The serialized RTC's also incorporate power control circuitry which allows the system to be powered on via an external stimulus, such as a keyboard or by a time and date (wake up) alarm. The $\overline{PWR}$ output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS1688/DS1691 incorporates a power on elapsed time counter, a power on cycle counter, and a battery powered continuous counter. These three counters provide valuable information for maintenance and warranty requirements.

Automatic backup and write protection for an external SRAM is provided through the V_{CCO} and $\overline{CEO}$ pins. The lithium energy source used to permanently power the real time clock is also used to retain RAM data in the absence of V_{CC} power through the V_{CCO} pin. The chip enable output to RAM ($\overline{CEO}$) is controlled during power transients to prevent data corruption.

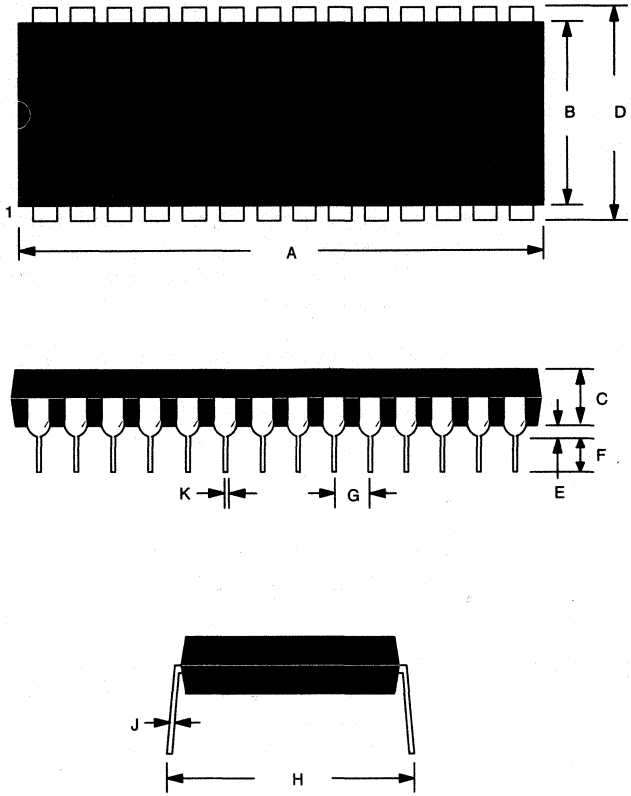
The DS1688 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time–of–day and memory status in the absence of power. The DS1691 incorporates the DS1688 chip, a 32.768 KHz crystal, and a lithium battery in a complete, self–contained timekeeping module. The entire unit is fully tested at Dallas Semiconductor such that a minimum of 10 years of timekeeping and data retention in the absence of V_{CC} is guaranteed.

For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than the SQW output, see the DS1689/DS1693 data sheet.

SIGNAL DESCRIPTION

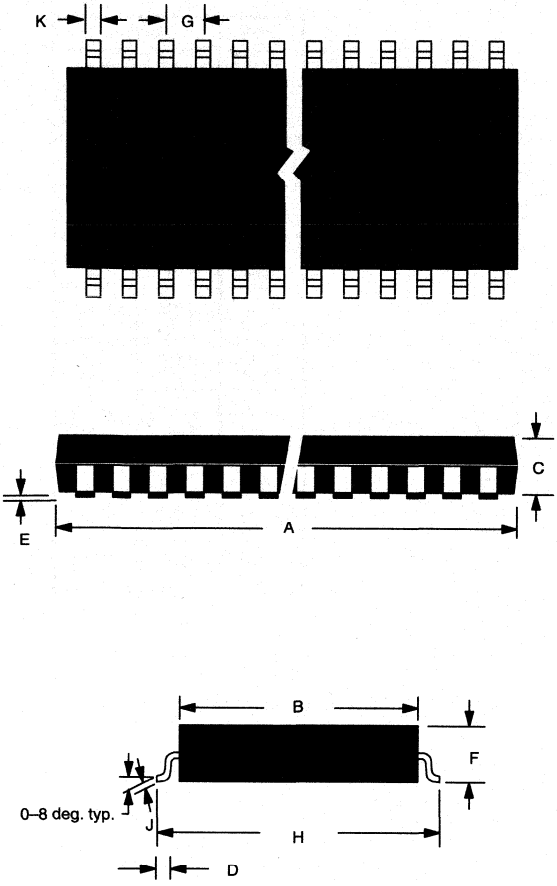
SQW (Square Wave Output) – The SQW output signal functions identical to the DS1689/DS1693 with an exception occurring at power–up. A 32 KHz square wave will be output on this pin, t_{REC}, after a power–up condition has been detected. This condition sets the following bits enabling the 32 KHz output; DV1=1, SQWE=1, and E32K=1. The square wave will be output on this pin if either SQWE=1 or E32K=1.

DS1688 28–PIN DIP



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.445	1.470
MM	36.70	37.34
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

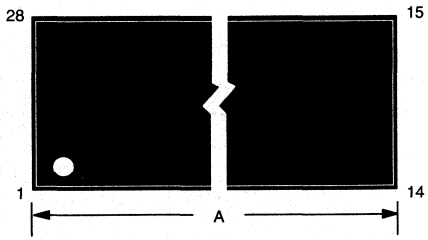
DS1688S 28–PIN SOIC

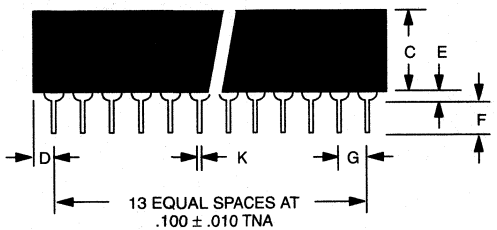


PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480 12.19
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51

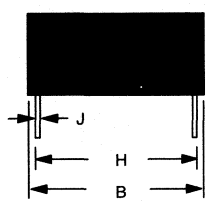
3

DS1691 28 PIN 740 MIL MODULE





PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.740
MM	17.65	18.80
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



NOTE: PINS 2, 3, 19 AND 23 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

DS1689/DS1693
3 Volt/5 Volt Serialized Real Time Clock with NVRAM Control

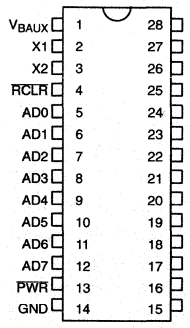
FEATURES
Incorporates industry standard DS1287 PC clock plus enhanced features:

- +3 or +5 volt operation
- 64–bit Silicon serial number
- 64–bit customer specific ROM or additional serial number available
- Power control circuitry supports system power on from date/time alarm or key closure
- Automatic battery backup and write protection to external SRAM
- Crystal select bit allows RTC to operate with 6 pF or 12.5 pF crystal
- 114 bytes user NVRAM
- Auxiliary battery input
- RAM clear input
- Century register
- 32 KHz output for power management
- 32–bit V_{CC} powered elapsed time counter
- 32–bit V_{BAT} powered elapsed time counter
- 16–bit power cycle counter
- Compatible with existing BIOS for original DS1287 functions
- Available as chip (DS1689) or standalone module with embedded battery and crystal (DS1693)
- Chips are available in industrial temperature version

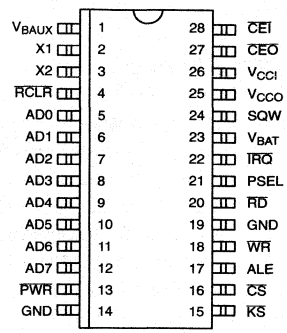
ORDERING INFORMATION

PART #	DESCRIPTION
DS1689	RTC Chip, 28–pin DIP
DS1689S	RTC Chip, 28–pin SOIC
DS1693	RTC Module; 28–pin DIP

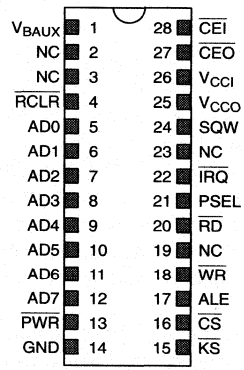
PIN ASSIGNMENT



DS1689 28-PIN DIP (600 MIL)



DS1689S 28-PIN SOIC (330 MIL)



DS1693 28-PIN ENCAPSULATED PACKAGE (740 MIL)

PIN DESCRIPTION

X1	–	Crystal Input
X2	–	Crystal Output
$\overline{RCLR}$	–	RAM Clear Input
AD0-AD7	–	Mux'ed Address/Data Bus
$\overline{PWR}$	–	Power–on Interrupt Output (open drain)
$\overline{KS}$	–	Kickstart Input
$\overline{CS}$	–	RTC Chip Select Input
ALE	–	RTC Address Strobe
$\overline{WR}$	–	RTC Write Data Strobe
$\overline{RD}$	–	RTC Read Data Strobe
V_{CCO}	–	RAM Power Supply Output

042795 1/30

$\overline{IRQ}$	–	Interrupt Request Output (open drain)
SQW	–	Square Wave Output
V_{CCI}	–	+3 or +5 Volt Main Supply
GND	–	Ground
V_{BAT}	–	Battery + Supply
V_{BAUX}	–	Auxiliary Battery Supply
PSEL	–	+3 or +5 Volt Power Select
$\overline{CEI}$	–	RAM Chip Enable In
$\overline{CEO}$	–	RAM Chip Enable Out

DESCRIPTION

The DS1689/DS1693 is a real time clock (RTC) designed as a successor to the industry standard DS1285, DS1385, DS1485, and DS1585 PC real time clocks. This device provides the industry standard DS1285 clock function with the new feature of either +3.0 or +5.0 volt operation and automatic backup and write protection to an external SRAM. The DS1689 also incorporates a number of enhanced features including a silicon serial number, power on/off control circuitry, 114 bytes of user NVSRAM, power on elapsed timer, and power cycle counter.

Each DS1689/DS1693 is individually manufactured with a unique 64-bit serial number as well as an additional 64–bit customer specific ROM or serial number. The serial number is programmed and tested at Dallas to insure that no two devices are alike. The serial number can be used to electronically identify a system for purposes such as establishment of a network node address or for maintenance tracking. Blocks of available numbers from Dallas Semiconductor can be reserved by the customer.

The serialized RTC's also incorporate power control circuitry which allows the system to be powered on via an external stimulus, such as a keyboard or by a time and date (wake up) alarm. The $\overline{PWR}$ output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS1689/DS1693 incorporates a power on elapsed time counter, a power on cycle counter, and a battery powered continuous counter. These three counters provide valuable information for maintenance and warranty requirements.

Automatic backup and write protection for an external SRAM is provided through the V_{CCO} and $\overline{CEO}$ pins. The lithium energy source used to permanently power the real time clock is also used to retain RAM data in the absence of V_{CC} power through the V_{CCO} pin. The chip enable output to RAM ($\overline{CEO}$) is controlled during power transients to prevent data corruption.

The DS1689 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time–of–day and memory status in the absence of power. The DS1693 incorporates the DS1689 chip, a 32.768 KHz crystal, and a lithium battery in a complete, self–contained timekeeping module. The entire unit is fully tested at Dallas Semiconductor such that a minimum of 10 years of timekeeping and data retention in the absence of V_{CC} is guaranteed.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1689/DS1693. The following paragraphs describe the function of each pin.

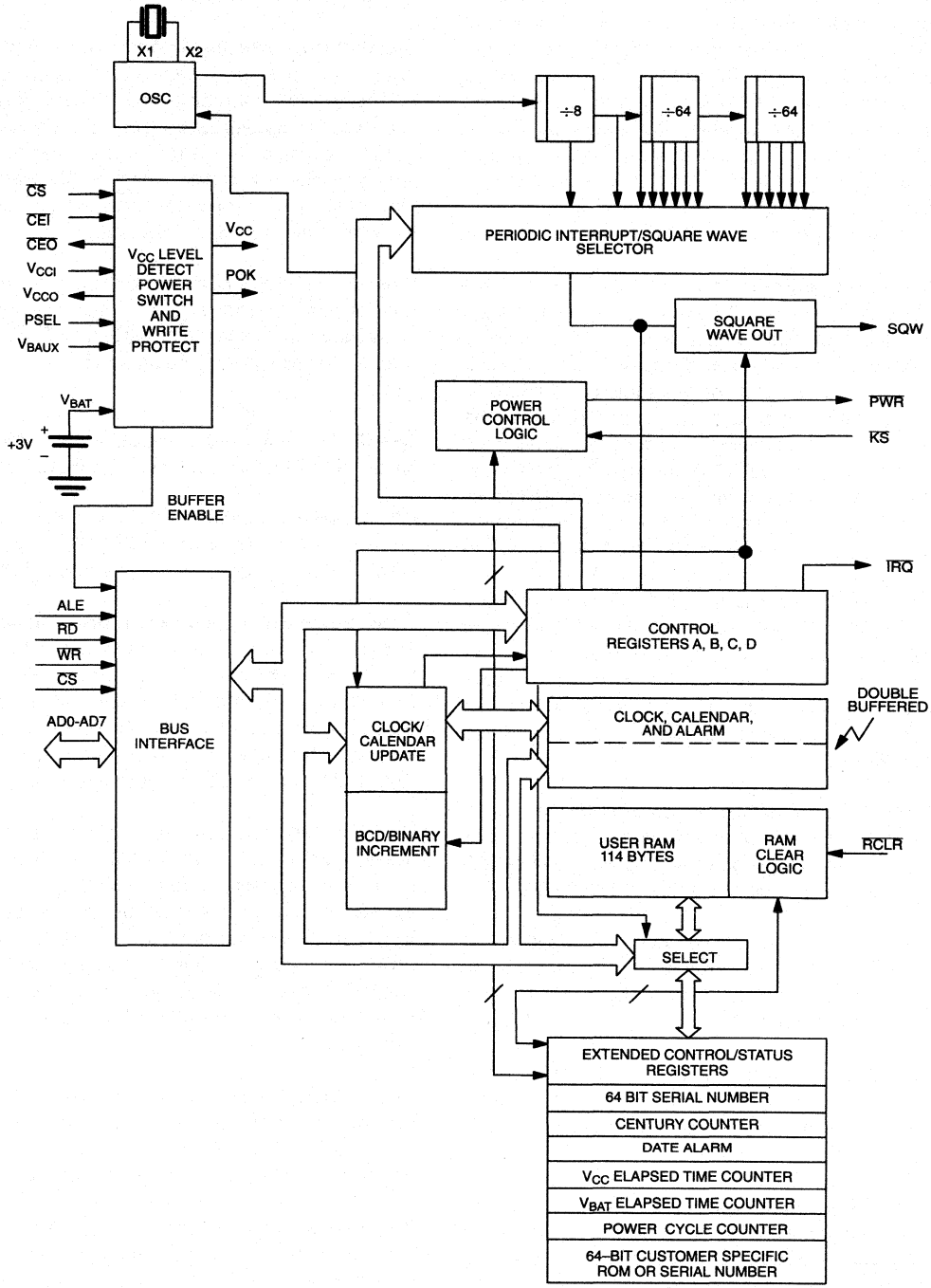
SIGNAL DESCRIPTIONS

GND, V_{CCI} - DC power is provided to the device on these pins. V_{CCI} is the +3 volt or +5 volt input. Five volt operation is selected when the PSEL pin is at a logic 1. If PSEL is floated or at a logic 0, the device will be in autosense mode and will determine the correct operating voltage based on the V_{CCI} voltage level.

PSEL (Power Select Input) – This pin selects whether 3 volt operation or 5 volt operation will be used. When PSEL is a logic 1, 5 volt operation is selected. When PSEL is a logic 0 or is floated, the device will be in autosense mode and will determine the correct mode of operation based on the voltage on V_{CCI}.

V_{CCO} (External SRAM Power Supply Output) – This pin will be internally connected to V_{CCI} when V_{CCI} is within nominal limits. However, during power fail, V_{CCO} will be internally connected to the V_{BAT} or V_{BAUX} (whichever is larger). For 5 volt operation, switch over from V_{CCI} to the backup supply occurs when V_{CCI} drops below the larger of V_{BAT} and V_{BAUX}. For 3 volt operation, switch over from V_{CCI} to the backup supply occurs at V_{PF} if V_{PF} is less than V_{BAT} and V_{BAUX}. If V_{PF} is greater than V_{BAT} and V_{BAUX}, the switch from V_{CCI} to the backup supply occurs when V_{CCI} drops below the larger of V_{BAT} and V_{BAUX}.

DS1689/DS1693 BLOCK DIAGRAM Figure 1



SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. A 32 KHz SQW signal is output when SQWE=1, the Enable 32 KHz (E32K) bit in extended register 04BH is a logic one, and V_{CC} is above V_{PF}. A 32 KHz square wave is also available when V_{CC} is less than V_{PF} if E32K=1, ABE=1, and voltage is applied to V_{BAUX}.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1689 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, at which time the DS1689/DS1693 latches the address. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ pulse. In a read cycle the DS1689/DS1693 outputs 8 bits of data during the latter portion of the $\overline{RD}$ pulse. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high. The address/data bus also serves as a bidirectional data path for the external extended RAM.

ALE (RTC Address Strobe Input; active high) - A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1689/DS1693.

$\overline{RD}$ (RTC Read Input; active low) - $\overline{RD}$ identifies the time period when the DS1689/DS1693 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

$\overline{WR}$ (RTC Write Input; active low) -The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed register.

$\overline{CS}$ (RTC Chip Select Input; active low) - The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1689/DS1693 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place with ALE asserted but without asserting $\overline{CS}$ will latch addresses. However, no data transfer will occur.

$\overline{IRQ}$ (Interrupt Request Output; open drain, active low) - The $\overline{IRQ}$ pin is an active low output of the DS1689/DS1693 that can be tied to the interrupt input of a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application software must clear all enabled flag bits contributing to IRQ's active state.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ pin is an open drain output and requires an external pull-up resistor.

$\overline{CEI}$ (RAM Chip Enable Input; active low) – $\overline{CEI}$ should be driven low to enable the external RAM.

$\overline{CEO}$ (RAM Chip Enable Output; active low) – When power is valid, $\overline{CEO}$ will equal $\overline{CEI}$. When power is not valid, $\overline{CEO}$ will be driven high regardless of $\overline{CEI}$.

$\overline{PWR}$ (Power On Output; open drain, active low) - The $\overline{PWR}$ pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the DS1689/DS1693, $\overline{PWR}$ may be automatically activated from a Kickstart input via the $\overline{KS}$ pin or from a Wake Up interrupt. Once the system is powered on, the state of $\overline{PWR}$ can be controlled via bits in the Dallas registers.

$\overline{KS}$ (Kickstart Input; active low) - When V_{CC} is removed from the DS1689/DS1693, the system can be powered on in response to an active low transition on the $\overline{KS}$ pin, as might be generated from a key closure. V_{BAUX} must be present and Auxiliary Battery Enable bit (ABE) must be set to 1 if the kickstart function is used, and the $\overline{KS}$ pin must be pulled up to the V_{BAUX} supply. While V_{CC} is applied, the $\overline{KS}$ pin can be used as an interrupt input.

$\overline{RCLR}$ (RAM Clear Input; active low) - If enabled by software, taking $\overline{RCLR}$ low will result in the clearing of the 114 bytes of user RAM. When enabled, $\overline{RCLR}$ can be activated whether or not V_{CC} is present.

V_{BAUX} - Auxiliary battery input required for kickstart and wake up features. This input also supports clock/calendar and External NVRAM if V_{BAT} is at lower voltage or is not present. A standard +3 volt lithium cell or other ener-

gy source can be used. Battery voltage must be held between +2.5 and +3.7 volts for proper operation. If V_{BAUX} is not going to be used it should be grounded and auxiliary battery enable bit bank 1, register 4BH, should=0.

DS1689 ONLY

X1, X2 - Connections for a standard 32.768 KHz quartz crystal. For greatest accuracy, the DS1689 must be used with a crystal that has a specified load capacitance of either 6 pF or 12.5 pF. The Crystal Select (CS) bit in Extended Control Register 4B is used to select operation with a 6 pF or 12.5 pF crystal. The crystal is attached directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal by guard–ringed with ground and that high frequency signals be kept away from the crystal area.

For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks". The DS1689 can also be driven by an external 32.768 KHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

V_{BAT} - Battery input for any standard 3 Volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation.

POWER–DOWN/POWER–UP CONSIDERATIONS

The real-time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CCI} input. When V_{CCI} is applied to the DS1689/DS1693 and reaches a level of greater than V_{PF} (power fail trip point), the device becomes accessible after t_{REC}, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied.

When PSEL is floating or logic 0, the DS1689 is in autosense mode and 3 volt or 5 volt operation is determined based on the voltage on V_{CCI}. Selection of 5 volt operation is automatically invoked when V_{CCI} rises above 4.5 volts for a minimum of t_{REC}. However, 3 volt operation is automatically selected if V_{CCI} does not rise above the level of 4.25 volts. Selection of the power supply input levels requires 150 ms of input stability before operation can commence.

When 5 volt operation is selected, the device is fully accessible and data can be written and read only when V_{CCI} is greater than 4.5 volts. When V_{CCI} is below 4.5 volts, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below the greater of V_{BAT} and V_{BAUX}, the RAM and timekeeper are switched over to a lithium battery connected either to the V_{BAT} pin or V_{BAUX} pin.

When 3 volt operation is selected and applied within normal limits, the device is fully accessible and data can be written or read. When V_{CCI} falls below V_{PF}, access to the device is inhibited. If V_{PF} is less than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CCI} to the backup supply (the greater of V_{BAT} and V_{BAUX}) when V_{CCI} drops below V_{PF}. If V_{PF} is greater than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CCI} to the backup supply when V_{CCI} drops below the larger of V_{BAT} and V_{BAUX}.

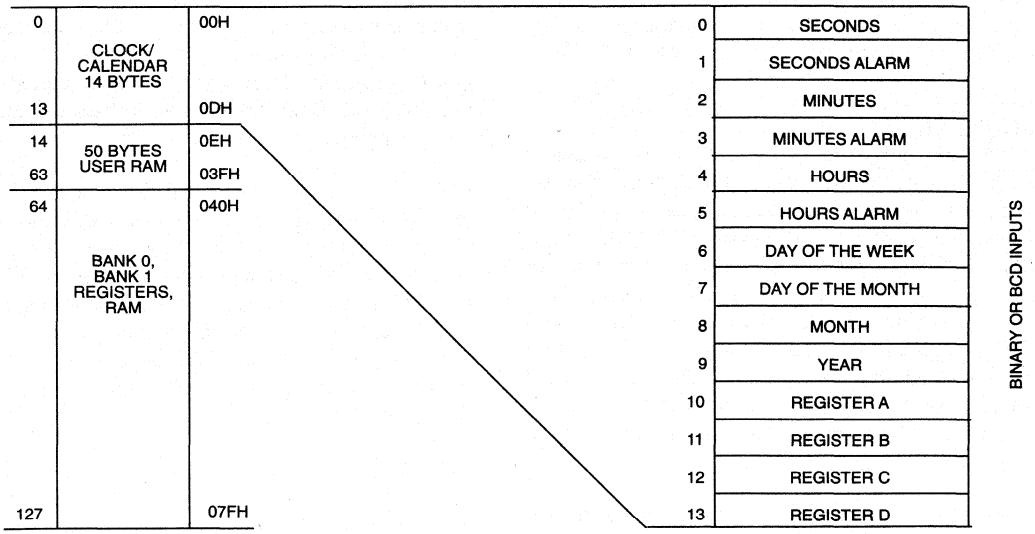
When V_{CC} falls below V_{PF}, the chip is write-protected. With the possible exception of the $\overline{KS}$, $\overline{PWR}$, and SQW pins, all inputs are ignored and all outputs are in a high impedance state.

RTC ADDRESS MAP

The address map for the RTC registers of the DS1689/DS1693 is shown in Figure 2. The address map consists of the 14 clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and four bytes are used for control and status. All registers can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

DS1689 REAL TIME CLOCK ADDRESS MAP Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching will be explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The four alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second use condition is to insert a "don't care" state in one or more of the four alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second. The three alarm bytes may be used in conjunction with the date alarm as described in the Wakeup/Kickstart section. The century counter will be discussed later in this text.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
00H	Seconds	0-59	00-3B	00-59
01H	Seconds Alarm	0-59	00-3B	00-59
02H	Minutes	0-59	00-3B	00-59
03H	Minutes Alarm	0-59	00-3B	00-59
04H	Hours 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours 24-Hour Mode	0-23	00-17	00-23
05H	Hours Alarm 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92 PM
	Hours Alarm 24-hr. Mode	0-23	00-17	00-23
06H	Day of Week Sunday=1	1-7	01-07	01-07
07H	Date of Month	1-31	01-1F	01-31
08H	Month	1-12	01-0C	01-12
09H	Year	0-99	00-63	00-99
BANK 1, 48H	Century	0-99	00-63	00-99
BANK 1, 49H	Date Alarm	1-31	01-1F	01-31

CONTROL REGISTERS

The four control registers; A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

NONVOLATILE RAM - RTC

The 114 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1689/DS1693. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible when bank 0 is selected.

INTERRUPT CONTROL

The DS1689/DS1693 includes six separate, fully automatic sources of interrupt for a processor:

1. Alarm interrupt
2. Periodic interrupt
3. Update-ended interrupt
4. Wake up interrupt
5. Kickstart interrupt
6. RAM clear interrupt

The conditions which generate each of these independent interrupt conditions are described in greater detail elsewhere in this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are a total of six bits including three bits in Register B and three bits in Extended Register B which enable the interrupts. The extended register locations are described later. Writing a logic 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ will immediately be set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits which are set remain stable throughout the read cycle. All bits which were set are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the $\overline{IRQ}$ line will be driven low when an interrupt flag bit is set and its corresponding enable bit is also set. $\overline{IRQ}$ will be held low as long as at least one of the six possible interrupt sources has it s flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS1689/DS1693 initiated an interrupt is accomplished by reading Register C and finding IRQF=1. IRQF will remain set until all enabled interrupt flag bits are cleared to 0.

SQUARE WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768 KHz crystal tied to X1 and X2. The square wave output is enabled and disabled via the SQWE bit in Register B. If the square wave is enabled (SQWE=1), then the output frequency will be determined by the settings of the E32K bit in Extended Register B and by the RS3-0 bits in Register A. If the E32K = 1, then a 32.768 KHz square wave will be output on the SQW pin regardless of the settings of RS3-0.

If E32K = 0, then the square wave output frequency is determined by the RS3-0 bits. These bits control a 1-of-15 decoder which selects one of thirteen taps that divide the 32.768 KHz frequency. The RS3-0 bits establish the SQW output frequency as shown in Table 2. In addition, RS3-0 bits control the periodic interrupt selection as described below.

If SQWE1, E32K=1, and the Auxiliary Battery Enable bit (ABE, bank 1; register 04BH) is enabled, and voltage is applied to V_{BAUX} then the 32 KHz square wave output signal will be output on the SQW pin in the absence of V_{CC}. This facility is provided to clock external power management circuitry. If any of the above requirements are not met, no square wave output signal will be generated on the SQW pin in the absence of V_{CC}.

A pattern of 01X in the DV2, DV1, and DV0, bits respectively, will turn the oscillator on and enable the countdown chain. Note that this is different than the DS1287, which required a pattern of 010 in these bits. DV0 is now a "don't care" because it is used for selection between register banks 0 and 1.

A pattern of 11X will turn the oscillator on, but the oscillator's countdown chain will be held in reset, as it was in the DS1287. Any other bit combination for DV2 and DV1 will keep the oscillator off.

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3-0 bits in Register A which select the square wave frequency (see Table 2). Changing the bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The Serialized RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, alarm and elapsed time byte is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows the time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

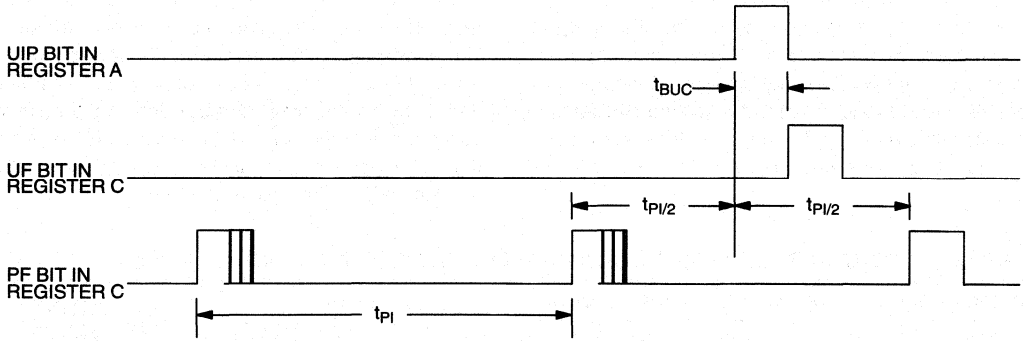
PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

EXT. REG. B	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
E32K	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625 ms	256 Hz
0	0	0	1	0	7.8125 ms	128 Hz
0	0	0	1	1	122.070 µs	8.192 KHz
0	0	1	0	0	244.141 µs	4.096 KHz
0	0	1	0	1	488.281 µs	2.048 KHz
0	0	1	1	0	976.5625 µs	1.024 KHz
0	0	1	1	1	1.953125 ms	512 Hz
0	1	0	0	0	3.90625 ms	256 Hz
0	1	0	0	1	7.8125 ms	128 Hz
0	1	0	1	0	15.625 ms	64 Hz
0	1	0	1	1	31.25 ms	32 Hz
0	1	1	0	0	62.5 ms	16 Hz
0	1	1	0	1	125 ms	8 Hz
0	1	1	1	0	250 ms	4 Hz
0	1	1	1	1	500 ms	2 Hz
1	X	X	X	X	*	32.768 KHz

*RS3-RS0 determine periodic interrupt rates as listed for E32K=0.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within (t_{PI} / 2+t_{BUC}) to ensure that data is not read during the update cycle.

UPDATE–ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1
t_{BUC} = DELAY TIME BEFORE UPDATE CYCLE = 244 µs

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2 - These bits are defined as follows:

DV2 = Countdown Chain
1 - resets countdown chain only if DV1=1
0 - countdown chain enabled

DV1 = Oscillator Enable
0 - oscillator off
1 - oscillator on

DV0 = Bank Select
0 - original bank
1 - extended registers

A pattern of 01X is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 01X is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

Enable the interrupt with the PIE bit;

Enable the SQW output pin with the SQWE bit;

Enable both at the same time and the same rate; or

Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1689/DS1693.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1689/DS1693 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1689/DS1693 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 and the E32K bit is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 am to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 WF = WIE = 1
AF = AIE = 1 KF = KSE = 1
UF = UIE = 1 RF = RIE = 1

i.e., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE) + (WF • WIE) + (KF • KSE) + (RF • RIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 0 THROUGH BIT 3 - These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit indicates the condition of the battery connected to the V_{BAT} pin or the battery connected to V_{BAUX}, whichever is at a higher voltage. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

EXTENDED FUNCTIONS

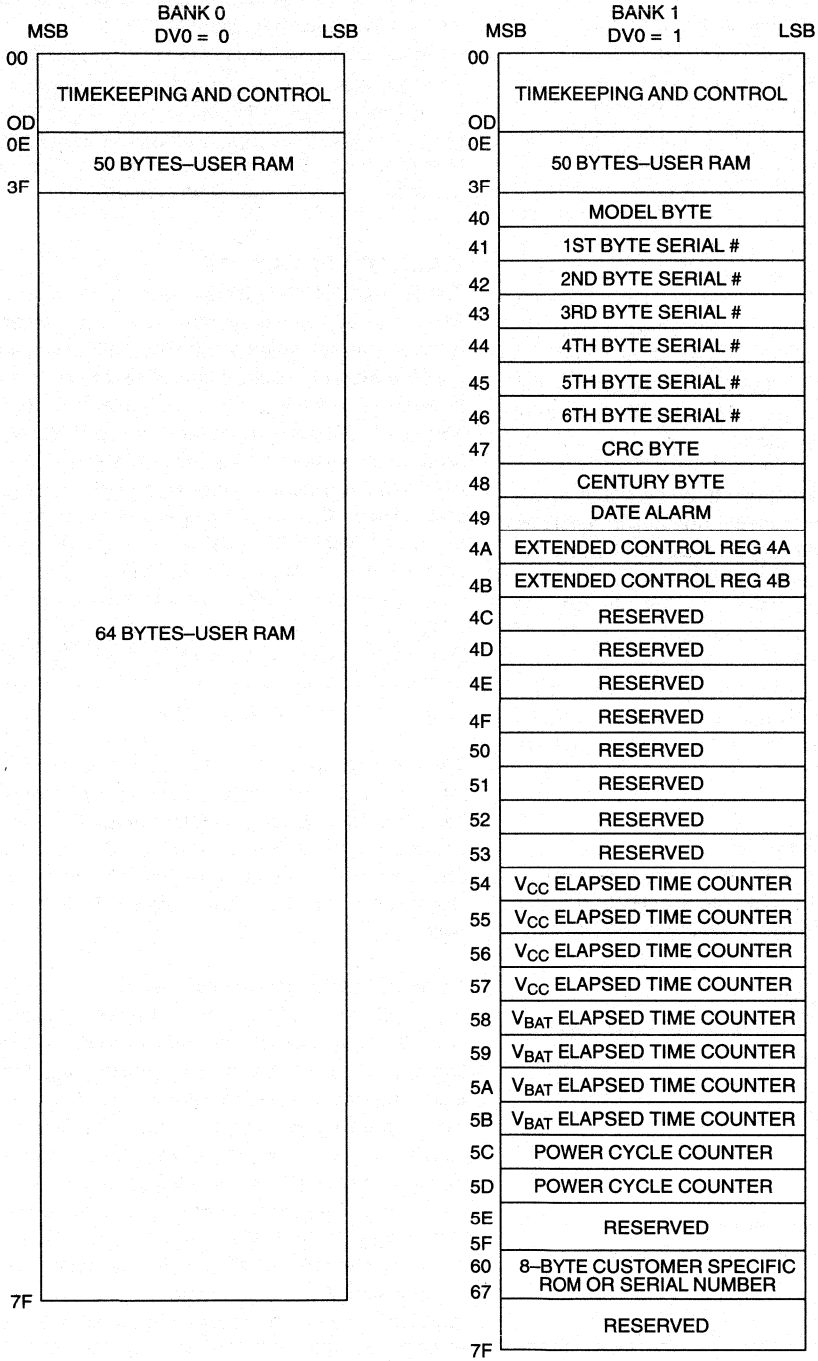
The extended functions provided by the DS1689/DS1693 that are new to the RAMified RTC family are accessed via a software controlled bank switching scheme, as illustrated in Figure 4. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS1689/DS1693 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers which provide control and status for the extended functions will be accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

1. Silicon Revision byte
2. Serial Number
3. Eight Byte Customer Specific ROM or Serial Number
4. Century counter
5. Auxiliary Battery Control/Status
6. Wake Up
7. Kickstart
8. RAM Clear Control/Status
9. V_{CC} Powered Elapsed Time Counter
10. V_{BAT} Powered Elapsed Time Counter
11. Power On Cycle Counter

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and will return a 0 if read.

DS1689/DS1693 EXTENDED REGISTER BANK DEFINITION Figure 4



SILICON SERIAL NUMBER/CUSTOMER SPECIFIC ROM

A total of 128 bits are available for use as serial number/ ROM. These bits may be used as a 128–bit serial number or as a unique 64–bit serial number and 64–bit customer specific serial number or ROM. The unique 64-bit serial number is located in bank 1 registers 40H-47H. This serial number is divided into three parts. The first byte in register 40H contains a model number to identify the device type and revision of the DS1689/DS1693. Registers 41H-46H contain a unique binary number. Register 47H contains a CRC byte used to validate the data in registers 40H-46H. The method used to create the CRC byte is proprietary to Dallas Semiconductor, but can be made available if required. Typical applications should consider this byte simply as part of the overall unique serial number. All 8 bytes of the serial number are read only registers.

The DS1689/DS1693 is manufactured such that no two devices will contain an identical number in locations 41H-47H. Blocks of numbers for these locations can be reserved by the customer. Contact Dallas Semiconductor for special ordering information for DS1689/DS1693 with reserved blocks of serial numbers.

As already mentioned, another 64 bits are available for use as an additional serial number or customer specific ROM. These 64 bits are located in bank 1 registers 60H–67H.

CENTURY COUNTER

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

AUXILIARY BATTERY

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS1689/DS1693 kickstart, wake up, and SQW output features in the absence of V_{CC}. This power source must be available in order to use these auxiliary features when no V_{CC} is applied to the device.

The Auxiliary Battery Enable (ABE; bank 1, register 04BH) bit in extended control register B is used to turn on and off the auxiliary battery for the above functions in the absence of V_{CC}. When set to a 1, V_{BAUX} battery power is enabled, and when cleared to 0, V_{BAUX} battery power is disabled to these functions.

In the DS1689/DS1693, this auxiliary battery may be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended external RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS1689 is to be backed-up using a single battery with the auxiliary features enabled, then V_{BAUX} should be used and connected to V_{BAT}. If V_{BAUX} is not to be used, it should be grounded and ABE should be cleared to 0.

WAKE UP/KICKSTART

The DS1689/DS1693 incorporates a wake up feature which can power the system on at a pre-determined date through activation of the $\overline{PWR}$ output pin. In addition, the kickstart feature can allow the system to be powered up in response to a low going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin. As a result, system power may be applied upon such events as a key closure, or modem ring detect signal. In order to use either the wake up or the kickstart features, the DS1689/DS1693 must have an auxiliary battery connected to the V_{BAUX} pin and the oscillator must be running and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the $\overline{PWR}$ pin will not be driven low in response to a kickstart or wakeup condition, while in battery-backed mode.

The wake up feature is controlled through the Wake up Interrupt Enable bit in extended control register B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake up feature, clearing WIE to 0 disables it. Similarly, the kickstart feature is controlled through the Kickstart Interrupt Enable bit in extended control register B (KSE, bank 1, 04BH).

A wake up sequence will occur as follows: When wake up is enabled via WIE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar will monitor the current date for a match condition with the date alarm register (bank 1, register 049H). In conjunction with the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake up will occur at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm will occur regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the $\overline{PWR}$ pin will automatically be driven low. This output can be used to turn on the main system power supply

which provides V_{CC} voltage to the DS1689/DS1693 as well as the other major components in the system. Also at this time, the Wake Up flag (WF, bank 1, register 04AH) will be set, indicating that a wake up condition has occurred.

A kickstart sequence will occur when kickstarting is enabled via KSE = 1. While the system is powered down, the $\overline{KS}$ input pin will be monitored for a low going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line will be pulled low, as it is for a wake up condition. Also at this time, the Kickstart Flag (KF, bank 1, register 04AH) will be set, indicating that a kickstart condition has occurred.

The timing associated with both the wake up and kickstarting sequences is illustrated in the Wake Up / Kickstart Timing Diagram in the Electrical Specifications section of this data sheet. The timing associated with these functions is divided into 5 intervals, labeled 1-5 on the diagram.

The occurrence of either a kickstart or wake up condition will cause the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS1689/DS1693 V_{CC} pin rises above the 3 volt power fail level before the power on timeout period (t_{POTO}) expires, then $\overline{PWR}$ will remain at the active low level. If V_{CC} does not rise above the 3 volt power fail voltage in this time, then the $\overline{PWR}$ output pin will be turned off and will return to its high impedance level. In this event, the $\overline{IRQ}$ pin will also remain tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power on sequence will remain set until cleared by software during a subsequent system power on.

If V_{CC} is applied within the timeout period, then the system power on sequence will continue as shown in intervals 2-5 in the timing diagram. During interval 2, $\overline{PWR}$ will remain active and $\overline{IRQ}$ will be driven to its active low level, indicating that either WF or KF was set in initiating the power on. In the diagram $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit will be automatically cleared to 0 in response to a successful power on. The $\overline{PWR}$ line will remain active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing zeroes to both of these control bits. As long as no other interrupt within the DS1689/DS1693 is pending, the $\overline{IRQ}$ line will be taken inactive once these bits are reset. Execution of the application software may proceed. During this time, both the wake up and kickstart functions may be used to generate status and interrupts. WF will be set in response to a date, hours, and minutes match condition. KF will be set in response to a low going transition on $\overline{KS}$. If the associated interrupt enable bit is set (WIE and/or KSE) then the $\overline{IRQ}$ line will driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS1689/DS1693 may cause $\overline{IRQ}$ to be driven low. While system power is applied, the on chip logic will always attempt to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake up or kickstart.

The system may be powered down under software control by setting the PAB bit to a logic 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ}$ output pin will be placed in a high impedance state when V_{CC} goes below V_{PF}. If the system is to be again powered on in response to a wake up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and nonvolatile RAM is in effect, $\overline{PWR}$ and $\overline{IRQ}$ are tri-stated, and monitoring of wake up and kickstart takes place.

RAM CLEAR

The DS1689/DS1693 provides a RAM clear function for the 114 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V_{CC} pin.

The RAM clear function is enabled or disabled via the RAM Clear Enable bit (RCE; bank 1, register 04BH). When this bit is set to a logic 1, the 114 bytes of user RAM will be cleared (all bits set to 1) when an active low transition is sensed on the $\overline{RCLR}$ pin. This action will have no effect on either the clock/calendar settings or upon the contents of the external extended RAM. The RAM clear Flag (RF, bank 1, register 04BH) will be set when the RAM clear operation has been completed. If V_{CC} is present at the time of the RAM clear and RIE=1, the $\overline{IRQ}$ line will also be driven low upon completion. The interrupt condition can be cleared by writing a zero to the RF bit. The $\overline{IRQ}$ line will then return to its inactive high level provided there are no other pending interrupts. Once the $\overline{RCLR}$ pin is activated, all read/write accesses are locked out for a minimum recover time, specified as t_{REC} in the Electrical Characteristics section.

When RCE is cleared to zero, the RAM clear function is disabled. The state of the $\overline{RCLR}$ pin will have no effect on the contents of the user RAM, and transitions on the $\overline{RCLR}$ pin have no effect on RF.

EXTENDED CONTROL REGISTERS

Two extended control registers are provided to supply controls and status information for the extended features offered by the DS1689/DS1693. These are designated as extended control registers A and B and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows.

EXTENDED CONTROL REGISTER 4A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	*	*	PAB	RF	WF	KF

VRT2 - This status bit gives the condition of the auxiliary battery. It is set to a logic 1 condition when the external lithium battery is connected to the V_{BAUX}. If this bit is read as a logic 0, the external battery should be replaced.

INCR - Increment in Progress status bit. This bit is set to a 1 when an increment to the time/date registers is in progress and the alarm checks are being made. INCR will be set to a 1 at 122 µs before the update cycle starts and will be cleared to 0 at the end of each update cycle.

PAB - Power Active Bar control bit. When this bit is 0, the $\overline{PWR}$ pin is in the active low state. This bit can be written to a logic 1 or 0 by the user. If either WF AND WIE = 1 OR KF AND KSE = 1, the PAB bit will be cleared to 0.

RF - Ram Clear Flag. This bit will be set to a logic 1 when a high to low transition occurs on the $\overline{RCLR}$ input if RCE=1. The RF bit is cleared by writing it to a logic 0. This bit can also be written to a logic 1 to force an interrupt condition.

WF - Wake up Alarm Flag - This bit is set to 1 when a wake up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

KF - Kickstart Flag - This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

EXTENDED CONTROL REGISTER 4B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32K	CS	RCE	PRS	RIE	WIE	KSE

ABE - Auxiliary Battery Enable. This bit when written to a logic 1 will enable the V_{BAUX} pin for extended functions.

E32K - Enable 32,768 output. This bit when written to a logic 1 will enable the 32,768 Hz oscillator frequency to be output on the SQW pin provided SQWE=1.

CS – Crystal Select Bit. When CS is set to a 0, the oscillator is configured for operation with a crystal that has a 6 pF specified load capacitance. When CS=1, the oscillator is configured for a 12.5 pF crystal.

RCE - RAM Clear Enable bit. When set to a 1, this bit enables a low level on pin 4 ($\overline{RCLR}$) to clear all 114 bytes of user RAM. When RCE = 0, the RAM clear function is disabled.

PRS – PAB Reset Select Bit. When set to a 0 the $\overline{PWR}$ pin will be set hi–Z when the DS1689 goes into power fail. When set to a 1, the $\overline{PWR}$ pin will remain active upon entering power fail.

RIE - Ram Clear Interrupt Enable. When RIE is set to a 1, the $\overline{IRQ}$ pin will be driven low when a RAM clear function is completed.

WIE - Wake Up Alarm Interrupt Enable. When V_{CC} voltage is absent and WIE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a wake up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If WIE is set while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to WF being set to 1. When WIE is cleared to a 0, the WF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

KSE - Kickstart Interrupt Enable. When V_{CC} voltage is absent and KSE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If KSE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to KF being set to 1. When KSE is cleared to a 0, the KF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

* Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no effect on operation.

ELAPSED TIME COUNTERS

The DS1689/DS1693 has two 32 bit elapsed time counters, which reside in bank 1 of the RTC registers. To access these counters the DV0 bit in register A must first be set to a logical 1.

The V_{CC} powered elapsed time counter resides in register 54H through 57H. The LSB of this counter resides in register 54 and the MSB is in 57H. The V_{CC} powered elapsed time counter runs only while the V_{CCI} input is within nominal limits. The elapsed time counter is a binary counter that records the number of seconds that have elapsed. The counter can be read or written at the users discretion. The V_{BAT} powered elapsed time counter resides in register 58H through 5BH. The LSB of this counter resides in register 58 and the MSB is in 5BH.

The V_{BAT} powered elapsed time counter runs continually as long as the V_{BAT} or V_{BAUX} pin is within nominal limits regardless of the condition of V_{CCI}. The number of seconds that have elapsed are recorded in a binary counter and the counter may be read or written at the user's discretion.

In a typical application the V_{BAT} powered elapsed time counter can be used to record the length of time that has elapsed from which the equipment which contains the device was first put into service. The V_{CC} powered counter can then be used to record the length of time that V_{CC} power is applied. These functions can be particularly useful for warranty and maintenance information. In addition, battery life can be predicted based on known loading factors. However, it is worth noting that a properly selected battery should power the DS1689/DS1693 and external RAM for the useful life of most equipment.

POWER CYCLE COUNTER

The DS1689/DS1693 has a 16 bit power cycle counter that resides in register 5C and 5D of bank 1. The LSB of this counter resides in 5C and the MSB is in 5D. This binary counter is incremented by 1 count each time V_{CCI} power is applied within nominal limits. This counter can be read or written at the user's discretion.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature DS1689 and DS1689S	–40°C to +85°C
Operating Temperature DS1693	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage 5 Volt Operation	V_{CCI}	4.5	5.0	5.5	V	1
Power Supply Voltage 3 Volt Operation	V_{CCI}	2.7	3.0	4.0	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		0.6	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	1
Auxiliary Battery Voltage	V_{BAUX}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.5V to 5.5 V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		7	15	mA	2, 3
CMOS Standby Current ($\overline{CS}$=V_{CC}-0.2V)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
$\overline{CEI}$ Input Leakage	$I_{\overline{CEI}}$	–200		+1	µA	15
PSEL Input Leakage	I_{PSEL}	–1		+200	µA	16
Output Leakage Current	I_{OL}	-1		+1	µA	8
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Output Voltage	V_{CCO1}	V_{CC}-0.3			V	4
Output Current	I_{CCO1}			85	mA	4
Power Fail Trip Point	V_{PF}	4.25	4.37	4.5	V	5
Battery Switch Voltage	V_{SW}		V_{BAT}, V_{BAUX}		V	
Output Voltage	V_{CCO2}	V_{BAT}-0.3			V	6

DC ELECTRICAL CHARACTERISTICS (cont'd) (0°C to 70°C; V_{CC}=4.5V to 5.5 V)

Output Current	I_{CCO2}	100			µA	6
Battery Leakage OSC ON	I_{BAT1}		500	1000	nA	
Battery Leakage OSC OFF	I_{BAT2}		50	150	nA	17
I/O Leakage	I_{LO}	–1		+1	µA	7
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			10.0	mA	1
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			60	Ω	12

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DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=2.7V to 4.0 V)

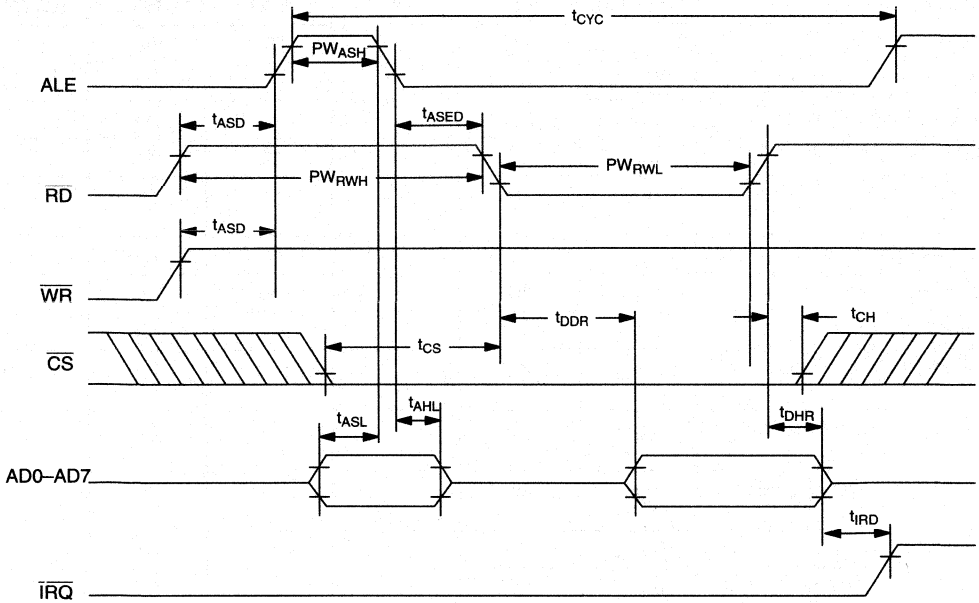
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		5	10	mA	2, 3
CMOS Standby Current ($\overline{CS}$=V_{CC}-0.2V)	I_{CC2}		0.5	2	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
$\overline{CEI}$ Input Leakage	$I_{\overline{CEI}}$	–160		+1	µA	15
PSEL Input Leakage	I_{PSEL}	+1		–160	µA	16
Output Leakage Current	I_{OL}	+160		–1	µA	8
Output Logic 1 Voltage @ 0.4 mA	V_{OH}	2.4			V	
Output Logic 0 Voltage @ 0.8 mA	V_{OL}			0.4	V	
Output Voltage	V_{CCO1}	V_{CC}-0.3			V	4
Output Current	I_{CCO1}			50	mA	4
Power Fail Trip Point	V_{PF}	2.5	2.6	2.7	V	5
Output Voltage	V_{CCO2}	V_{BAT}-0.3			V	6
Output Current	I_{CCO2}	100			µA	6
Battery Leakage OSC ON	I_{BAT1}		500	1000	nA	
Battery Leakage OSC OFF	I_{BAT2}		50	150	nA	17
I/O Leakage	I_{LO}	–1		+1	µA	7
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			4	mA	1
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			120	Ω	12

RTC AC TIMING CHARACTERISTICS

(0°C to 70°C; V_{CC} = 2.7V to 4.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	915		DC	ns	
Pulse Width, $\overline{RD}/\overline{WR}$ Low	PW_{RWL}	375			ns	
Pulse Width, $\overline{RD}/\overline{WR}$ High	PW_{RWH}	450			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	75			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		120	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	90			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	30			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	30			ns	
Pulse Width ALE High	PW_{ASH}	180			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	120			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		370	ns	9
Data Setup Time	t_{DSW}	180			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	
$\overline{CEI}$ to $\overline{CEO}$ Delay	t_{CED}			20	ns	

DS1689/DS1693 BUS TIMING FOR READ CYCLE TO RTC

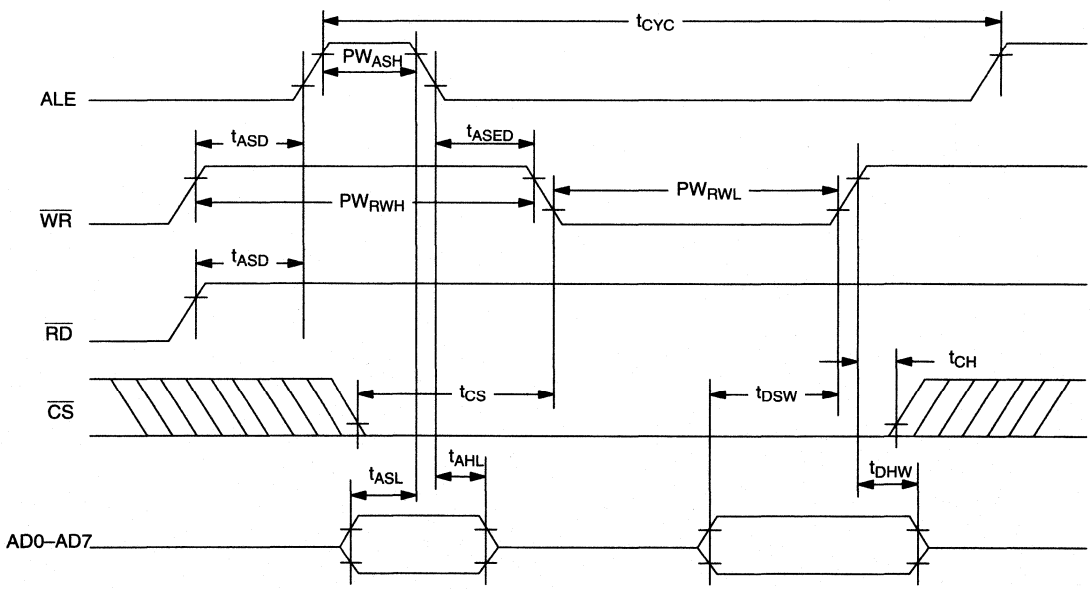


RTC AC TIMING CHARACTERISTICS

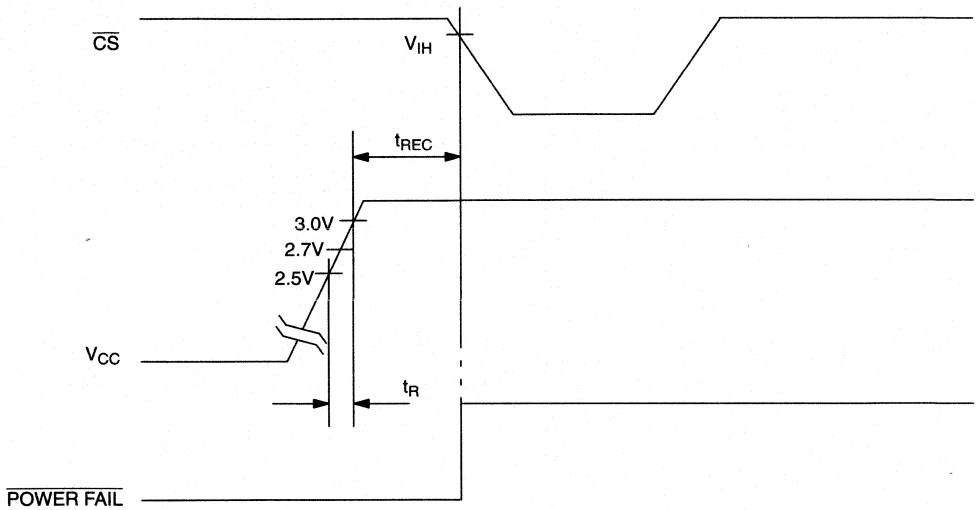
(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{RWL}	125			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{RWH}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	9
Data Setup Time	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	
$\overline{CEI}$ to $\overline{CEO}$ Delay	t_{CED}			10	ns	

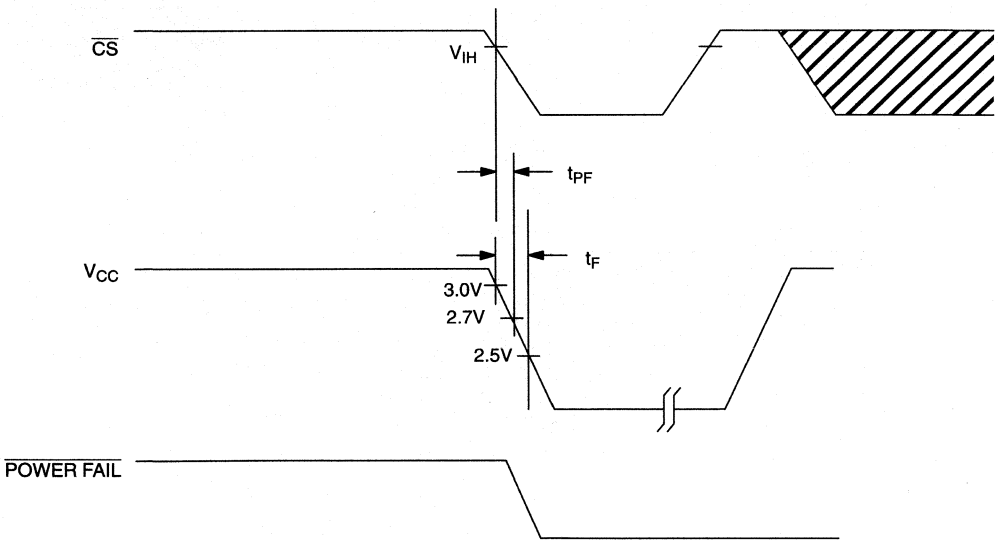
DS1689/DS1693 BUS TIMING FOR WRITE CYCLE TO RTC AND RTC REGISTERS



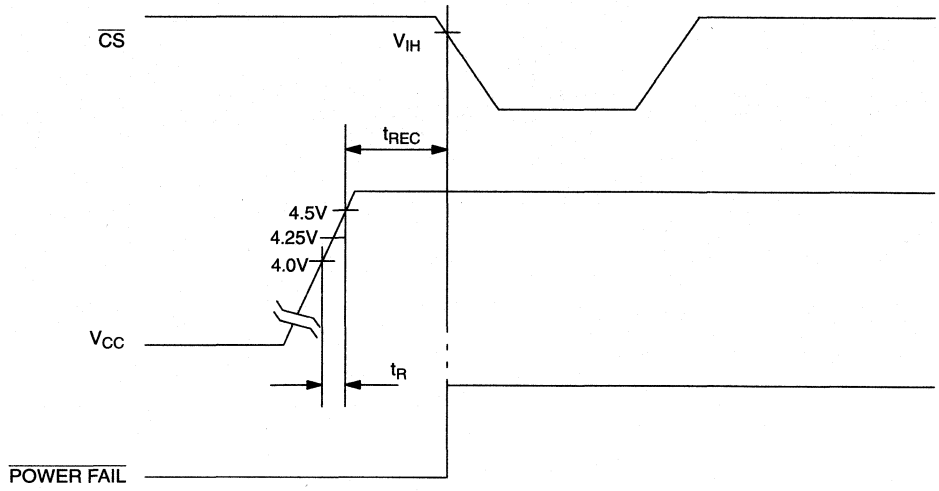
POWER–UP CONDITION 3 VOLT OPERATION



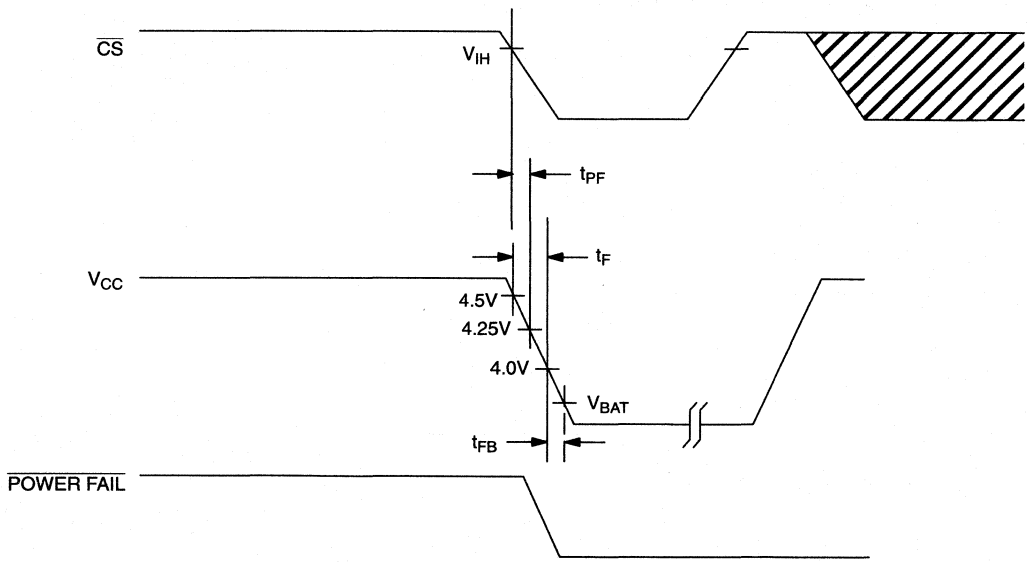
POWER–DOWN CONDITION 3 VOLT OPERATION



POWER–UP CONDITION 5.0 VOLT OPERATION



POWER–DOWN CONDITION 5.0 VOLT OPERATION



POWER-UP POWER-DOWN TIMING 5 VOLT OPERATION

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	13, 14

POWER-UP POWER-DOWN TIMING 3 VOLT OPERATION

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $2.5 \le V_{CC} \le 3.0V$	300			µs	
V_{CC} Slew Rate Power Up	t_R $3.0V \ge V_{CC} \ge 2.5V$	0			µs	
Expected Data Retention	t_{DR}	10			years	13, 14

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

(t_A = 25°C)

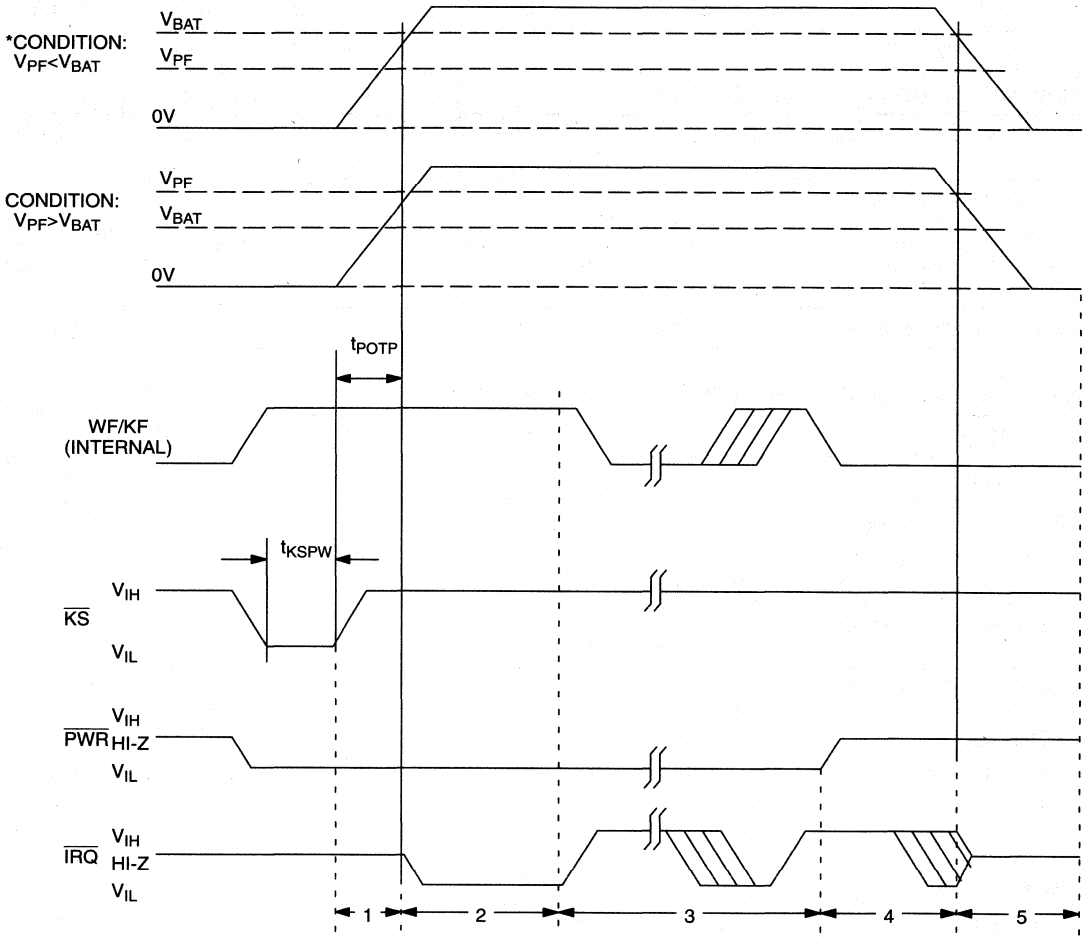
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

WAKE UP/KICKSTART TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t_{KSPW}	2			µs	
Wake up/Kickstart Power On Timeout	t_{POTO}	2			seconds	10

WAKE UP/KICKSTART TIMING



NOTE:

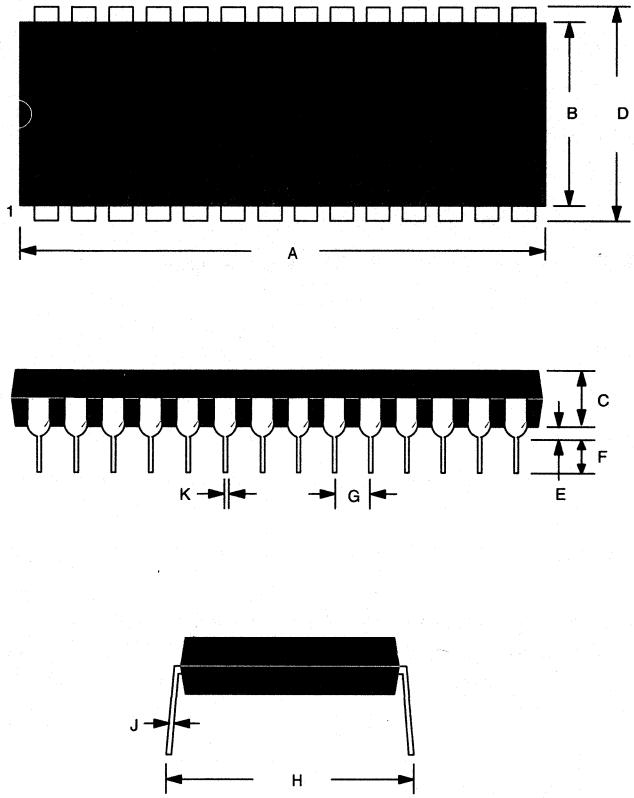
Time intervals shown above are referenced in Wake up/Kickstart section.

* This condition can occur when the device is operated in 3 volt mode.

NOTES:

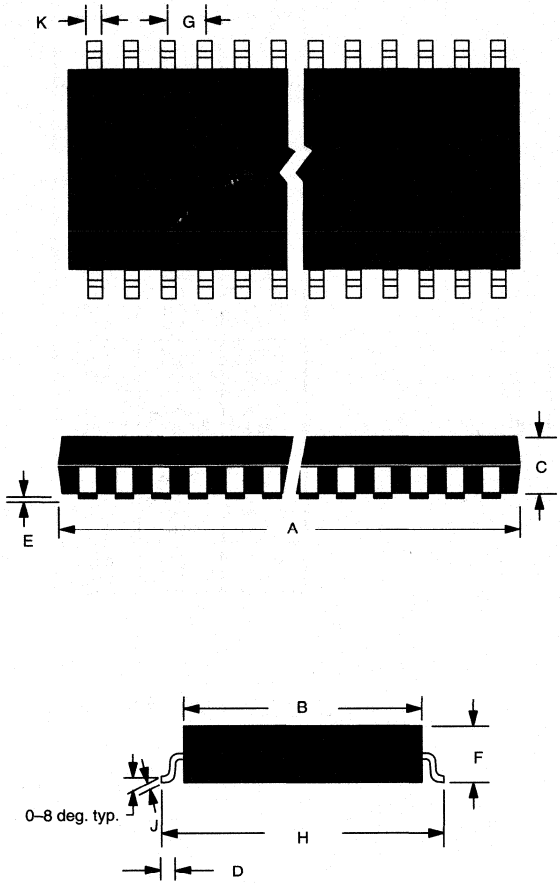
1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Value for voltage and currents is from the V_{CCI} input pin to the V_{CCO} pin.
5. Write protection trip point occurs during power fail prior to switchover from V_{CC} to V_{BAT}.
6. Value for voltage and currents is from the V_{BAT} input pin to the V_{CCO} pin.
7. Applies to the AD0–AD7 pins, and the SQW pin when each is in a high impedance state.
8. The $\overline{IRQ}$ pin is open drain.
9. Measured with a load of 50 pF + 1 TTL gate.
10. Wakeup kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.
11. V_{SW} is determined by the larger of V_{BAT} and V_{BAUX}.
12. Z_{CE} is an average input to output impedance as the input is swept from GND to V_{CCI} and less than 4 mA is forced through Z_{CE}.
13. The DS1693 will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
14. t_{DR} is the amount of time that the internal battery can power the internal oscillator and internal registers of the DS1693. As such, t_{DR} is specified with V_{CCO} floating. If V_{CCO} is powering an external SRAM, an auxiliary battery must be connected to the V_{BAUX} pin. The auxiliary battery should be sized such that it can power the external SRAM for the t_{DR} period.
15. The $\overline{CEI}$ pin has an internal pull–up of 60 KΩ.
16. The PSEL pin has an internal pull–down of 60 KΩ..
17. For industrial grade parts, I_{BAT} (with OSC off) limit increases to 250 nA.

DS1689 28–PIN DIP



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.445 36.70	1.470 37.34
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.625 15.88	0.675 17.15
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

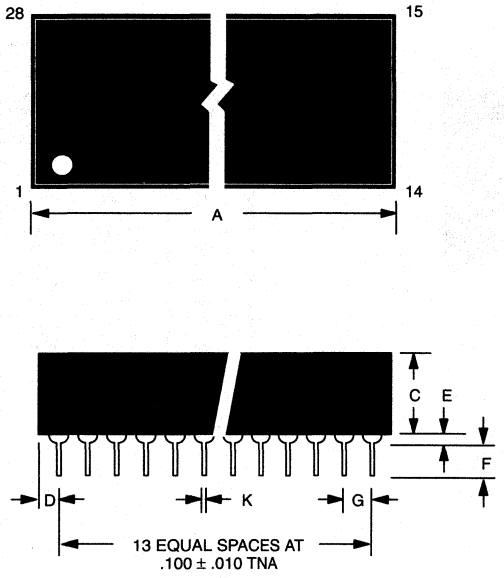
DS1689S 28–PIN SOIC



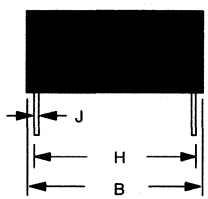
PKG	28-PIN	
DIM	MIN	MAX
A IN.	0.706	0.728
MM	17.93	18.49
B IN.	0.338	0.350
MM	8.58	8.89
C IN.	0.086	0.110
MM	2.18	2.79
D IN.	0.020	0.050
MM	0.58	1.27
E IN.	0.002	0.014
MM	0.05	0.36
F IN.	0.090	0.124
MM	2.29	3.15
G IN.	0.050	BSC
MM	1.27	
H IN.	0.460	0.480
MM	11.68	12.19
J IN.	0.006	0.013
MM	0.15	0.33
K IN.	0.014	0.020
MM	0.36	0.51

3

DS1693 28 PIN 740 MIL MODULE



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.740
MM	17.65	18.80
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



NOTE: PINS 2, 3, 19 AND 23 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

DS17285/DS17287
3 Volt/5 Volt Real Time Clock

3

FEATURES

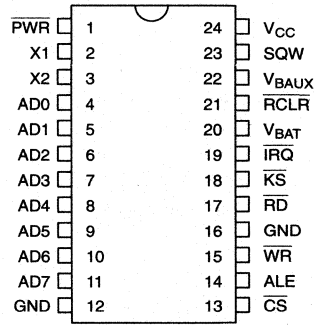
Incorporates industry standard DS1287 PC clock plus enhanced features:

- +3 or +5 volt operation
- SMI recovery stack
- 64–bit silicon serial number
- Power control circuitry supports system power on from date/time alarm or key closure
- 32 KHz output on power–up
- Crystal select bit allows RTC to operate with 6 pF or 12.5 pF crystal
- 114 bytes user NVRAM
- 2K bytes of additional NVRAM
- Auxiliary battery input
- RAM clear input
- Century register
- Date alarm register
- Compatible with existing BIOS for original DS1287 functions
- Available as chip (DS17285) or standalone module with embedded battery and crystal (DS17287)

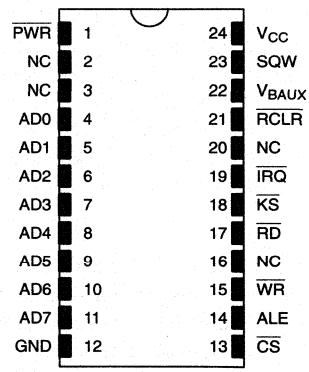
ORDERING INFORMATION

PART #	DESCRIPTION
DS17285–X	RTC Chip; 24–pin DIP
DS17285S–X	RTC Chip; 24–pin SOIC
DS17285E–X	RTC Chip; 28–pin TSOP
DS17287–X	RTC Module; 24–pin DIP
–3	+3 volt device
–5	+5 volt device

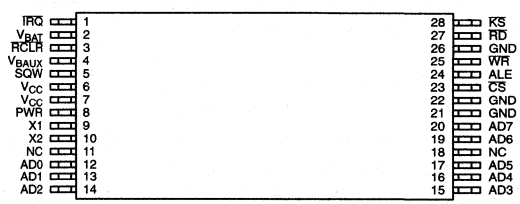
PIN ASSIGNMENT



DS17285 24–PIN DIP
DS17285S 24–PIN SOIC



DS17287 24–PIN ENCAPSULATED PACKAGE



DS17285E 28–PIN TSOP

PIN DESCRIPTION

X1	–	Crystal Input
X2	–	Crystal Output
$\overline{RCLR}$	–	RAM Clear Input
AD0-AD7	–	Mux'ed Address/Data Bus
$\overline{PWR}$	–	Power–on Interrupt Output (open drain)
$\overline{KS}$	–	Kickstart Input
$\overline{CS}$	–	RTC Chip Select Input
ALE	–	RTC Address Strobe
$\overline{WR}$	–	RTC Write Data Strobe
$\overline{RD}$	–	RTC Read Data Strobe
$\overline{IRQ}$	–	Interrupt Request Output (open drain)
SQW	–	Square Wave Output
V_{CC}	–	+3 or +5 Volt Main Supply
GND	–	Ground
V_{BAT}	–	Battery + Supply
V_{BAUX}	–	Auxiliary Battery Supply
NC	–	No Connection

DESCRIPTION

The DS17285/DS17287 is a real time clock (RTC) designed as a successor to the industry standard DS1285, DS1385, DS1485, DS1585, and DS1685 PC real time clocks. This device provides the industry standard DS1285 clock function with either +3.0 or +5.0 volt operation. The DS17285 also incorporates a number of enhanced features including a silicon serial number, power on/off control circuitry, 114 bytes of user NVSRAM plus 2K bytes of additional NVRAM, and 32.768 KHz output for sustaining power management activities.

The DS17285/DS17287 power control circuitry allows the system to be powered on via an external stimulus, such as a keyboard or by a time and date (wake up) alarm. The $\overline{PWR}$ output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS17285 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time–of–day and memory status in the absence of power. The DS17287 incorporates the DS17285 chip, a 32.768 KHz crystal, and a lithium battery in a complete, self–contained timekeeping module. The entire unit is fully tested at Dallas Semiconductor such that a minimum of 10 years of timekeeping and data retention in the absence of V_{CC} is guaranteed.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS17285/DS17287. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +3 volt or +5 volt input.

SQW (Square Wave Output) - The SQW pin will provide a 32 KHz square wave output, t_{REC}, after a power–up condition has been detected. This condition sets the following bits, enabling the 32 KHz output; DV1=1, and E32K=1. A square wave will be output on this pin if either SQWE=1 or E32K=1. If E32K=1, then 32 KHz will be output regardless of the other control bits. If E32K=0, then the output frequency is dependent on the control bits in register A. The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in register B or the E32K bit in extended register 4Bh. A 32 KHz SQW signal is output when the Enable 32 KHz (E32K) bit in extended register 4Bh is a logic one, and V_{CC} is above V_{PF}. A 32 KHz square wave is also available when V_{CC} is less than V_{PF} if E32K=1, ABE=1, and voltage is applied to the V_{BAUX} pin.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS17285 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, at which time the DS17285/DS17287 latches the address. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ pulse. In a read cycle the DS17285/DS17287 outputs 8 bits of data during the latter portion of the $\overline{RD}$ pulse. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high. The address/data bus also serves as a bidirectional data path for the external extended RAM.

ALE (RTC Address Strobe Input; active high) - A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS17285/DS17287.

$\overline{RD}$ (RTC Read Input; active low) - $\overline{RD}$ identifies the time period when the DS17285/DS17287 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

$\overline{WR}$ (RTC Write Input; active low) -The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed register.

$\overline{CS}$ (RTC Chip Select Input; active low) - The Chip Select signal must be asserted low during a bus cycle for the DS17285/DS17287 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place with ALE asserted but without asserting $\overline{CS}$ will latch addresses. However, no data transfer will occur.

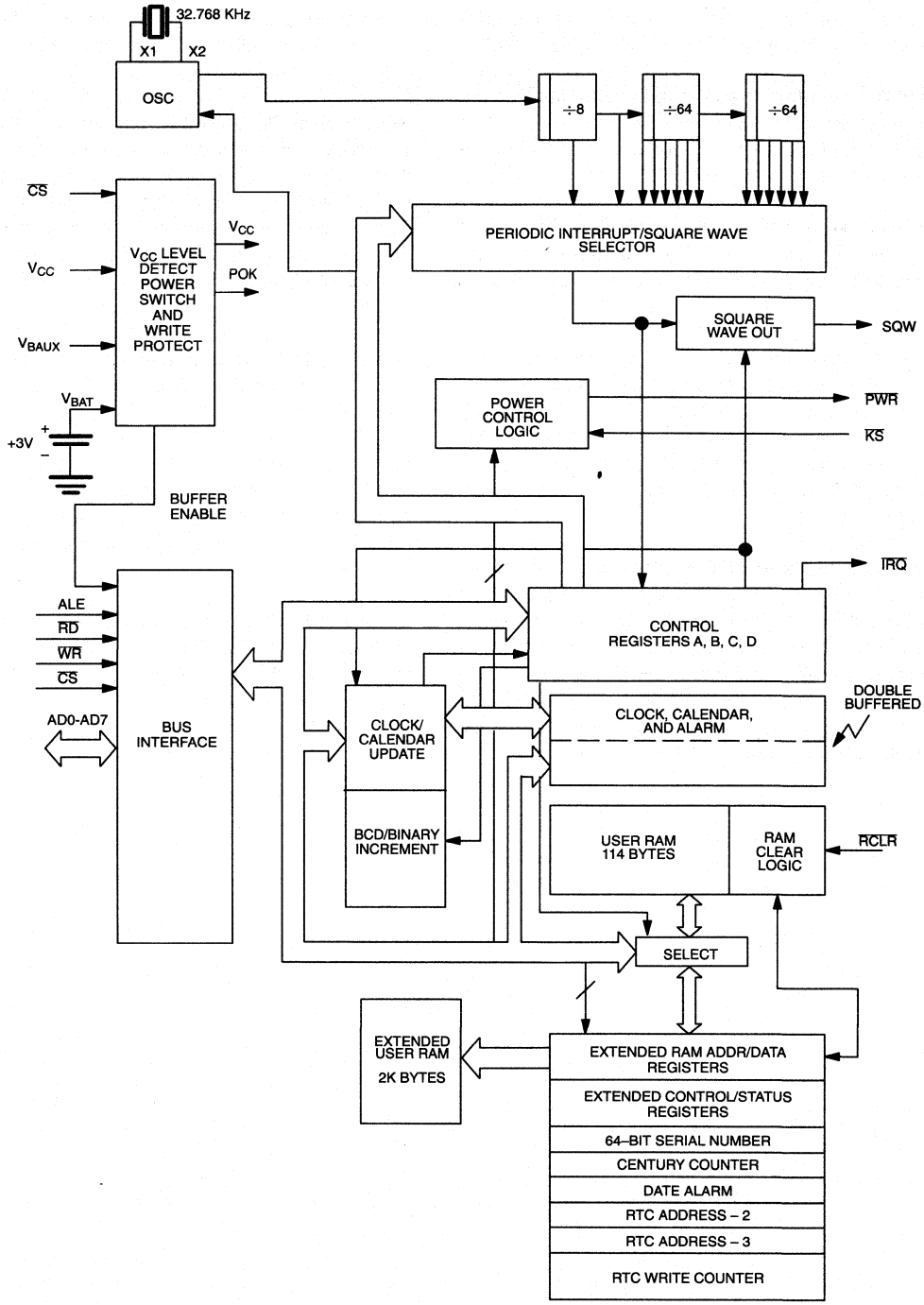
$\overline{IRQ}$ (Interrupt Request Output; open drain, active low) - The $\overline{IRQ}$ pin is an active low output of the DS17285/DS17287 that can be tied to the interrupt input of a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application software must clear all enabled flag bits contributing to $\overline{IRQ}$'s active state. When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ pin is an open drain output and requires an external pull-up resistor.

$\overline{PWR}$ (Power On Output; open drain, active low) - The $\overline{PWR}$ pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the DS17285/DS17287, $\overline{PWR}$ may be automatically activated from a Kickstart input via the $\overline{KS}$ pin or from a Wake Up interrupt. Once the system is powered on, the state of $\overline{PWR}$ can be controlled via bits in the Dallas registers.

$\overline{KS}$ (Kickstart Input; active low) - When V_{CC} is removed from the DS17285/DS17287, the system can be powered on in response to an active low transition on the $\overline{KS}$ pin, as might be generated from a key closure. V_{BAUX} must be present and Auxiliary Battery Enable bit (ABE) must be set to 1 if the kickstart function is used, and the $\overline{KS}$ pin must be pulled up to the V_{BAUX} supply. While V_{CC} is applied, the $\overline{KS}$ pin can be used as an interrupt input.

$\overline{RCLR}$ (RAM Clear Input; active low) - If enabled by software, taking $\overline{RCLR}$ low will result in the clearing of the 114 bytes of user RAM. When enabled, $\overline{RCLR}$ can be activated whether or not V_{CC} is present.

DS17285/DS17287 BLOCK DIAGRAM Figure 1



V_{BAUX} - Auxiliary battery input required for kickstart and wake up features. This input also supports clock/calendar and user RAM if V_{BAT} is at lower voltage or is not present. A standard +3 volt lithium cell or other energy source can be used. Battery voltage must be held between +2.5 and +3.7 volts for proper operation. If V_{BAUX} is not going to be used it should be grounded and auxiliary battery enable bit bank 1, register 4BH, should=0.

DS17285 ONLY

X1, X2 - Connections for a standard 32.768 KHz quartz crystal. For greatest accuracy, the DS17285 must be used with a crystal that has a specified load capacitance of either 6 pF or 12.5 pF. The Crystal Select (CS) bit in Extended Control Register 4B is used to select operation with a 6 pF or 12.5 pF crystal. The crystal is attached directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area.

For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks". The DS17285 can also be driven by an external 32.768 KHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

V_{BAT} - Battery input for any standard 3 Volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation.

POWER–DOWN/POWER–UP CONSIDERATIONS

The real-time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS17285/DS17287 and reaches a level of greater than V_{PF} (power fail trip point), the device becomes accessible after t_{REC}, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied.

The DS17285/DS17287 is available in either a 3 volt or a 5 volt device.

The 5 volt device is fully accessible and data can be written and read only when V_{CC} is greater than 4.5 volts. When V_{CC} is below 4.5 volts, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below the greater of V_{BAT} and V_{BAUX}, the RAM and timekeeper are switched over to a lithium battery connected either to the V_{BAT} pin or V_{BAUX} pin.

The 3 volt device is fully accessible and data can be written or read only when V_{CC} is greater than 2.7 volts. When V_{CC} falls below V_{PF}, access to the device is inhibited. If V_{PF} is less than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply (the greater of V_{BAT} and V_{BAUX}) when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply when V_{CC} drops below the larger of V_{BAT} and V_{BAUX}.

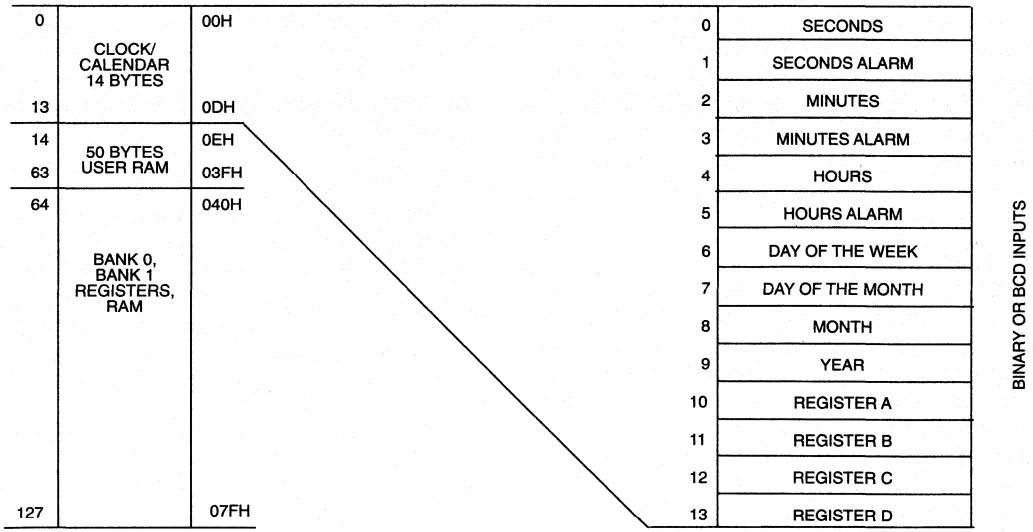
When V_{CC} falls below V_{PF}, the chip is write-protected. With the possible exception of the $\overline{KS}$, $\overline{PWR}$, $\overline{RCLR}$, and SQW pins, all inputs are ignored and all outputs are in a high impedance state.

RTC ADDRESS MAP

The address map for the RTC registers of the DS17285/DS17287 is shown in Figure 2. The address map consists of the 14 clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and four bytes are used for control and status. All registers can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

DS17285 REAL TIME CLOCK ADDRESS MAP Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching will be explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The four alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second use condition is to insert a "don't care" state in one or more of the four alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second. The three alarm bytes may be used in conjunction with the date alarm as described in the Wakeup/Kickstart section. The century counter will be discussed later in this text.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
00H	Seconds	0-59	00-3B	00-59
01H	Seconds Alarm	0-59	00-3B	00-59
02H	Minutes	0-59	00-3B	00-59
03H	Minutes Alarm	0-59	00-3B	00-59
04H	Hours 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours 24-Hour Mode	0-23	00-17	00-23
05H	Hours Alarm 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92 PM
	Hours Alarm 24-hr. Mode	0-23	00-17	00-23
06H	Day of Week Sunday=1	1-7	01-07	01-07
07H	Date of Month	1-31	01-1F	01-31
08H	Month	1-12	01-0C	01-12
09H	Year	0-99	00-63	00-99
BANK 1, 48H	Century	0-99	00-63	00-99
BANK 1, 49H	Date Alarm	1-31	01-1F	01-31

CONTROL REGISTERS

The four control registers; A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

NONVOLATILE RAM - RTC

The general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS17285/DS17287. They can be used by the application program as nonvolatile memory and are fully available during the update cycle.

The user RAM is divided into two separate memory banks. When the bank 0 is selected, the 14 real time clock registers and 114 bytes of user RAM are accessible. When bank 1 is selected, an additional 2K bytes of user RAM are accessible through the extended RAM address and data registers.

INTERRUPT CONTROL

The DS17285/DS17287 includes six separate, fully automatic sources of interrupt for a processor:

1. Alarm interrupt
2. Periodic interrupt
3. Update-ended interrupt
4. Wake up interrupt
5. Kickstart interrupt
6. RAM clear interrupt

The conditions which generate each of these independent interrupt conditions are described in greater detail elsewhere in this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are a total of six bits including three bits in Register B and three bits in Extended Register 4B which enable the interrupts. The extended register locations are described later. Writing a logic 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ will immediately be set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As

a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register 4A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register 4B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits which are set remain stable throughout the read cycle. All bits which were set are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register 4A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the $\overline{IRQ}$ line will be driven low when an interrupt flag bit is set and its corresponding enable bit is also set. $\overline{IRQ}$ will be held low as long as at least one of the six possible interrupt sources has it s flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS17285/DS17287 initiated an interrupt is accomplished by reading Register C and finding IRQF=1. IRQF will remain set until all enabled interrupt flag bits are cleared to 0.

SQUARE WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768 KHz crystal tied to X1 and X2. The square wave output is enabled and disabled via the SQWE bit in Register B or the E32K bit in extended register 4Bh. If the square wave is enabled (SQWE=1 or E32K=1), then the output frequency will be determined by the settings of the E32K bit in Extended Register 4Bh and by the RS3-0 bits in Register A. If E32K=1, then a 32.768 KHz square wave will be output on the SQW pin regardless of the settings of RS3-0 and SQWE.

If E32K = 0, then the square wave output frequency is determined by the RS3-0 bits. These bits control a 1-of-15 decoder which selects one of thirteen taps that divide the 32.768 KHz frequency. The RS3-0 bits establish the SQW output frequency as shown in Table 2. In addition, RS3-0 bits control the periodic interrupt selection as described below.

If E32K=1, and the Auxiliary Battery Enable bit (ABE, bank 1; register 04BH) is enabled, and voltage is applied to V_{BAUX} then the 32 KHz square wave output signal will be output on the SQW pin in the absence of V_{CC}. This facility is provided to clock external power management circuitry. If any of the above requirements are not met, no square wave output signal will be generated on the SQW pin in the absence of V_{CC}.

A pattern of 01X in the DV2, DV1, and DV0, bits respectively, will turn the oscillator on and enable the countdown chain. Note that this is different than the DS1287, which required a pattern of 010 in these bits. DV0 is now a "don't care" because it is used for selection between register banks 0 and 1.

A pattern of 11X will turn the oscillator on, but the oscillator's countdown chain will be held in reset, as it was in the DS1287. Any other bit combination for DV2 and DV1 will keep the oscillator off.

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3-0 bits in Register A which select the square wave frequency (see Table 2). Changing the bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE and E32K bits control the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The Serialized RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, alarm and elapsed time byte is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows the time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all alarm locations.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

3

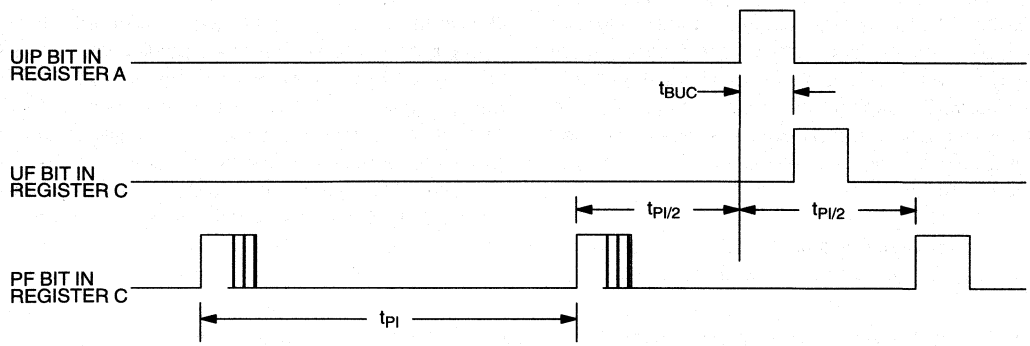
PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

EXT. REG. B	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
E32K	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625 ms	256 Hz
0	0	0	1	0	7.8125 ms	128 Hz
0	0	0	1	1	122.070 µs	8.192 KHz
0	0	1	0	0	244.141 µs	4.096 KHz
0	0	1	0	1	488.281 µs	2.048 KHz
0	0	1	1	0	976.5625 µs	1.024 KHz
0	0	1	1	1	1.953125 ms	512 Hz
0	1	0	0	0	3.90625 ms	256 Hz
0	1	0	0	1	7.8125 ms	128 Hz
0	1	0	1	0	15.625 ms	64 Hz
0	1	0	1	1	31.25 ms	32 Hz
0	1	1	0	0	62.5 ms	16 Hz
0	1	1	0	1	125 ms	8 Hz
0	1	1	1	0	250 ms	4 Hz
0	1	1	1	1	500 ms	2 Hz
1	X	X	X	X	*	32.768 KHz

*RS3-RS0 determine periodic interrupt rates as listed for E32K=0.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within (t_{PI} / 2+t_{BUC}) to ensure that data is not read during the update cycle.

UPDATE–ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1
t_{BUC} = DELAY TIME BEFORE UPDATE CYCLE = 244 µs

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These bits are defined as follows:

DV2 = Countdown Chain
- 1 - resets countdown chain only if DV1=1
- 0 - countdown chain enabled

DV1 = Oscillator Enable
- 0 - oscillator off
- 1 - oscillator on, V_{CC} power–up state

DV0 = Bank Select
- 0 - original bank
- 1 - extended registers

A pattern of 01X is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 01X is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

Enable the interrupt with the PIE bit;

Enable the SQW output pin with the SQWE or E32K bits;

Enable both at the same time and the same rate; or

Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS17285/DS17287.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS17285/DS17287 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS17285/DS17287 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one and E32K=0, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to zero and E32K=0, the SQW pin is held low. SQWE is a read/write bit. SQWE is set to a one when V_{CC} is powered up.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 WF = WIE = 1
AF = AIE = 1 KF = KSE = 1
UF = UIE = 1 RF = RIE = 1

i.e., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE) + (WF • WIE) + (KF • KSE) + (RF • RIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 3 THROUGH BIT 0 - These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit indicates the condition of the battery connected to the V_{BAT} pin or the battery connected to V_{BAUX}, whichever is at a higher voltage. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

EXTENDED FUNCTIONS

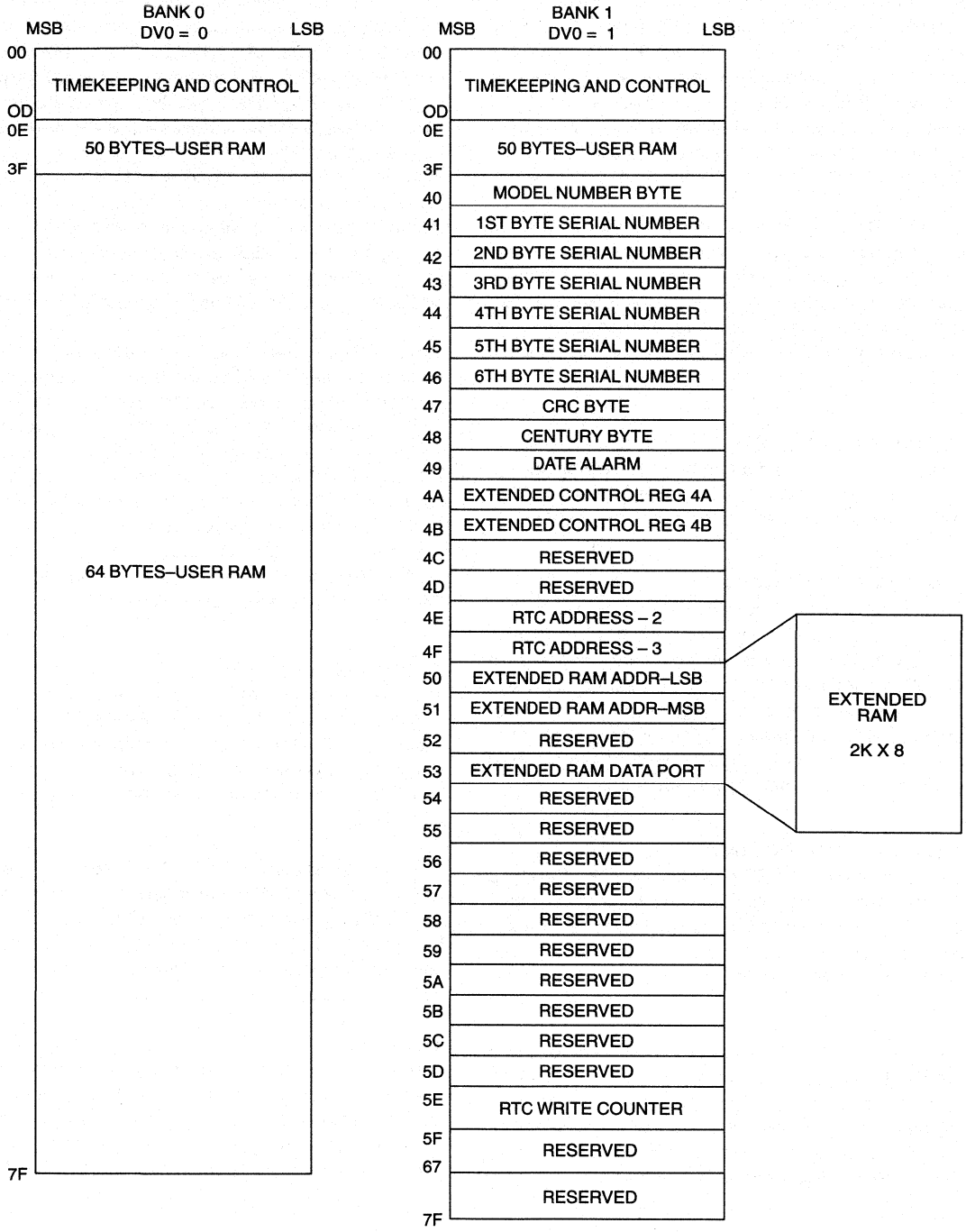
The extended functions provided by the DS17285/DS17287 that are new to the RAMified RTC family are accessed via a software controlled bank switching scheme, as illustrated in Figure 4. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS17285/DS17287 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers which provide control and status for the extended functions will be accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

1. 64–bit Silicon Serial Number
2. Century counter
3. Date Alarm
4. Auxiliary Battery Control/Status
5. Wake Up
6. Kickstart
7. RAM Clear Control/Status
8. 2K bytes Extended RAM Access

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and will return a 0 if read.

DS17285/DS17287 EXTENDED REGISTER BANK DEFINITION Figure 4



SILICON SERIAL NUMBER

A unique 64–bit lasered serial number is located in bank 1, registers 40h – 47h. This serial number is divided into three parts. The first byte in register 40h contains a model number to identify the device type and revision of the DS17285/DS17287. Registers 41h – 46h contain a unique binary number. Register 47h contains a CRC byte used to validate the data in registers 40h – 46h. All eight bytes of the serial number are read–only registers.

The DS17285/DS17287 is manufactured such that no two devices will contain an identical number in locations 41h – 47h. Blocks of numbers for these locations can be reserved by the customer. Contact Dallas Semiconductor for special ordering information for DS17285/DS17287's with reserved blocks of serial numbers.

CENTURY COUNTER

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

RTC WRITE COUNTER

An eight bit counter located in extended register bank 1, 5Eh, will count the number of times the RTC is written to. This counter will be incremented on the rising edge of the $\overline{WR}$ signal every time that the $\overline{CS}$ signal qualifies it. This counter is a read–only register and will roll–over after 256 RTC write pulses. This counter can be used to determine if and how many RTC writes have occurred since the last time this register was read.

2K X 8 EXTENDED RAM

The DS17285/DS17287 provides 2K x 8 of on–chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power–up, the RAM is taken out of write protect status by the internal power OK signal (POK) generated from the write protect circuitry.

The on–chip 2K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7 to AD0. Access to the SRAM is controlled by three on–chip latch registers. Two registers are used to hold the SRAM address, and the other register is used to hold read/write data. The SRAM address space is from 00h to 07FFh.

Access to the extended 2K x 8 RAM is controlled via three of the Dallas registers shown in Figure 4. The Dallas registers in bank 1 must first be selected by setting the DV0 bit in register A to a logic 1. The 11–bit address of the RAM location to be accessed must be loaded into the extended RAM address registers located at 50h and 51h. The least significant address byte should be written to location 50h, and the most significant 3–bits (right–justified) should be loaded in location 51h. Data in the addressed location may be read by performing a read operation from location 53h, or written to by performing a write operation to location 53h. Data in any addressed location may be read or written repeatedly without changing the address in location 50h and 51h.

To read or write consecutive extended RAM locations, a burst mode feature can be enabled to increment the extended RAM address. To enable the burst mode feature, set the BME bit in the extended control register 4Ah, to a logic 1. With burst mode enabled, write the extended RAM starting address location to registers 50h and 51h. Then read or write the extended RAM data from/to register 53h. The extended RAM address locations are automatically incremented on the rising edge of $\overline{RD}$ or $\overline{WR}$ only when register 53h is being accessed. Refer to the Burst Mode Timing Waveform.

AUXILIARY BATTERY

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS17285/DS17287 kickstart, wake up, and SQW output features in the absence of V_{CC}. This power source must be available in order to use these auxiliary features when no V_{CC} is applied to the device.

The Auxiliary Battery Enable (ABE; bank 1, register 04BH) bit in extended control register 4B is used to turn on and off the auxiliary battery for the above functions in the absence of V_{CC}. When set to a 1, V_{BAUX} battery power is enabled, and when cleared to 0, V_{BAUX} battery power is disabled to these functions.

In the DS17285/DS17287, this auxiliary battery may be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended external RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS17285 is to be backed-up using a single battery with the auxiliary fea-

tures enabled, then V_{BAUX} should be used and connected to V_{BAT}. If V_{BAUX} is not to be used, it should be grounded and ABE should be cleared to 0.

WAKE UP/KICKSTART

The DS17285/DS17287 incorporates a wake up feature which can power the system on at a pre-determined date through activation of the $\overline{PWR}$ output pin. In addition, the kickstart feature can allow the system to be powered up in response to a low going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin. As a result, system power may be applied upon such events as a key closure, or modem ring detect signal. In order to use either the wake up or the kickstart features, the DS17285/DS17287 must have an auxiliary battery connected to the V_{BAUX} pin and the oscillator must be running and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the $\overline{PWR}$ pin will not be driven low in response to a kickstart or wakeup condition, while in battery-backed mode.

The wake up feature is controlled through the Wake up Interrupt Enable bit in extended control register 4B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake up feature, clearing WIE to 0 disables it. Similarly, the kickstart feature is controlled through the Kickstart Interrupt Enable bit in extended control register 4B (KSE, bank 1, 04BH).

A wake up sequence will occur as follows: When wake up is enabled via WIE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar will monitor the current date for a match condition with the date alarm register (bank 1, register 049H). In conjunction with the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake up will occur at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm will occur regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the $\overline{PWR}$ pin will automatically be driven low. This output can be used to turn on the main system power supply which provides V_{CC} voltage to the DS17285/DS17287 as well as the other major components in the system. Also at this time, the Wake Up flag (WF, bank 1, register 04AH) will be set, indicating that a wake up condition has occurred.

A kickstart sequence will occur when kickstarting is enabled via KSE = 1. While the system is powered down, the $\overline{KS}$ input pin will be monitored for a low going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line will be pulled low, as it is for a wake up condition. Also at this time, the Kickstart Flag (KF, bank 1, register 04AH) will be set, indicating that a kickstart condition has occurred.

The timing associated with both the wake up and kickstarting sequences is illustrated in the Wake Up / Kickstart Timing Diagram in the Electrical Specifications section of this data sheet. The timing associated with these functions is divided into 5 intervals, labeled 1-5 on the diagram.

The occurrence of either a kickstart or wake up condition will cause the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS17285/DS17287 V_{CC} pin rises above the 3 volt power fail level before the power on timeout period (t_{POTO}) expires, then $\overline{PWR}$ will remain at the active low level. If V_{CC} does not rise above the 3 volt power fail voltage in this time, then the $\overline{PWR}$ output pin will be turned off and will return to its high impedance level. In this event, the $\overline{IRQ}$ pin will also remain tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power on sequence will remain set until cleared by software during a subsequent system power on.

If V_{CC} is applied within the timeout period, then the system power on sequence will continue as shown in intervals 2-5 in the timing diagram. During interval 2, $\overline{PWR}$ will remain active and $\overline{IRQ}$ will be driven to its active low level, indicating that either WF or KF was set in initiating the power on. In the diagram $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit will be automatically cleared to 0 in response to a successful power on. The $\overline{PWR}$ line will remain active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing zeroes to both of these control bits. As long as no other interrupt within the DS17285/DS17287 is pending, the $\overline{IRQ}$ line will be taken inactive once these bits are reset. Execution of the application software may proceed. During this time, both the wake up and kickstart functions may be used to

generate status and interrupts. WF will be set in response to a date, hours, minutes, and seconds match condition. KF will be set in response to a low going transition on $\overline{KS}$. If the associated interrupt enable bit is set (WIE and/or KSE) then the $\overline{IRQ}$ line will driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS17285/DS17287 may cause $\overline{IRQ}$ to be driven low. While system power is applied, the on chip logic will always attempt to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake up or kickstart.

The system may be powered down under software control by setting the PAB bit to a logic 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ}$ output pin will be placed in a high impedance state when V_{CC} goes below V_{PF}. If the system is to be again powered on in response to a wake up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and nonvolatile RAM is in effect and $\overline{IRQ}$ is tri-stated, and monitoring of wake up and kickstart takes place. If PRS=1, $\overline{PWR}$ stays active, otherwise if PRS=0 $\overline{PWR}$ is tri–stated.

RAM CLEAR

The DS17285/DS17287 provides a RAM clear function for the 114 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V_{CC} pin.

The RAM clear function is enabled or disabled via the RAM Clear Enable bit (RCE; bank 1, register 04BH). When this bit is set to a logic 1, the 114 bytes of user RAM will be cleared (all bits set to 1) when an active low transition is sensed on the $\overline{RCLR}$ pin. This action will have no effect on either the clock/calendar settings or upon the contents of the extended RAM. The RAM clear Flag (RF, bank 1, register 04AH) will be set when the RAM clear operation has been completed. If V_{CC} is present at the time of the RAM clear and RIE=1, the $\overline{IRQ}$ line will also be driven low upon completion. The interrupt condition can be cleared by writing a zero to the RF bit. The $\overline{IRQ}$ line will then return to its inactive high level provided there are no other pending interrupts. Once the $\overline{RCLR}$ pin is activated, all read/write accesses are locked out for a minimum recover time, specified as t_{REC} in the Electrical Characteristics section.

When RCE is cleared to zero, the RAM clear function is disabled. The state of the $\overline{RCLR}$ pin will have no effect on the contents of the user RAM, and transitions on the $\overline{RCLR}$ pin have no effect on RF.

EXTENDED CONTROL REGISTERS

Two extended control registers are provided to supply controls and status information for the extended features offered by the DS17285/DS17287. These are designated as extended control registers 4A and 4B and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows.

EXTENDED CONTROL REGISTER 4A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	BME	*	PAB	RF	WF	KF

VRT2 - This status bit gives the condition of the auxiliary battery. It is set to a logic 1 condition when the external lithium battery is connected to the V_{BAUX}. If this bit is read as a logic 0, the external battery should be replaced.

INCR - Increment in Progress status bit. This bit is set to a 1 when an increment to the time/date registers is in progress and the alarm checks are being made. INCR will be set to a 1 at 122 µs before the update cycle starts and will be cleared to 0 at the end of each update cycle.

BME – Burst Mode Enable. The burst mode enable bit allows the extended user RAM address registers to automatically increment for consecutive reads and writes. When BME is set to a logic one, the automatic incrementing will be enabled and when BME is set to a logic zero, the automatic incrementing will be disabled.

PAB - Power Active Bar control bit. When this bit is 0, the $\overline{PWR}$ pin is in the active low state. When this bit is 1, the $\overline{PWR}$ pin is in the high impedance state. This bit can be written to a logic 1 or 0 by the user. If either WF AND WIE = 1 OR KF AND KSE = 1, the PAB bit will be cleared to 0.

RF - Ram Clear Flag. This bit will be set to a logic 1 when a high to low transition occurs on the $\overline{RCLR}$ input if RCE=1. The RF bit is cleared by writing it to a logic 0. This bit can also be written to a logic 1 to force an interrupt condition.

WF - Wake up Alarm Flag - This bit is set to 1 when a wake up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

KF - Kickstart Flag - This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

EXTENDED CONTROL REGISTER 4B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32K	CS	RCE	PRS	RIE	WIE	KSE

ABE - Auxiliary Battery Enable. This bit when written to a logic 1 will enable the V_{BAUX} pin for extended functions.

E32K - Enable 32.768 KHz output. This bit when written to a logic 1 will enable the 32.768 KHz oscillator frequency to be output on the SQW pin. E32K is set to a one when V_{CC} is powered up.

CS – Crystal Select Bit. When CS is set to a 0, the oscillator is configured for operation with a crystal that has a 6 pF specified load capacitance. When CS=1, the oscillator is configured for a 12.5 pF crystal.

RCE - RAM Clear Enable bit. When set to a 1, this bit enables a low level on $\overline{RCLR}$ to clear all 114 bytes of user RAM. When RCE = 0, $\overline{RCLR}$ and the RAM clear function are disabled.

PRS – PAB Reset Select Bit. When set to a 0 the $\overline{PWR}$ pin will be set hi–Z when the DS17285 goes into power fail. When set to a 1, the $\overline{PWR}$ pin will remain active upon entering power fail.

RIE - Ram Clear Interrupt Enable. When RIE is set to a 1, the $\overline{IRQ}$ pin will be driven low when a RAM clear function is completed.

WIE - Wake Up Alarm Interrupt Enable. When V_{CC} voltage is absent and WIE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a wake up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If WIE is set while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to WF being set to 1. When WIE is cleared to a 0, the WF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

KSE - Kickstart Interrupt Enable. When V_{CC} voltage is absent and KSE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If KSE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to KF being set to 1. When KSE is cleared to a 0, the KF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

* Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no effect on operation.

SYSTEM MAINTENANCE INTERRUPT (SMI) RECOVERY STACK

An SMI recovery register stack is located in the extended register bank, locations 4Eh and 4Fh. This register stack, shown below, can be used by the BIOS to recover from an SMI occurring during an RTC read or write.

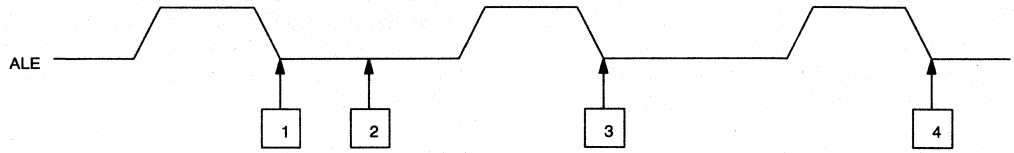
	RTC ADDRESS
	RTC ADDRESS – 1
4Eh	RTC ADDRESS – 2
4Fh	RTC ADDRESS – 3

SMI RECOVERY STACK

7	6	5	4	3	2	1	0
DV0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

REGISTER BIT DEFINITION

The RTC address is latched on the falling edge of the ALE signal. Each time an RTC address is latched, the register address stack is pushed. The stack is only four registers deep, holding the three previous RTC addresses in addition to the current RTC address being accessed. The following waveform illustrates how the BIOS could recover the RTC address when an SMI occurs.



1. The RTC address is latched.
2. An SMI is generated before an RTC read or write occurs.
3. RTC address 0Ah is latched and the address from "1" is pushed to the "RTC Address – 1" stack location. This step is necessary to change the bank select bit, DV0=1.
4. RTC address 4Eh is latched and the address from "1" is pushed to location 4Eh, "RTC Address – 2" while 0Ah is pushed to the "RTC Address – 1" location. The data in this register, 4Eh, is the RTC address lost due to the SMI.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature DS17285	–55°C to +125°C
Storage Temperature DS17287	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage 5 Volt Operation	V_{CC}	4.5	5.0	5.5	V	1
Power Supply Voltage 3 Volt Operation	V_{CC}	2.7	3.0	3.3	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		0.6	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	1
Auxiliary Battery Voltage	V_{BAUX}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		25	50	mA	2, 3
CMOS Standby Current ($\overline{CS}$=V_{CC}-0.2V)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
Output Leakage Current	I_{OL}	–1		+1	µA	6
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Power Fail Trip Point	V_{PF}	4.25	4.37	4.5	V	4
Battery Switch Voltage	V_{SW}		V_{BAT}, V_{BAUX}		V	9

DC ELECTRICAL CHARACTERISTICS (cont'd)

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Leakage OSC ON	I_{BAT1}		0.50	1.5	µA	12
Battery Leakage OSC OFF	I_{BAT2}		0.050	1.0	µA	12
I/O Leakage	I_{LO}	–1		+1	µA	5
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			10.0	mA	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=3.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		15	30	mA	2, 3
CMOS Standby Current ($\overline{CS}$=V_{CC}-0.2)	I_{CC2}		0.5	2	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
Output Leakage Current	I_{OL}	–1		+1	µA	6
Output Logic 1 Voltage @ 0.4 mA	V_{OH}	2.4			V	
Output Logic 0 Voltage @ 0.8 mA	V_{OL}			0.4	V	
Power Fail Trip Point	V_{PF}	2.5	2.6	2.7	V	4
Battery Leakage OSC ON	I_{BAT1}		0.50	1.5	µA	12
Battery Leakage OSC OFF	I_{BAT2}		0.050	1.0	µA	12
I/O Leakage	I_{LO}	–1		+1	µA	5
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			4	mA	1

RTC AC TIMING CHARACTERISTICS

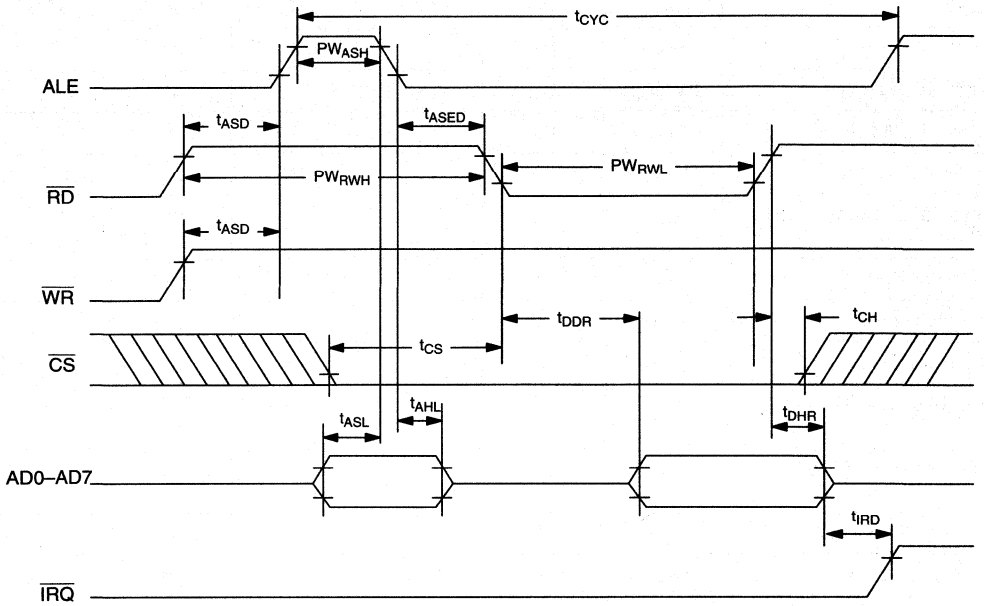
($0°C$ to $70°C$; $V_{CC} = 3.0V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	915		DC	ns	
Pulse Width, $\overline{RD}/\overline{WR}$ Low	PW_{RWL}	375			ns	
Pulse Width, $\overline{RD}/\overline{WR}$ High	PW_{RWH}	450			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	75			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		120	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	90			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	30			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	30			ns	
Pulse Width ALE High	PW_{ASH}	180			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	120			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		370	ns	7
Data Setup Time	t_{DSW}	180			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

AC TEST CONDITIONS

Output Load: 50 pF
Input Pulse Levels: 0–3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS17285/DS17287 BUS TIMING FOR READ CYCLE TO RTC

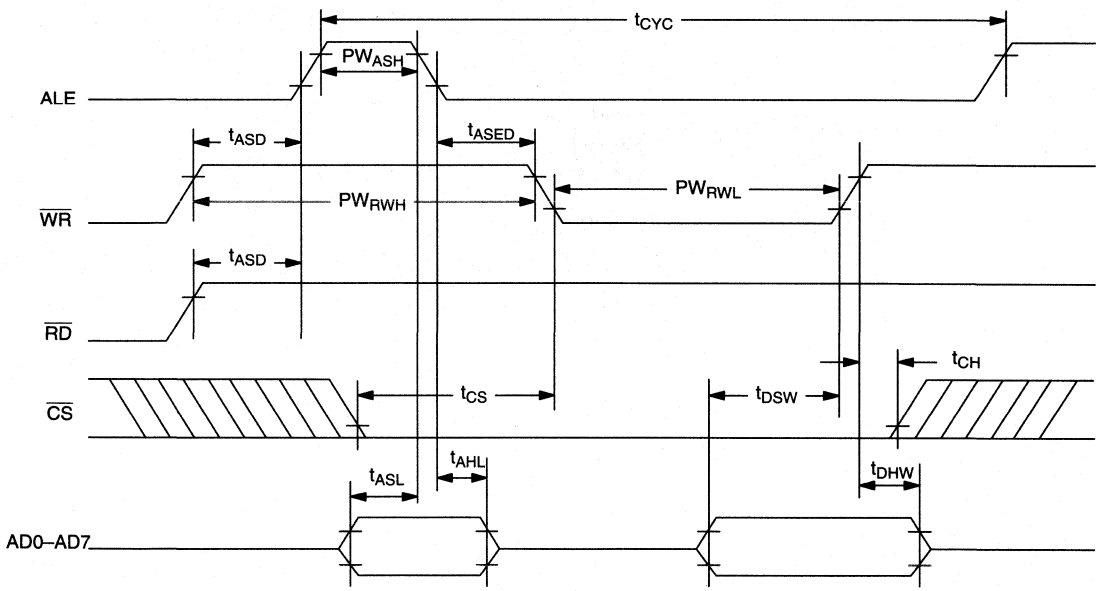


RTC AC TIMING CHARACTERISTICS

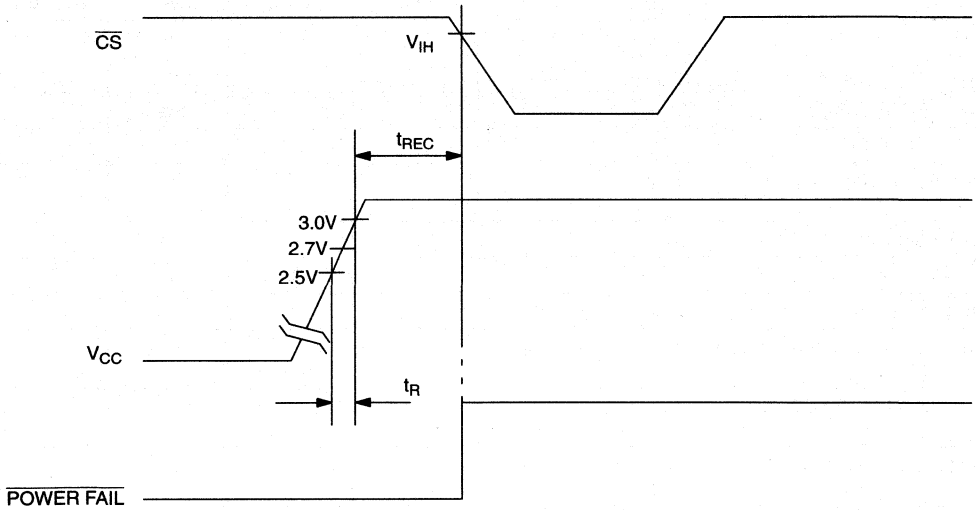
($0°C$ to $70°C$; $V_{CC} = 5.0V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}/\overline{WR}$ Low	PW_{RWL}	125			ns	
Pulse Width, $\overline{RD}/\overline{WR}$ High	PW_{RWH}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	7
Data Setup Time	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

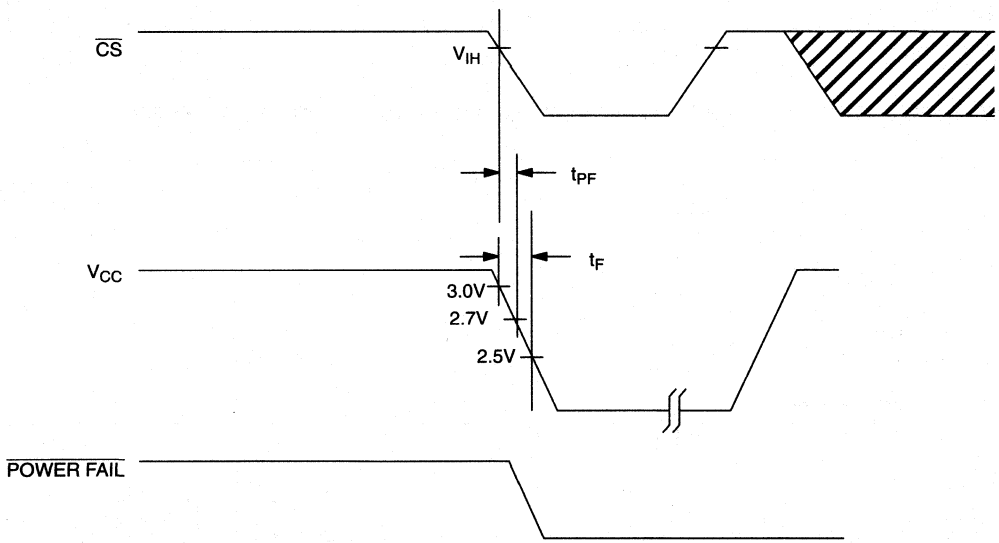
DS17285/DS17287 BUS TIMING FOR WRITE CYCLE TO RTC AND RTC REGISTERS



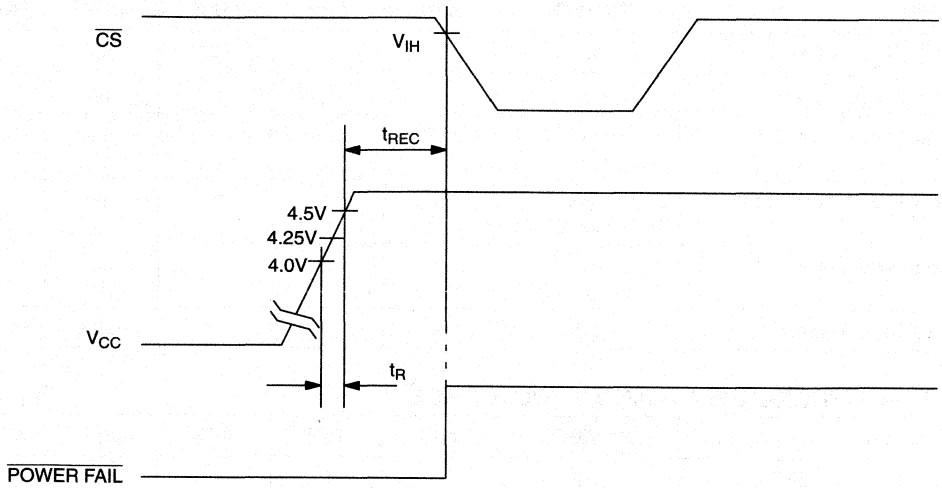
POWER–UP CONDITION 3 VOLT DEVICE



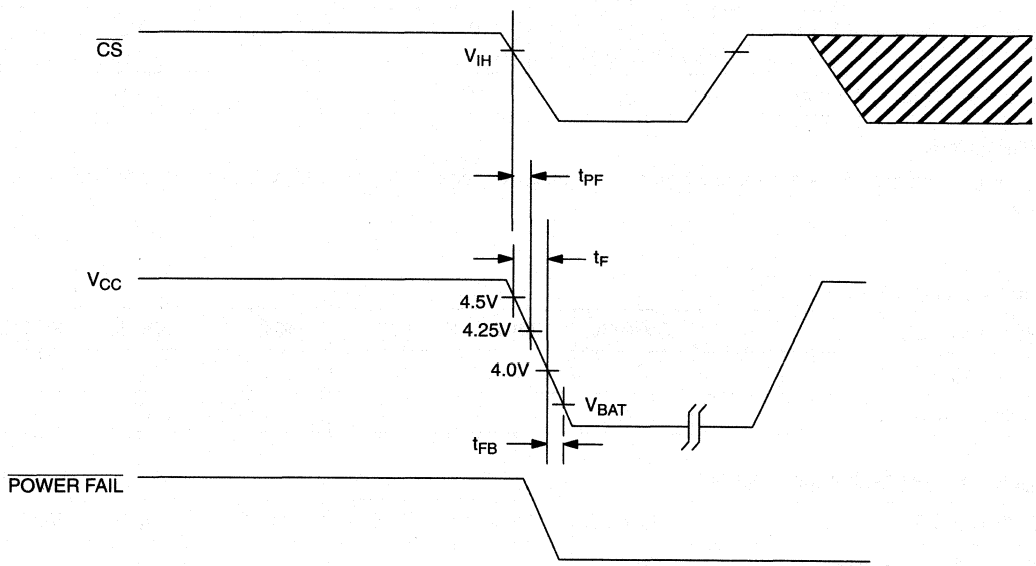
POWER–DOWN CONDITION 3 VOLT DEVICE



POWER–UP CONDITION 5.0 VOLT DEVICE



POWER–DOWN CONDITION 5.0 VOLT DEVICE



POWER-UP POWER-DOWN TIMING 5 VOLT DEVICE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	10, 11

POWER-UP POWER-DOWN TIMING 3 VOLT DEVICE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $2.5 \le V_{CC} \le 3.0V$	300			µs	
V_{CC} Slew Rate Power Up	t_R $3.0V \ge V_{CC} \ge 2.5V$	0			µs	
Expected Data Retention	t_{DR}	10			years	10, 11

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

(t_A = 25°C)

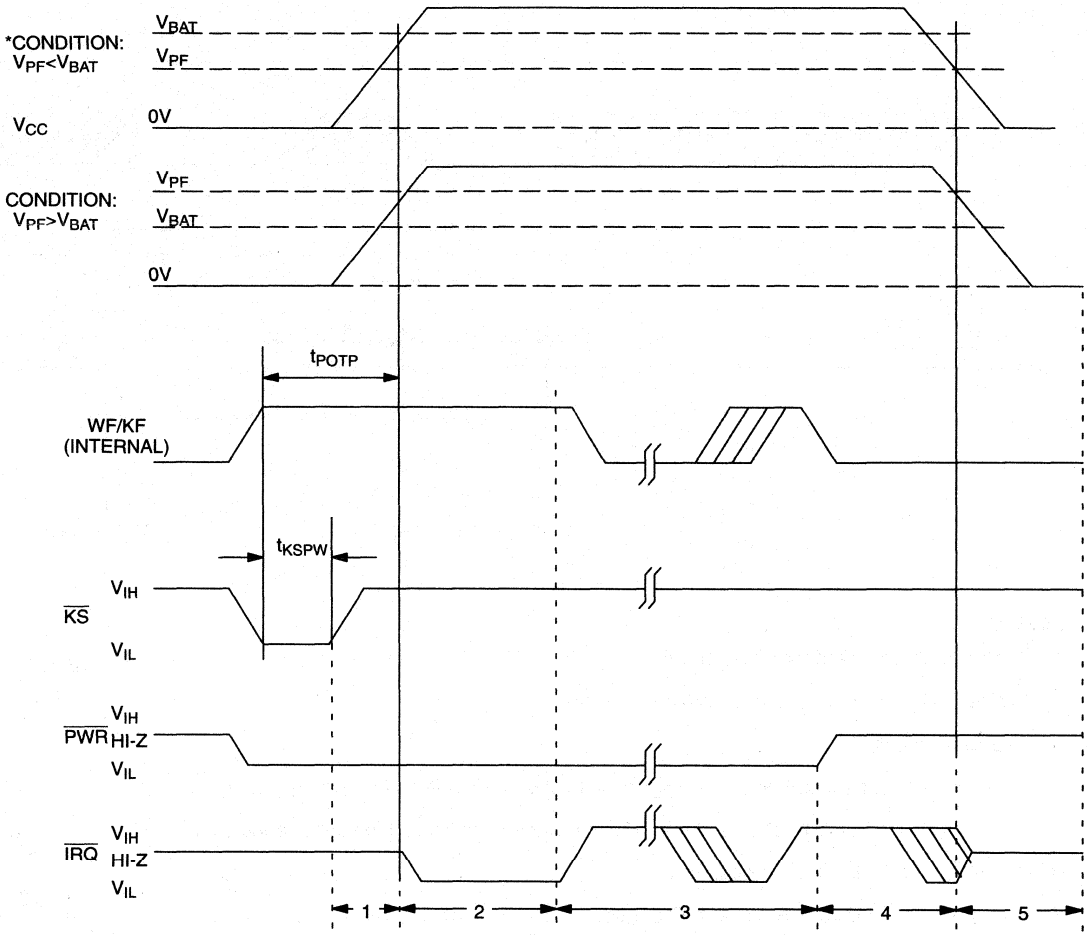
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

WAKE UP/KICKSTART TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t_{KSPW}	2			µs	
Wake up/Kickstart Power On Timeout	t_{POTO}	2			seconds	8

WAKE UP/KICKSTART TIMING

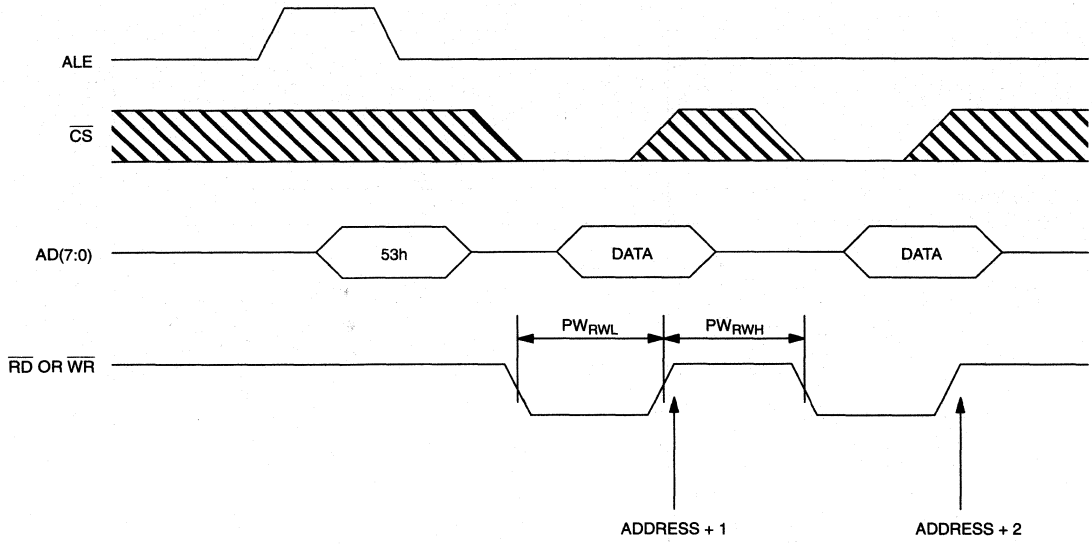


NOTE:

Time intervals shown above are referenced in Wake up/Kickstart section.

* This condition can occur with the 3 volt device.

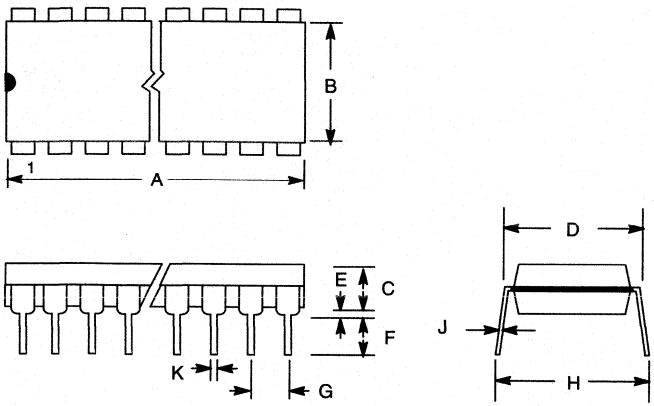
BURST MODE TIMING WAVEFORM



NOTES:

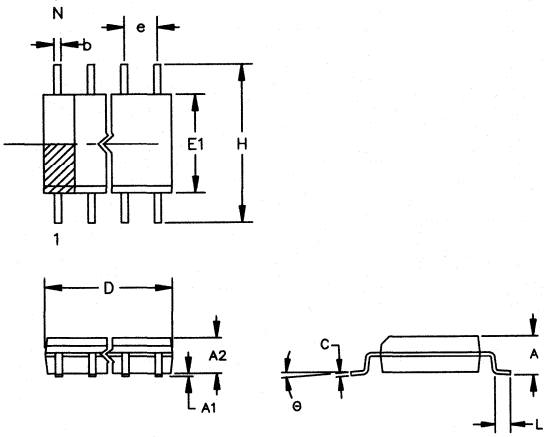
1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Write protection trip point occurs during power fail prior to switchover from V_{CC} to V_{BAT}.
5. Applies to the AD0–AD7 pins, and the SQW pin when each is in a high impedance state.
6. The $\overline{IRQ}$ and $\overline{PWR}$ pins are open drain.
7. Measured with a load of 50 pF + 1 TTL gate.
8. Wakeup kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.
9. V_{SW} is determined by the larger of V_{BAT} and V_{BAUX}.
10. The DS17287 will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
11. t_{DR} is the amount of time that the internal battery can power the internal oscillator and internal registers of the DS17287.
12. I_{BAT1} and I_{BAT2} are measured at V_{BAT} = 3.5V.

DS17285 24–PIN DIP



PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	1.245 31.62	1.270 32.25
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.380	0.050 1.27
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.625 15.88	0.675 17.15
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

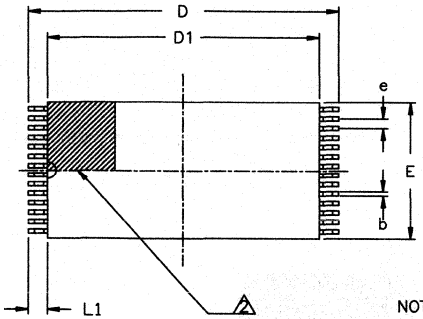
DS17285 24–PIN SOIC

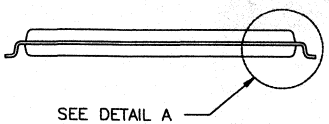


The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33
D IN. MM	0.598 15.19	0.612 15.54
e IN. MM	.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02
Θ	0°	8°

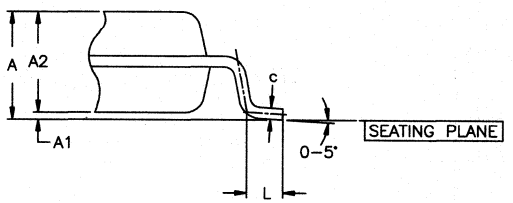
DS17285 28–PIN TSOP





NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT ONE HALF OF ITS AREA MUST BE LOCATED WITHIN THE ZONE INDICATED.

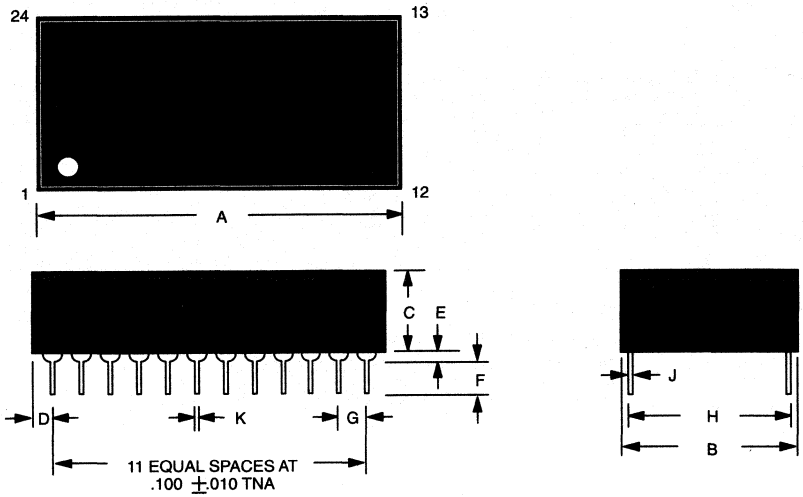


DETAIL A

PKG	28-PIN	
DIM	MIN	MAX
A	–	1.20
A1	0.05	–
A2	0.91	1.02
b	0.18	0.27
c	0.15	0.20
D	13.20	13.60
D1	11.70	11.90
E	7.90	8.10
e	0.55 BSC	
L	0.30	0.70
L1	0.80 BSC	

56–G5003–000

DS17287 REAL TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.720 18.29	0.740 18.80
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

DS17485/DS17487
3 Volt/5 Volt Real Time Clock

3

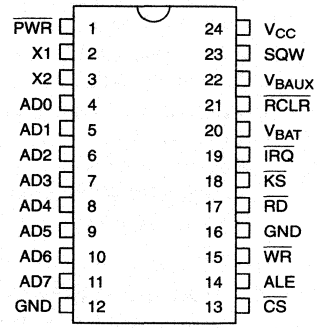
FEATURES
Incorporates industry standard DS1287 PC clock plus enhanced features:

- +3 or +5 volt operation
- SMI recovery stack
- 64–bit silicon serial number
- Power control circuitry supports system power on from date/time alarm or key closure
- 32 KHz output on power–up
- Crystal select bit allows RTC to operate with 6 pF or 12.5 pF crystal
- 114 bytes user NVRAM
- Auxiliary battery input
- 4K bytes additional NVRAM
- RAM clear input
- Century register
- Date alarm register
- Compatible with existing BIOS for original DS1287 functions
- Available as chip (DS17485) or standalone module with embedded battery and crystal (DS17487)

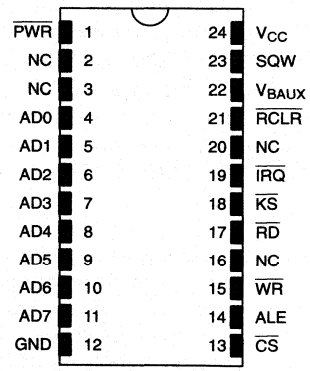
ORDERING INFORMATION

PART #	DESCRIPTION
DS17485–X	RTC Chip; 24–pin DIP
DS17485S–X	RTC Chip; 24–pin SOIC
DS17485E–X	RTC Chip; 28–pin TSOP
DS17487–X	RTC Module; 24–pin DIP
–3	+3 volt device
–5	+5 volt device

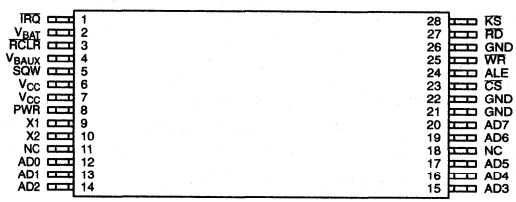
PIN ASSIGNMENT



DS17485 24–PIN DIP
DS17485S 24–PIN SOIC



DS17487 24–PIN ENCAPSULATED PACKAGE



DS17485E 28–PIN TSOP

PIN DESCRIPTION

X1	–	Crystal Input
X2	–	Crystal Output
$\overline{RCLR}$	–	RAM Clear Input
AD0-AD7	–	Mux'ed Address/Data Bus
$\overline{PWR}$	–	Power–on Interrupt Output (open drain)
$\overline{KS}$	–	Kickstart Input
$\overline{CS}$	–	RTC Chip Select Input
ALE	–	RTC Address Strobe
$\overline{WR}$	–	RTC Write Data Strobe
$\overline{RD}$	–	RTC Read Data Strobe
$\overline{IRQ}$	–	Interrupt Request Output (open drain)
SQW	–	Square Wave Output
V_{CC}	–	+3 or +5 Volt Main Supply
GND	–	Ground
V_{BAT}	–	Battery + Supply
V_{BAUX}	–	Auxiliary Battery Supply
NC	–	No Connection

DESCRIPTION

The DS17485/DS17487 is a real time clock (RTC) designed as a successor to the industry standard DS1285, DS1385, DS1485, DS1585, and DS1685 PC real time clocks. This device provides the industry standard DS1285 clock function with either +3.0 or +5.0 volt operation. The DS17485 also incorporates a number of enhanced features including a silicon serial number, power on/off control circuitry, 114 bytes of user NVSRAM plus 4K bytes of additional NVRAM, and 32.768 KHz output for sustaining power management activities.

The DS17485/DS17487 power control circuitry allows the system to be powered on via an external stimulus, such as a keyboard or by a time and date (wake up) alarm. The $\overline{PWR}$ output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS17485 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time–of–day and memory status in the absence of power. The DS17487 incorporates the DS17485 chip, a 32.768 KHz crystal, and a lithium battery in a complete, self–contained timekeeping module. The entire unit is fully tested at Dallas Semiconductor such that a minimum of 10 years of timekeeping and data retention in the absence of V_{CC} is guaranteed.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS17485/DS17487. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +3 volt or +5 volt input.

SQW (Square Wave Output) - The SQW pin will provide a 32 KHz square wave output, t_{REC}, after a power–up condition has been detected. This condition sets the following bits, enabling the 32 KHz output; DV1=1, and E32K=1. A square wave will be output on this pin if either SQWE=1 or E32K=1. If E32K=1, then 32 KHz will be output regardless of the other control bits. If E32K=0, then the output frequency is dependent on the control bits in register A. The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in register B or the E32K bit in extended register 4Bh. A 32 KHz SQW signal is output when the Enable 32 KHz (E32K) bit in extended register 4Bh is a logic one, and V_{CC} is above V_{PF}. A 32 KHz square wave is also available when V_{CC} is less than V_{PF} if E32K=1, ABE=1, and voltage is applied to the V_{BAUX} pin.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS17485 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, at which time the DS17485/DS17487 latches the address. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ pulse. In a read cycle the DS17485/DS17487 outputs 8 bits of data during the latter portion of the $\overline{RD}$ pulse. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high. The address/data bus also serves as a bidirectional data path for the external extended RAM.

ALE (RTC Address Strobe Input; active high) - A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS17485/DS17487.

$\overline{RD}$ (RTC Read Input; active low) - $\overline{RD}$ identifies the time period when the DS17485/DS17487 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

$\overline{WR}$ (RTC Write Input; active low) -The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed register.

$\overline{CS}$ (RTC Chip Select Input; active low) - The Chip Select signal must be asserted low during a bus cycle for DS17485/DS17487 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place with ALE asserted but without asserting $\overline{CS}$ will latch addresses. However, no data transfer will occur.

$\overline{IRQ}$ (Interrupt Request Output; open drain, active low) - The $\overline{IRQ}$ pin is an active low output of the DS17485/DS17487 that can be tied to the interrupt input of a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application software must clear all enabled flag bits contributing to $\overline{IRQ}$'s active state.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ pin is an open drain output and requires an external pull-up resistor.

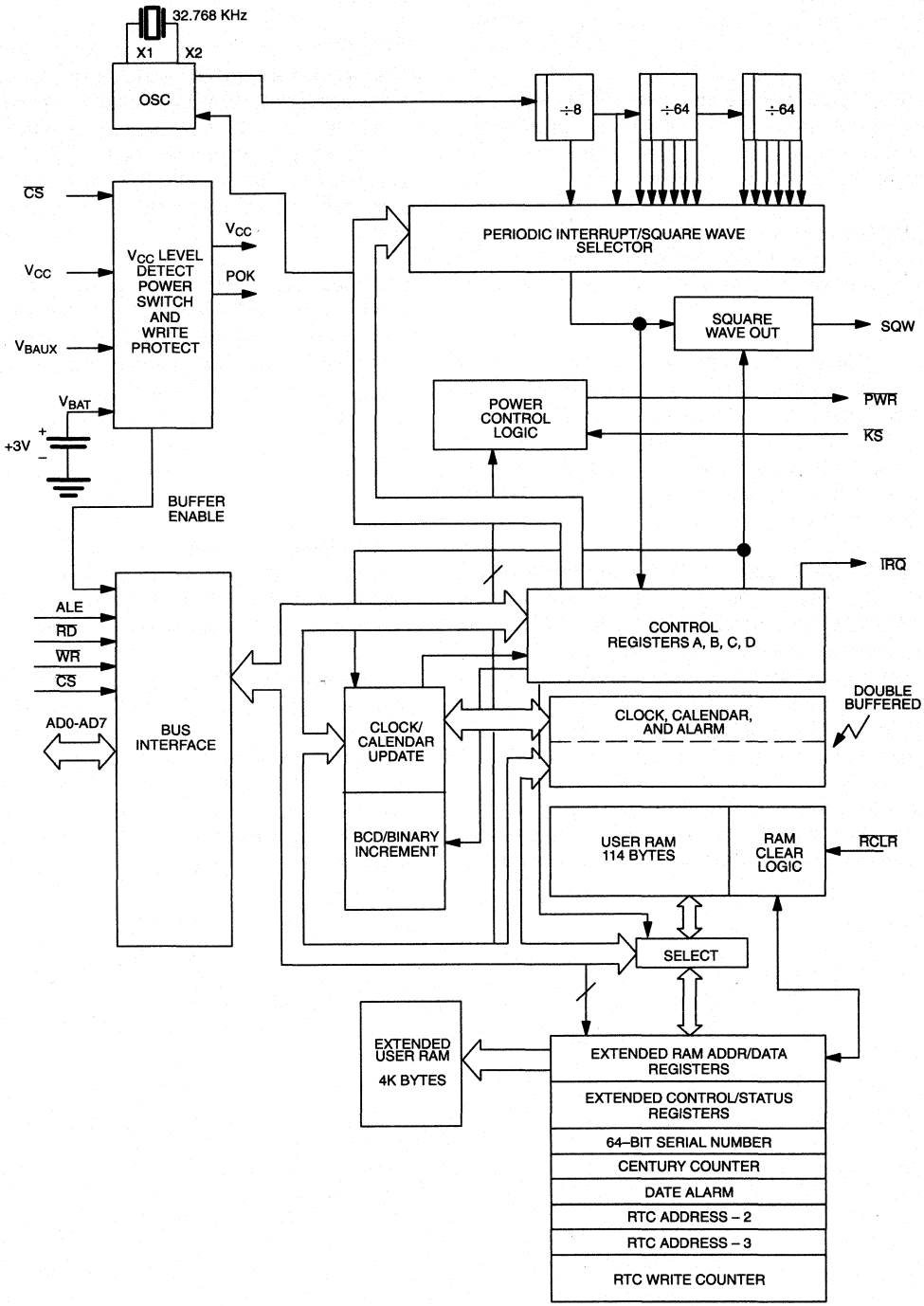
$\overline{PWR}$ (Power On Output; open drain, active low) - The $\overline{PWR}$ pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the DS17485/DS17487, $\overline{PWR}$ may be automatically activated from a Kickstart input via the $\overline{KS}$ pin or from a Wake Up interrupt. Once the system is powered on, the state of $\overline{PWR}$ can be controlled via bits in the Dallas registers.

$\overline{KS}$ (Kickstart Input; active low) - When V_{CC} is removed from the DS17485/DS17487, the system can be powered on in response to an active low transition on the $\overline{KS}$ pin, as might be generated from a key closure. V_{BAUX} must be present and Auxiliary Battery Enable bit (ABE) must be set to 1 if the kickstart function is used, and the $\overline{KS}$ pin must be pulled up to the V_{BAUX} supply. While V_{CC} is applied, the $\overline{KS}$ pin can be used as an interrupt input.

$\overline{RCLR}$ (RAM Clear Input; active low) - If enabled by software, taking $\overline{RCLR}$ low will result in the clearing of the 114 bytes of user RAM. When enabled, $\overline{RCLR}$ can be activated whether or not V_{CC} is present.

V_{BAUX} - Auxiliary battery input required for kickstart and wake up features. This input also supports clock/calendar and user RAM if V_{BAT} is at lower voltage or is not present. A standard +3 volt lithium cell or other energy source can be used. Battery voltage must be held between +2.5 and +3.7 volts for proper operation. If V_{BAUX} is not going to be used it should be grounded and auxiliary battery enable bit bank 1, register 4BH, should=0.

DS17485/DS17487 BLOCK DIAGRAM Figure 1



DS17485 ONLY

X1, X2 - Connections for a standard 32.768 KHz quartz crystal. For greatest accuracy, the DS17485 must be used with a crystal that has a specified load capacitance of either 6 pF or 12.5 pF. The Crystal Select (CS) bit in Extended Control Register 4B is used to select operation with a 6 pF or 12.5 pF crystal. The crystal is attached directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area.

For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks". The DS17485 can also be driven by an external 32.768 KHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

V_{BAT} - Battery input for any standard 3 Volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation.

POWER–DOWN/POWER–UP CONSIDERATIONS

The real-time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS17485/DS17487 and reaches a level of greater than V_{PF} (power fail trip point), the device becomes accessible after t_{REC}, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied.

The DS17485/DS17487 is available in either a 3 volt or a 5 volt device.

The 5 volt device is fully accessible and data can be written and read only when V_{CC} is greater than 4.5 volts. When V_{CC} is below 4.5 volts, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below the greater of V_{BAT} and V_{BAUX}, the RAM and timekeeper are switched over to a lithium battery connected either to the V_{BAT} pin or V_{BAUX} pin.

The 3 volt device is fully accessible and data can be written or read only when V_{CC} is greater than 2.7 volts. When V_{CC} falls below V_{PF}, access to the device is inhibited. If V_{PF} is less than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply (the greater of V_{BAT} and V_{BAUX}) when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply when V_{CC} drops below the larger of V_{BAT} and V_{BAUX}.

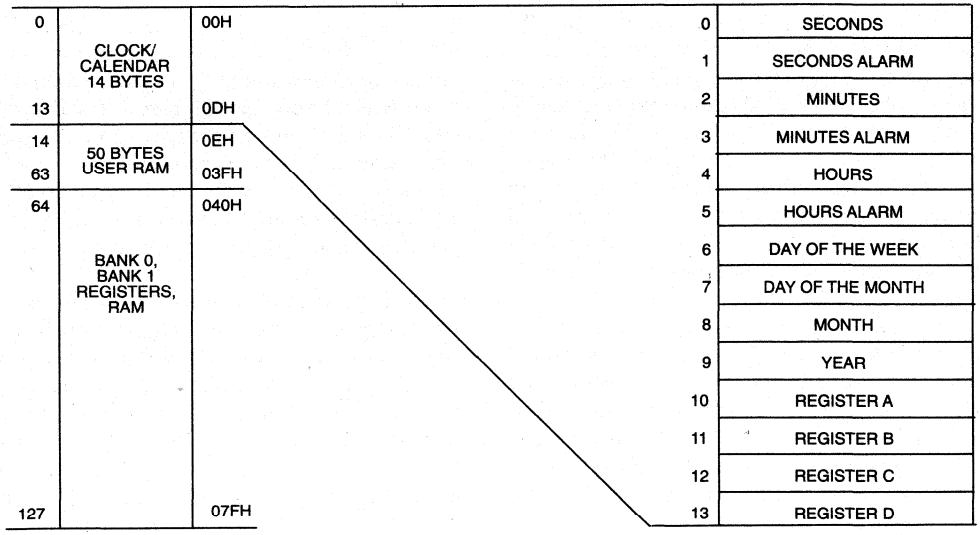
When V_{CC} falls below V_{PF}, the chip is write-protected. With the possible exception of the $\overline{KS}$, $\overline{PWR}$, $\overline{RCLR}$ and SQW pins, all inputs are ignored and all outputs are in a high impedance state.

RTC ADDRESS MAP

The address map for the RTC registers of the DS17485/DS17487 is shown in Figure 2. The address map consists of the 14 clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and four bytes are used for control and status. All registers can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

DS17485 REAL TIME CLOCK ADDRESS MAP Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching will be explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The four alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second use condition is to insert a "don't care" state in one or more of the four alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second. The three alarm bytes may be used in conjunction with the date alarm as described in the Wakeup/Kickstart section. The century counter will be discussed later in this text.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
00H	Seconds	0-59	00-3B	00-59
01H	Seconds Alarm	0-59	00-3B	00-59
02H	Minutes	0-59	00-3B	00-59
03H	Minutes Alarm	0-59	00-3B	00-59
04H	Hours 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours 24-Hour Mode	0-23	00-17	00-23
05H	Hours Alarm 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92 PM
	Hours Alarm 24-hr. Mode	0-23	00-17	00-23
06H	Day of Week Sunday=1	1-7	01-07	01-07
07H	Date of Month	1-31	01-1F	01-31
08H	Month	1-12	01-0C	01-12
09H	Year	0-99	00-63	00-99
BANK 1, 48H	Century	0-99	00-63	00-99
BANK 1, 49H	Date Alarm	1-31	01-1F	01-31

CONTROL REGISTERS

The four control registers; A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

NONVOLATILE RAM - RTC

The general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS17485/DS17487. They can be used by the application program as nonvolatile memory and are fully available during the update cycle.

The user RAM is divided into two separate memory banks. When the bank 0 is selected, the 14 real time clock registers and 114 bytes of user RAM are accessible. When bank 1 is selected, an additional 4K bytes of user RAM are accessible through the extended RAM address and data registers.

INTERRUPT CONTROL

The DS17485/DS17487 includes six separate, fully automatic sources of interrupt for a processor:

1. Alarm interrupt
2. Periodic interrupt
3. Update-ended interrupt
4. Wake up interrupt
5. Kickstart interrupt
6. RAM clear interrupt

The conditions which generate each of these independent interrupt conditions are described in greater detail elsewhere in this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are a total of six bits including three bits in Register B and three bits in Extended Register 4B which enable the interrupts. The extended register locations are described later. Writing a logic 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ will immediately be set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As

a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register 4A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register 4B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits which are set remain stable throughout the read cycle. All bits which were set are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register 4A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the $\overline{IRQ}$ line will be driven low when an interrupt flag bit is set and its corresponding enable bit is also set. $\overline{IRQ}$ will be held low as long as at least one of the six possible interrupt sources has it s flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS17485/DS17487 initiated an interrupt is accomplished by reading Register C and finding IRQF=1. IRQF will remain set until all enabled interrupt flag bits are cleared to 0.

SQUARE WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768 KHz crystal tied to X1 and X2. The square wave output is enabled and disabled via the SQWE bit in Register B or the E32K bit in extended register 4Bh. If the square wave is enabled (SQWE=1 or E32K=1), then the output frequency will be determined by the settings of the E32K bit in Extended Register 4Bh and by the RS3-0 bits in Register A. If E32K=1, then a 32.768 KHz square wave will be output on the SQW pin regardless of the settings of RS3-0 and SQWE.

If E32K = 0, then the square wave output frequency is determined by the RS3-0 bits. These bits control a 1-of-15 decoder which selects one of thirteen taps that divide the 32.768 KHz frequency. The RS3-0 bits establish the SQW output frequency as shown in Table 2. In addition, RS3-0 bits control the periodic interrupt selection as described below.

If E32K=1, and the Auxiliary Battery Enable bit (ABE, bank 1; register 04BH) is enabled, and voltage is applied to V_{BAUX} then the 32 KHz square wave output signal will be output on the SQW pin in the absence of V_{CC}. This facility is provided to clock external power management circuitry. If any of the above requirements are not met, no square wave output signal will be generated on the SQW pin in the absence of V_{CC}.

A pattern of 01X in the DV2, DV1, and DV0, bits respectively, will turn the oscillator on and enable the countdown chain. Note that this is different than the DS1287, which required a pattern of 010 in these bits. DV0 is now a "don't care" because it is used for selection between register banks 0 and 1.

A pattern of 11X will turn the oscillator on, but the oscillator's countdown chain will be held in reset, as it was in the DS1287. Any other bit combination for DV2 and DV1 will keep the oscillator off.

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3-0 bits in Register A which select the square wave frequency (see Table 2). Changing the bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE and E32K bits control the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The Serialized RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, alarm and elapsed time byte is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows the time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all alarm locations.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

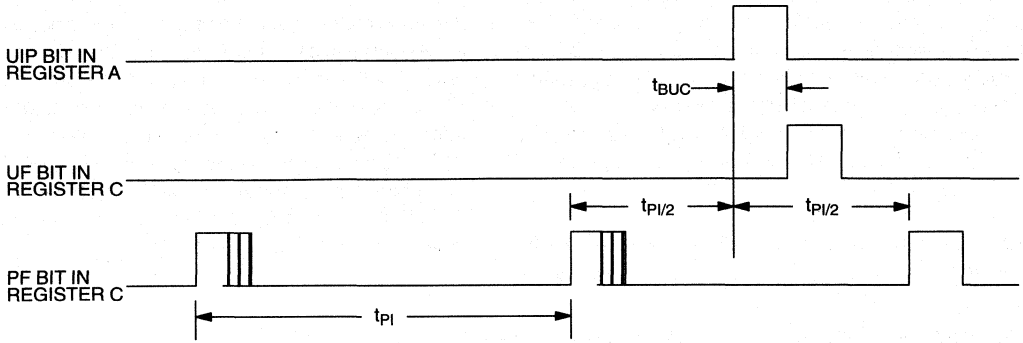
PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

EXT. REG. B	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
E32K	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625 ms	256 Hz
0	0	0	1	0	7.8125 ms	128 Hz
0	0	0	1	1	122.070 µs	8.192 KHz
0	0	1	0	0	244.141 µs	4.096 KHz
0	0	1	0	1	488.281 µs	2.048 KHz
0	0	1	1	0	976.5625 µs	1.024 KHz
0	0	1	1	1	1.953125 ms	512 Hz
0	1	0	0	0	3.90625 ms	256 Hz
0	1	0	0	1	7.8125 ms	128 Hz
0	1	0	1	0	15.625 ms	64 Hz
0	1	0	1	1	31.25 ms	32 Hz
0	1	1	0	0	62.5 ms	16 Hz
0	1	1	0	1	125 ms	8 Hz
0	1	1	1	0	250 ms	4 Hz
0	1	1	1	1	500 ms	2 Hz
1	X	X	X	X	*	32.768 KHz

*RS3-RS0 determine periodic interrupt rates as listed for E32K=0.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within (t_{PI} / 2+t_{BUC}) to ensure that data is not read during the update cycle.

UPDATE–ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1
t_{BUC} = DELAY TIME BEFORE UPDATE CYCLE = 244 µs

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These bits are defined as follows:

DV2 = Countdown Chain
- 1 - resets countdown chain only if DV1=1
- 0 - countdown chain enabled

DV1 = Oscillator Enable
- 0 - oscillator off
- 1 - oscillator on, V_{CC} power–up state

DV0 = Bank Select
- 0 - original bank
- 1 - extended registers

A pattern of 01X is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 01X is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

Enable the interrupt with the PIE bit;

Enable the SQW output pin with the SQWE or E32K bits;

Enable both at the same time and the same rate; or

Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS17485/DS17487.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS17485/DS17487 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS17485/DS17487 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one and E32K=0, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to zero and E32K=0, the SQW pin is held low. SQWE is a read/write bit. SQWE is set to a one when V_{CC} is powered up.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 WF = WIE = 1
AF = AIE = 1 KF = KSE = 1
UF = UIE = 1 RF = RIE = 1

i.e., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE) + (WF • WIE) + (KF • KSE) + (RF • RIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 3 THROUGH BIT 0 - These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time bit is a read only status bit. When VRT = 0, the RTC and RAM data are questionable and indicates that the lithium energy source has been exhausted and should be replaced. This bit indicates the status of the V_{BAT} and V_{BAUX} inputs.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

EXTENDED FUNCTIONS

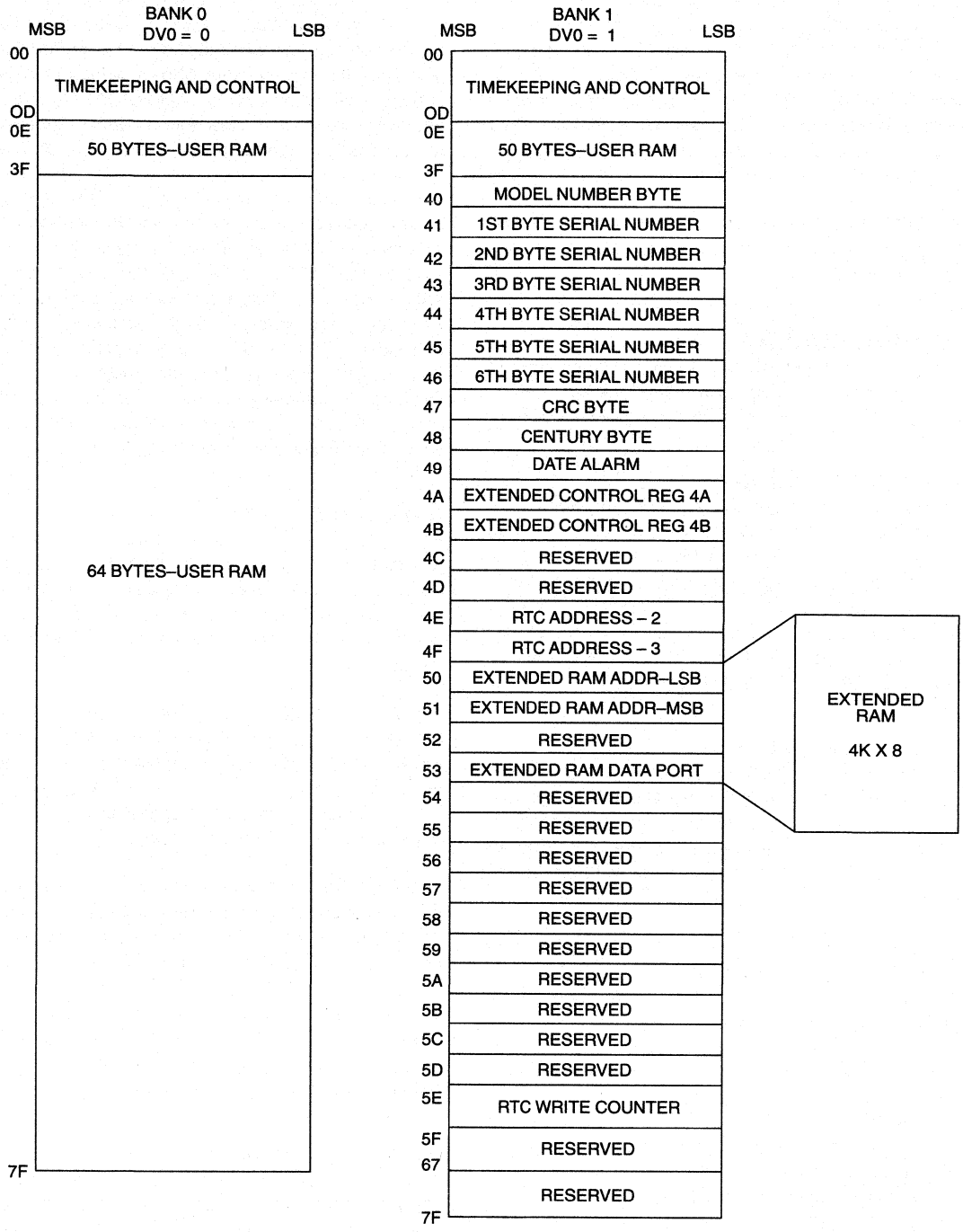
The extended functions provided by the DS17485/DS17487 that are new to the RAMified RTC family are accessed via a software controlled bank switching scheme, as illustrated in Figure 4. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS17485/DS17487 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers which provide control and status for the extended functions will be accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

1. 64–bit Silicon Serial Number
2. Century counter
3. Date Alarm
4. Auxiliary Battery Control/Status
5. Wake Up
6. Kickstart
7. RAM Clear Control/Status
8. 4K bytes Extended RAM Access

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and will return a 0 if read.

DS17485/DS17487 EXTENDED REGISTER BANK DEFINITION Figure 4



SILICON SERIAL NUMBER

A unique 64–bit lasered serial number is located in bank 1, registers 40h – 47h. This serial number is divided into three parts. The first byte in register 40h contains a model number to identify the device type and revision of the DS17485/DS17487. Registers 41h – 46h contain a unique binary number. Register 47h contains a CRC byte used to validate the data in registers 40h – 46h. All eight bytes of the serial number are read–only registers.

The DS17485/DS17487 is manufactured such that no two devices will contain an identical number in locations 41h – 47h.

CENTURY COUNTER

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

RTC WRITE COUNTER

An eight bit counter located in extended register bank 1, 5Eh, will count the number of times the RTC is written to. This counter will be incremented on the rising edge of the $\overline{WR}$ signal every time that the $\overline{CS}$ signal qualifies it. This counter is a read–only register and will roll–over after 256 RTC write pulses. This counter can be used to determine if and how many RTC writes have occurred since the last time this register was read.

4K X 8 EXTENDED RAM

The DS17485/DS17487 provides 4K x 8 of on–chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power–up, the RAM is taken out of write protect status by the internal power OK signal (POK) generated from the write protect circuitry.

The on–chip 4K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7 to AD0. Access to the SRAM is controlled by three on–chip latch registers. Two registers are used to hold the SRAM address, and the other register is used to hold read/write data. The SRAM address space is from 00h to 0FFFh.

Access to the extended 4K x 8 RAM is controlled via three of the Dallas registers shown in Figure 4. The Dallas registers in bank 1 must first be selected by setting the DV0 bit in register A to a logic 1. The 12–bit address of the RAM location to be accessed must be loaded into the extended RAM address registers located at 50h and 51h. The least significant address byte should be written to location 50h, and the most significant 4–bits (right–justified) should be loaded in location 51h. Data in the addressed location may be read by performing a read operation from location 53h, or written to by performing a write operation to location 53h. Data in any addressed location may be read or written repeatedly without changing the address in location 50h and 51h.

To read or write consecutive extended RAM locations, a burst mode feature can be enabled to increment the extended RAM address. To enable the burst mode feature, set the BME bit in the extended control register 4Ah, to a logic 1. With burst mode enabled, write the extended RAM starting address location to registers 50h and 51h. Then read or write the extended RAM data from/to register 53h. The extended RAM address locations are automatically incremented on the rising edge of $\overline{RD}$ or $\overline{WR}$ only when register 53h is being accessed. Refer to the Burst Mode Timing Waveform.

AUXILIARY BATTERY

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS17485/DS17487 kickstart, wake up, and SQW output features in the absence of V_{CC}. This power source must be available in order to use these auxiliary features when no V_{CC} is applied to the device.

The Auxiliary Battery Enable (ABE; bank 1, register 04BH) bit in extended control register 4B is used to turn on and off the auxiliary battery for the above functions in the absence of V_{CC}. When set to a 1, V_{BAUX} battery power is enabled, and when cleared to 0, V_{BAUX} battery power is disabled to these functions.

In the DS17485/DS17487, this auxiliary battery may be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended external RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS17485 is to be backed-up using a single battery with the auxiliary features enabled, then V_{BAUX} should be used and connected to V_{BAT}. If V_{BAUX} is not to be used, it should be grounded and ABE should be cleared to 0.

WAKE UP/KICKSTART

The DS17485/DS17487 incorporates a wake up feature which can power the system on at a pre-determined date through activation of the $\overline{PWR}$ output pin. In addi-

tion, the kickstart feature can allow the system to be powered up in response to a low going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin. As a result, system power may be applied upon such events as a key closure, or modem ring detect signal. In order to use either the wake up or the kickstart features, the DS17485/DS17487 must have an auxiliary battery connected to the V_{BAUX} pin and the oscillator must be running and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the $\overline{PWR}$ pin will not be driven low in response to a kickstart or wakeup condition, while in battery-backed mode.

The wake up feature is controlled through the Wake up Interrupt Enable bit in extended control register 4B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake up feature, clearing WIE to 0 disables it. Similarly, the kickstart feature is controlled through the Kickstart Interrupt Enable bit in extended control register 4B (KSE, bank 1, 04BH).

A wake up sequence will occur as follows: When wake up is enabled via WIE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar will monitor the current date for a match condition with the date alarm register (bank 1, register 049H). In conjunction with the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake up will occur at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm will occur regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the $\overline{PWR}$ pin will automatically be driven low. This output can be used to turn on the main system power supply which provides V_{CC} voltage to the DS17485/DS17487 as well as the other major components in the system. Also at this time, the Wake Up flag (WF, bank 1, register 04AH) will be set, indicating that a wake up condition has occurred.

A kickstart sequence will occur when kickstarting is enabled via KSE = 1. While the system is powered down, the $\overline{KS}$ input pin will be monitored for a low going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line will be pulled low, as it is for a wake up condition. Also at this time, the Kickstart Flag (KF, bank 1, register 04AH) will be set, indicating that a kickstart condition has occurred.

The timing associated with both the wake up and kickstarting sequences is illustrated in the Wake Up / Kickstart Timing Diagram in the Electrical Specifications section of this data sheet. The timing associated with these functions is divided into 5 intervals, labeled 1-5 on the diagram.

The occurrence of either a kickstart or wake up condition will cause the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS17485/DS17487 V_{CC} pin rises above the 3 volt power fail level before the power on timeout period (t_{POTO}) expires, then $\overline{PWR}$ will remain at the active low level. If V_{CC} does not rise above the 3 volt power fail voltage in this time, then the $\overline{PWR}$ output pin will be turned off and will return to its high impedance level. In this event, the $\overline{IRQ}$ pin will also remain tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power on sequence will remain set until cleared by software during a subsequent system power on.

If V_{CC} is applied within the timeout period, then the system power on sequence will continue as shown in intervals 2-5 in the timing diagram. During interval 2, $\overline{PWR}$ will remain active and $\overline{IRQ}$ will be driven to its active low level, indicating that either WF or KF was set in initiating the power on. In the diagram $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit will be automatically cleared to 0 in response to a successful power on. The $\overline{PWR}$ line will remain active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing zeroes to both of these control bits. As long as no other interrupt within the DS17485/DS17487 is pending, the $\overline{IRQ}$ line will be taken inactive once these bits are reset. Execution of the application software may proceed. During this time, both the wake up and kickstart functions may be used to generate status and interrupts. WF will be set in response to a date, hours, minutes, and seconds match condition. KF will be set in response to a low going transition on $\overline{KS}$. If the associated interrupt enable bit is set (WIE and/or KSE) then the $\overline{IRQ}$ line will driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS17485/DS17487 may cause $\overline{IRQ}$ to be driven low. While system power is applied, the on chip logic will always attempt to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake up condition. This is true even if $\overline{PWR}$ was pre-

viously inactive as the result of power being applied by some means other than wake up or kickstart.

The system may be powered down under software control by setting the PAB bit to a logic 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ}$ output pin will be placed in a high impedance state when V_{CC} goes below V_{PF}. If the system is to be again powered on in response to a wake up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and nonvolatile RAM is in effect and $\overline{IRQ}$ is tri-stated, and monitoring of wake up and kickstart takes place. If PRS=1, $\overline{PWR}$ stays active, otherwise if PRS=0 $\overline{PWR}$ is tri–stated.

RAM CLEAR

The DS17485/DS17487 provides a RAM clear function for the 114 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V_{CC} pin.

The RAM clear function is enabled or disabled via the RAM Clear Enable bit (RCE; bank 1, register 04BH). When this bit is set to a logic 1, the 114 bytes of user RAM will be cleared (all bits set to 1) when an active low transition is sensed on the $\overline{RCLR}$ pin. This action will have no effect on either the clock/calendar settings or upon the contents of the extended RAM. The RAM clear Flag (RF, bank 1, register 04AH) will be set when the RAM clear operation has been completed. If V_{CC} is present at the time of the RAM clear and RIE=1, the $\overline{IRQ}$ line will also be driven low upon completion. The interrupt condition can be cleared by writing a zero to the RF bit. The $\overline{IRQ}$ line will then return to its inactive high level provided there are no other pending interrupts. Once the $\overline{RCLR}$ pin is activated, all read/write accesses are locked out for a minimum recover time, specified as t_{REC} in the Electrical Characteristics section.

When RCE is cleared to zero, the RAM clear function is disabled. The state of the $\overline{RCLR}$ pin will have no effect on the contents of the user RAM, and transitions on the $\overline{RCLR}$ pin have no effect on RF.

EXTENDED CONTROL REGISTERS

Two extended control registers are provided to supply controls and status information for the extended features offered by the DS17485/DS17487. These are designated as extended control registers 4A and 4B and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows.

EXTENDED CONTROL REGISTER 4A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	BME	*	PAB	RF	WF	KF

VRT2 - The Valid RAM and Time 2 bit is a read only status bit. When VRT2 = 0, the RTC and RAM data are questionable and indicates that the lithium energy source connected to the V_{BAUX} input has been exhausted and should be replaced. This bit indicates the status of the V_{BAUX} input.

INCR - Increment in Progress status bit. This bit is set to a 1 when an increment to the time/date registers is in progress and the alarm checks are being made. INCR will be set to a 1 at 122 µs before the update cycle starts and will be cleared to 0 at the end of each update cycle.

BME – Burst Mode Enable. The burst mode enable bit allows the extended user RAM address registers to automatically increment for consecutive reads and writes. When BME is set to a logic one, the automatic incrementing will be enabled and when BME is set to a logic zero, the automatic incrementing will be disabled.

PAB - Power Active Bar control bit. When this bit is 0, the $\overline{PWR}$ pin is in the active low state. When this bit is 1, the $\overline{PWR}$ pin is in the high impedance state. This bit can be written to a logic 1 or 0 by the user. If either WF AND WIE = 1 OR KF AND KSE = 1, the PAB bit will be cleared to 0.

RF - Ram Clear Flag. This bit will be set to a logic 1 when a high to low transition occurs on the $\overline{RCLR}$ input if RCE=1. The RF bit is cleared by writing it to a logic 0. This bit can also be written to a logic 1 to force an interrupt condition.

WF - Wake up Alarm Flag - This bit is set to 1 when a wake up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

KF - Kickstart Flag - This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

EXTENDED CONTROL REGISTER 4B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32K	CS	RCE	PRS	RIE	WIE	KSE

ABE - Auxiliary Battery Enable. This bit when written to a logic 1 will enable the V_{BAUX} pin for extended functions.

E32K - Enable 32.768 KHz output. This bit when written to a logic 1 will enable the 32.768 KHz oscillator frequency to be output on the SQW pin. E32K is set to a one when V_{CC} is powered up.

CS – Crystal Select Bit. When CS is set to a 0, the oscillator is configured for operation with a crystal that has a 6 pF specified load capacitance. When CS=1, the oscillator is configured for a 12.5 pF crystal.

RCE - RAM Clear Enable bit. When set to a 1, this bit enables a low level on $\overline{RCLR}$ to clear all 114 bytes of user RAM. When RCE = 0, $\overline{RCLR}$ and the RAM clear function are disabled.

PRS – PAB Reset Select Bit. When set to a 0 the $\overline{PWR}$ pin will be set hi–Z when the DS17485 goes into power fail. When set to a 1, the $\overline{PWR}$ pin will remain active upon entering power fail.

RIE - Ram Clear Interrupt Enable. When RIE is set to a 1, the $\overline{IRQ}$ pin will be driven low when a RAM clear function is completed.

WIE - Wake Up Alarm Interrupt Enable. When V_{CC} voltage is absent and WIE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a wake up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If WIE is set while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to WF being set to 1. When WIE is cleared to a 0, the WF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

KSE - Kickstart Interrupt Enable. When V_{CC} voltage is absent and KSE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If KSE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to KF being set to 1. When KSE is cleared to a 0, the KF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

* Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no effect on operation.

SYSTEM MAINTENANCE INTERRUPT (SMI) RECOVERY STACK

An SMI recovery register stack is located in the extended register bank, locations 4Eh and 4Fh. This register stack, shown below, can be used by the BIOS to recover from an SMI occurring during an RTC read or write.

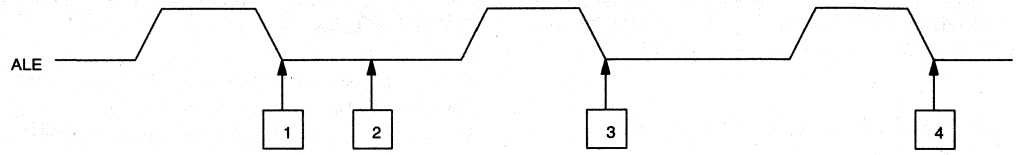
	RTC ADDRESS
	RTC ADDRESS – 1
4Eh	RTC ADDRESS – 2
4Fh	RTC ADDRESS – 3

SMI RECOVERY STACK

7	6	5	4	3	2	1	0
DV0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

REGISTER BIT DEFINITION

The RTC address is latched on the falling edge of the ALE signal. Each time an RTC address is latched, the register address stack is pushed. The stack is only four registers deep, holding the three previous RTC addresses in addition to the current RTC address being accessed. The following waveform illustrates how the BIOS could recover the RTC address when an SMI occurs.



1. The RTC address is latched.
2. An SMI is generated before an RTC read or write occurs.
3. RTC address 0Ah is latched and the address from "1" is pushed to the "RTC Address – 1" stack location. This step is necessary to change the bank select bit, DV0=1.
4. RTC address 4Eh is latched and the address from "1" is pushed to location 4Eh, "RTC Address – 2" while 0Ah is pushed to the "RTC Address – 1" location. The data in this register, 4Eh, is the RTC address lost due to the SMI.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature DS17485	–55°C to +125°C
Storage Temperature DS17487	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage 5 Volt Operation	V_{CC}	4.5	5.0	5.5	V	1
Power Supply Voltage 3 Volt Operation	V_{CC}	2.7	3.0	3.3	V	1
Input Logic 1	V_{IH}	2.3		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		0.6	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	1
Auxiliary Battery Voltage	V_{BAUX}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		25	50	mA	2, 3
CMOS Standby Current ($\overline{CS}$=V_{CC}-0.2V)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
Output Leakage Current	I_{OL}	–1		+1	µA	6
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Power Fail Trip Point	V_{PF}	4.25	4.37	4.5	V	4
Battery Switch Voltage	V_{SW}		V_{BAT}, V_{BAUX}		V	9

DC ELECTRICAL CHARACTERISTICS (cont'd) (0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Leakage OSC ON	I_{BAT1}		0.50	1.5	µA	12
Battery Leakage OSC OFF	I_{BAT2}		0.050	1.0	µA	12
I/O Leakage	I_{LO}	–1		+1	µA	5
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			10.0	mA	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=3.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		15	30	mA	2, 3
CMOS Standby Current ($\overline{CS}$=V_{CC}-0.2)	I_{CC2}		0.5	2	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
Output Leakage Current	I_{OL}	–1		+1	µA	6
Output Logic 1 Voltage @ 0.4 mA	V_{OH}	2.4			V	
Output Logic 0 Voltage @ 0.8 mA	V_{OL}			0.4	V	
Power Fail Trip Point	V_{PF}	2.5	2.6	2.7	V	4
Battery Leakage OSC ON	I_{BAT1}		0.50	1.5	µA	12
Battery Leakage OSC OFF	I_{BAT2}		0.050	1.0	µA	12
I/O Leakage	I_{LO}	–1		+1	µA	5
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			4	mA	1

RTC AC TIMING CHARACTERISTICS

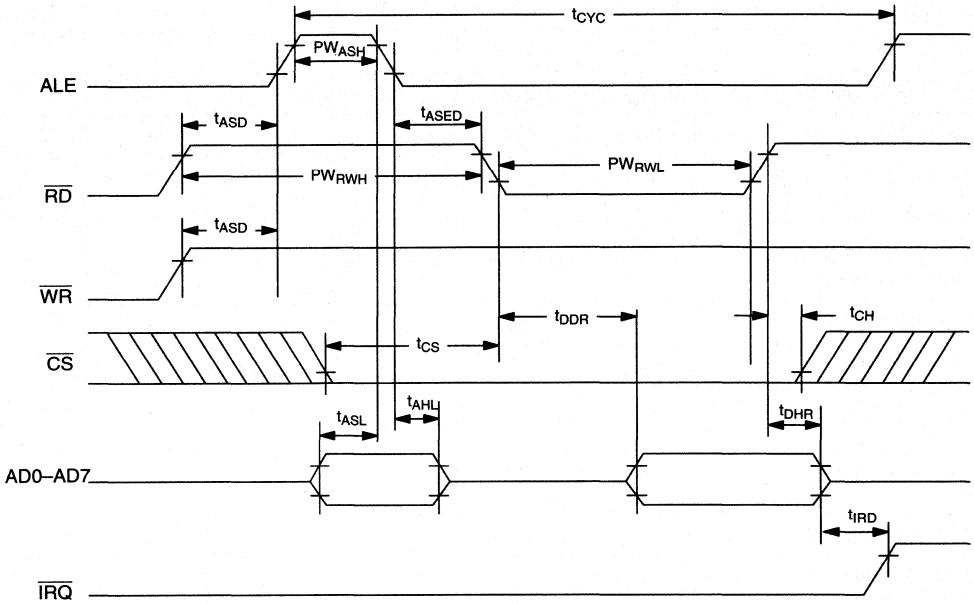
(0°C to 70°C; V_{CC} = 3.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	915		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{RWL}	375			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{RWH}	450			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	75			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		120	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	90			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	30			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	30			ns	
Pulse Width ALE High	PW_{ASH}	180			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	120			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		370	ns	7
Data Setup Time	t_{DSW}	180			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

AC TEST CONDITIONS

Output Load: 50 pF
Input Pulse Levels: 0–3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS17485/DS17487 BUS TIMING FOR READ CYCLE TO RTC

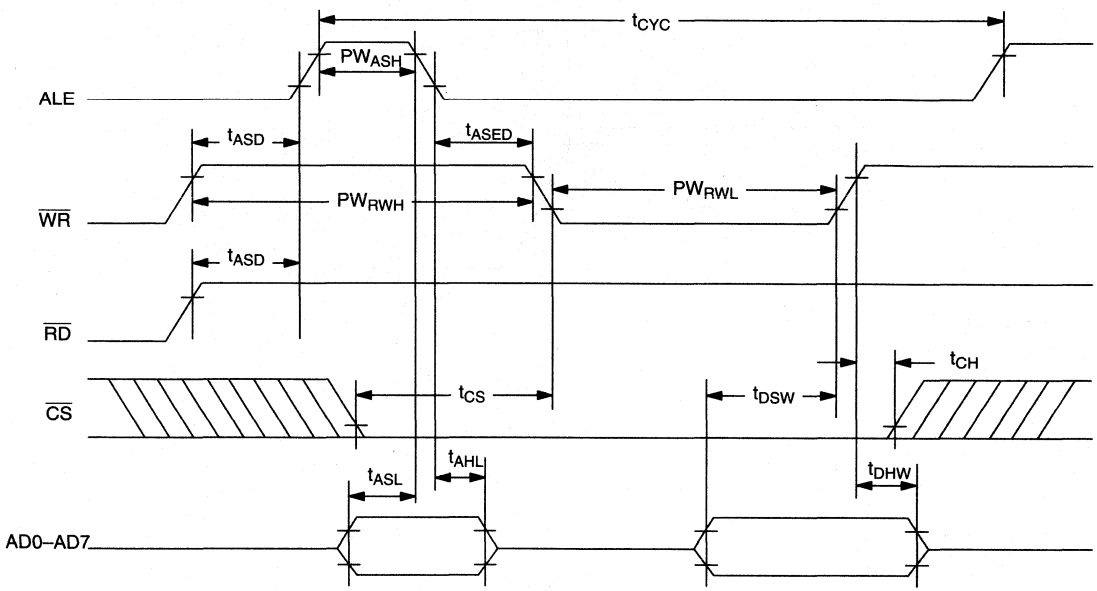


RTC AC TIMING CHARACTERISTICS

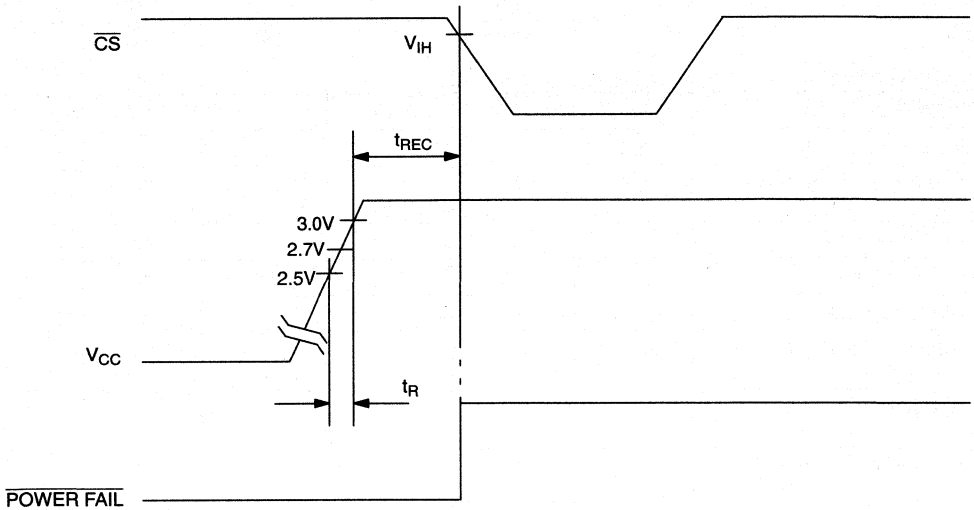
(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{RWL}	125			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{RWH}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	7
Data Setup Time	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

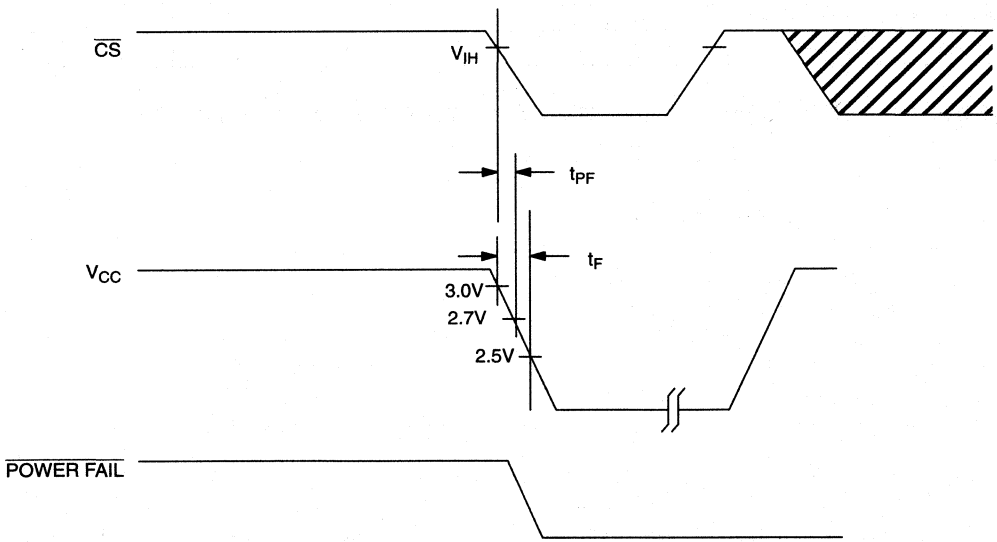
DS17485/DS17487 BUS TIMING FOR WRITE CYCLE TO RTC AND RTC REGISTERS



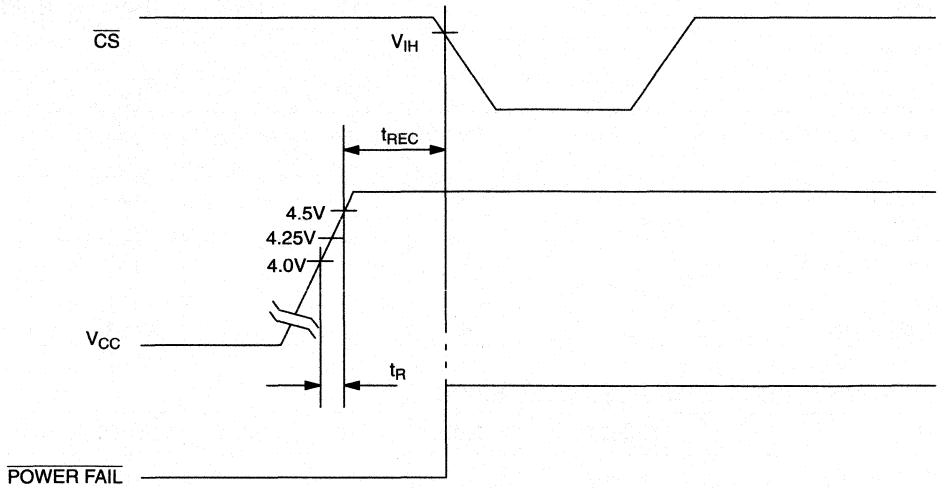
POWER–UP CONDITION 3 VOLT DEVICE



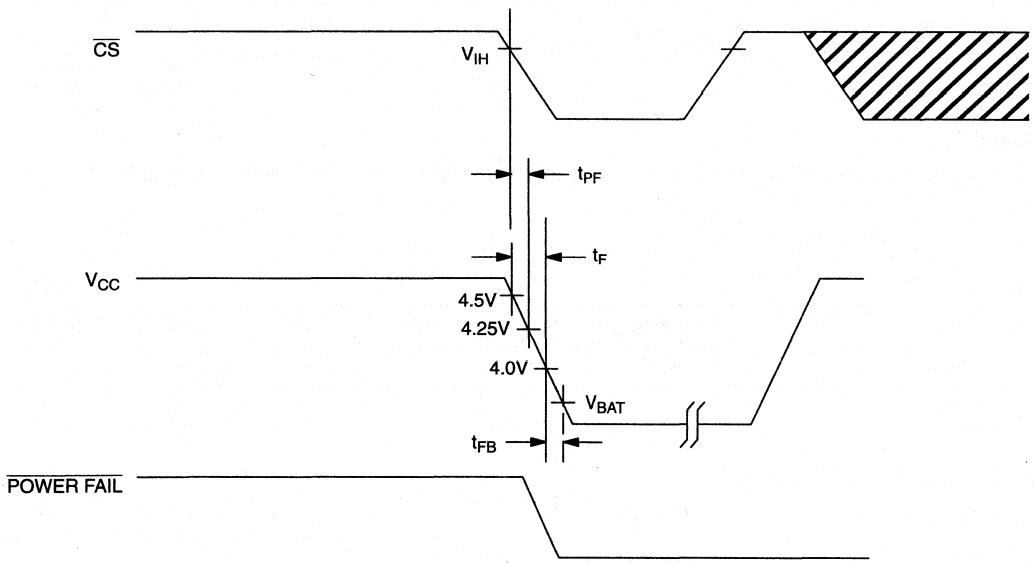
POWER–DOWN CONDITION 3 VOLT DEVICE



POWER–UP CONDITION 5.0 VOLT DEVICE



POWER–DOWN CONDITION 5.0 VOLT DEVICE



POWER-UP POWER-DOWN TIMING 5 VOLT DEVICE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	10, 11

POWER-UP POWER-DOWN TIMING 3 VOLT DEVICE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $2.5 \le V_{CC} \le 3.0V$	300			µs	
V_{CC} Slew Rate Power Up	t_R $3.0V \ge V_{CC} \ge 2.5V$	0			µs	
Expected Data Retention	t_{DR}	10			years	10, 11

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

(t_A = 25°C)

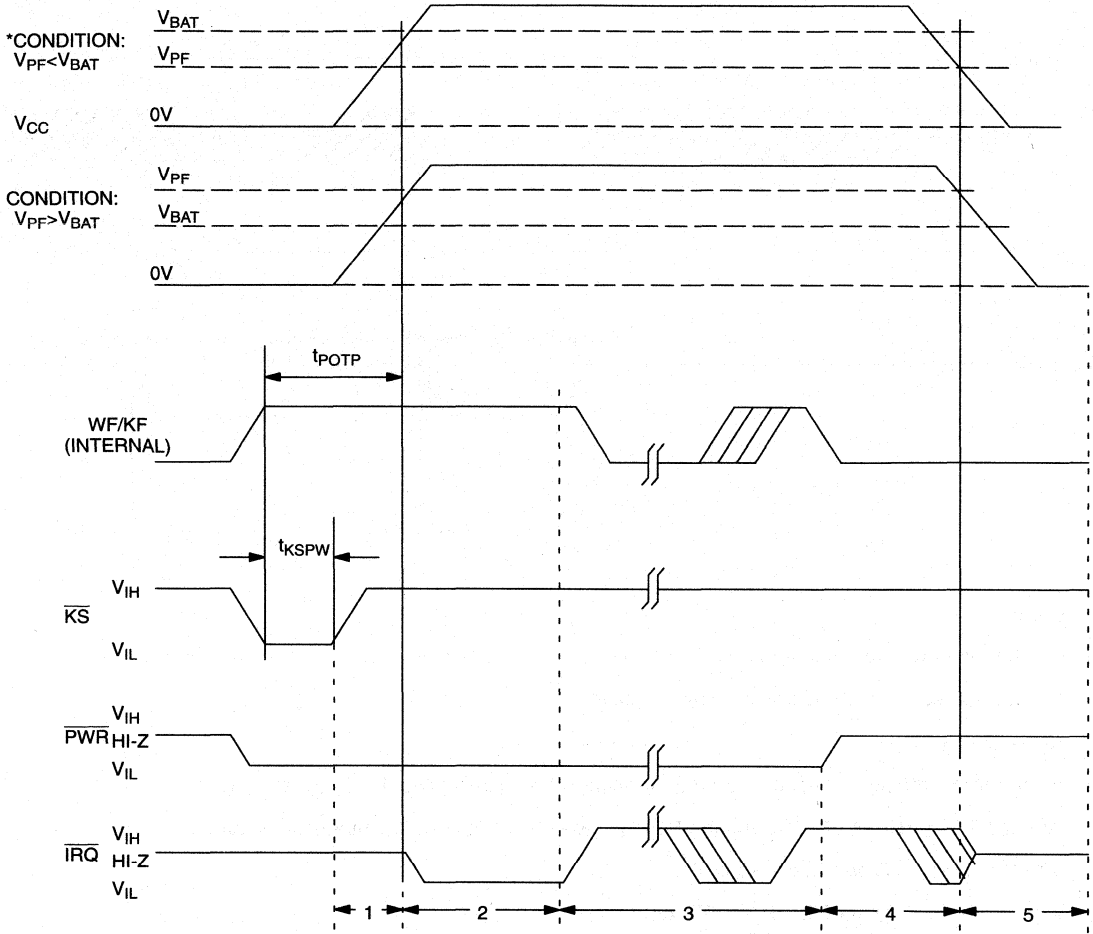
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

WAKE UP/KICKSTART TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t_{KSPW}	2			µs	
Wake up/Kickstart Power On Timeout	t_{POTO}	2			seconds	8

WAKE UP/KICKSTART TIMING

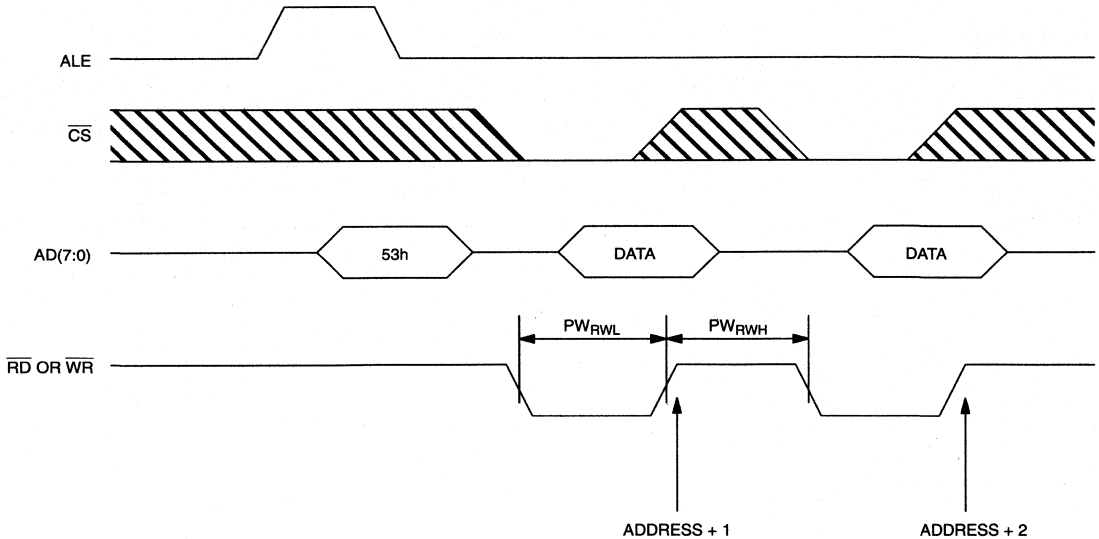


NOTE:

Time intervals shown above are referenced in Wake up/Kickstart section.

* This condition can occur with the 3 volt device.

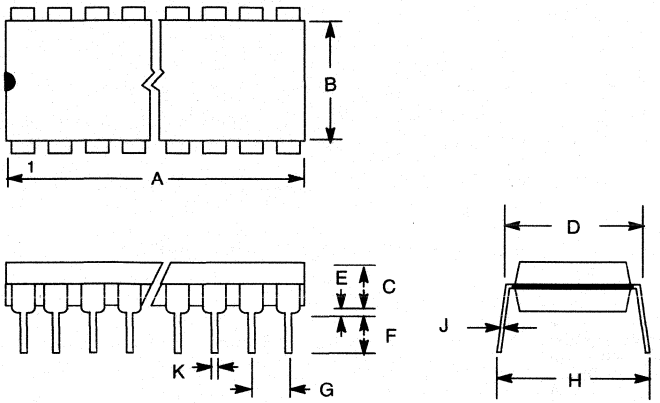
BURST MODE TIMING WAVEFORM



NOTES:

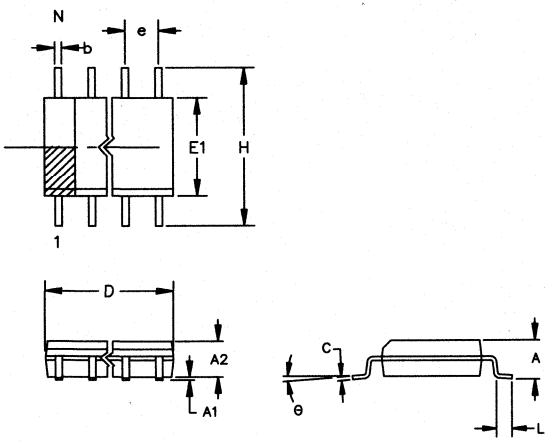
1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Write protection trip point occurs during power fail prior to switchover from V_{CC} to V_{BAT}.
5. Applies to the AD0–AD7 pins, and the SQW pin when each is in a high impedance state.
6. The $\overline{IRQ}$ and $\overline{PWR}$ pins are open drain.
7. Measured with a load of 50 pF + 1 TTL gate.
8. Wakeup kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.
9. V_{SW} is determined by the larger of V_{BAT} and V_{BAUX}.
10. The DS17487 will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
11. t_{DR} is the amount of time that the internal battery can power the internal oscillator and internal registers of the DS17487.
12. I_{BAT1} and I_{BAT2} are measured at V_{BAT} = 3.5V.

DS17485 24–PIN DIP



PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	1.245 31.62	1.270 32.25
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.380	0.050 1.27
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.625 15.88	0.675 17.15
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

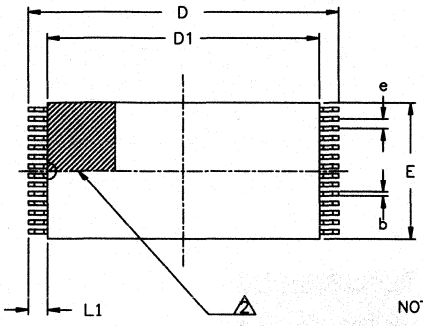
DS17485 24–PIN SOIC



The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

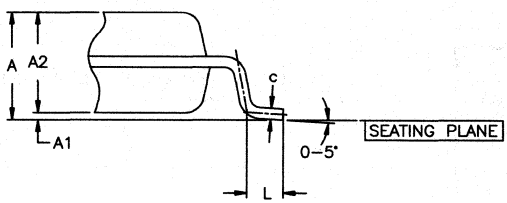
PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33
D IN. MM	0.598 15.19	0.612 15.54
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02
Θ	0°	8°

DS17485E 28–PIN TSOP



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT ONE HALF OF ITS AREA MUST BE LOCATED WITHIN THE ZONE INDICATED.

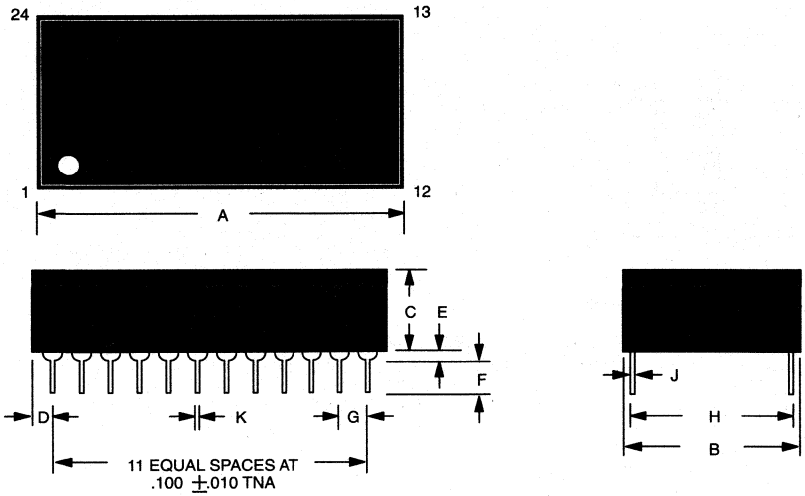


DETAIL A

PKG	28-PIN	
DIM	MIN	MAX
A	–	1.20
A1	0.05	–
A2	0.91	1.02
b	0.18	0.27
c	0.15	0.20
D	13.20	13.60
D1	11.70	11.90
E	7.90	8.10
e	0.55 BSC	
L	0.30	0.70
L1	0.80 BSC	

56–G5003–000

DS17487 REAL TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.720 18.29	0.740 18.80
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

DS17885/DS17887
3 Volt/5 Volt Real Time Clock

3

FEATURES
Incorporates industry standard DS1287 PC clock plus enhanced features:

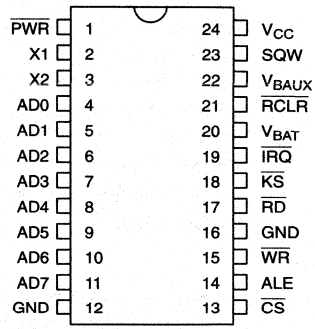
- +3 or +5 volt operation
- SMI recovery stack
- 64–bit silicon serial number
- Power control circuitry supports system power on from date/time alarm or key closure
- 32 KHz output on power–up
- Crystal select bit allows RTC to operate with 6 pF or 12.5 pF crystal
- 114 bytes user NVRAM
- Auxiliary battery input
- 8K bytes additional NVRAM
- RAM clear input
- Century register
- Date alarm register
- Compatible with existing BIOS for original DS1287 functions
- Available as chip (DS17885) or standalone module with embedded battery and crystal (DS17887)

ORDERING INFORMATION

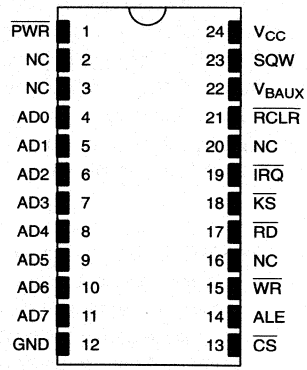
PART #	DESCRIPTION
DS17885–X	RTC Chip; 24–pin DIP
DS17885E–X	RTC Chip; 28–pin TSOP
DS17885S–X	RTC Chip; 24–pin SOIC
DS17887–X	RTC Module; 24–pin DIP

–3 +3 volt device
–5 +5 volt device

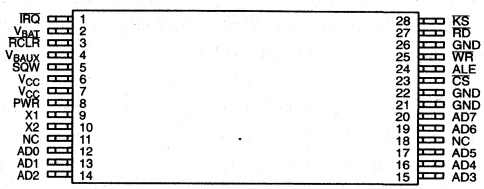
PIN ASSIGNMENT



DS17885 24–PIN DIP
DS17885S 24–PIN SOIC



DS17887 24–PIN ENCAPSULATED PACKAGE



DS17885E 28–PIN TSOP

PIN DESCRIPTION

X1	–	Crystal Input
X2	–	Crystal Output
$\overline{RCLR}$	–	RAM Clear Input
AD0-AD7	–	Mux'ed Address/Data Bus
$\overline{PWR}$	–	Power–on Interrupt Output (open drain)
$\overline{KS}$	–	Kickstart Input
$\overline{CS}$	–	RTC Chip Select Input
ALE	–	RTC Address Strobe
$\overline{WR}$	–	RTC Write Data Strobe
$\overline{RD}$	–	RTC Read Data Strobe
$\overline{IRQ}$	–	Interrupt Request Output (open drain)
SQW	–	Square Wave Output
V_{CC}	–	+3 or +5 Volt Main Supply
GND	–	Ground
V_{BAT}	–	Battery + Supply
V_{BAUX}	–	Auxiliary Battery Supply
NC	–	No Connection

DESCRIPTION

The DS17885/DS17887 is a real time clock (RTC) designed as a successor to the industry standard DS1285, DS1385, DS1485, DS1585, and DS1685 PC real time clocks. This device provides the industry standard DS1285 clock function with either +3.0 or +5.0 volt operation. The DS17885 also incorporates a number of enhanced features including a silicon serial number, power on/off control circuitry, 114 bytes of user NVSRAM plus 8K bytes of additional NVRAM, and 32.768 KHz output for sustaining power management activities.

The DS17885/DS17887 power control circuitry allows the system to be powered on via an external stimulus, such as a keyboard or by a time and date (wake up) alarm. The $\overline{PWR}$ output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS17885 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time–of–day and memory status in the absence of power. The DS17887 incorporates the DS17885 chip, a 32.768 KHz crystal, and a lithium battery in a complete, self–contained timekeeping module. The entire unit is fully tested at Dallas Semiconductor such that a minimum of 10 years of timekeeping and data retention in the absence of V_{CC} is guaranteed.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS17885/DS17887. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +3 volt or +5 volt input.

SQW (Square Wave Output) - The SQW pin will provide a 32 KHz square wave output, t_{REC}, after a power–up condition has been detected. This condition sets the following bits, enabling the 32 KHz output; DV1=1, and E32K=1. A square wave will be output on this pin if either SQWE=1 or E32K=1. If E32K=1, then 32 KHz will be output regardless of the other control bits. If E32K=0, then the output frequency is dependent on the control bits in register A. The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in register B or the E32K bit in extended register 4Bh. A 32 KHz SQW signal is output when the Enable 32 KHz (E32K) bit in extended register 4Bh is a logic one, and V_{CC} is above V_{PF}. A 32 KHz square wave is also available when V_{CC} is less than V_{PF} if E32K=1, ABE=1, and voltage is applied to the V_{BAUX} pin.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS17885 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, at which time the DS17885/DS17887 latches the address. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ pulse. In a read cycle the DS17885/DS17887 outputs 8 bits of data during the latter portion of the $\overline{RD}$ pulse. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high. The address/data bus also serves as a bidirectional data path for the external extended RAM.

ALE (RTC Address Strobe Input; active high) - A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS17885/DS17887.

$\overline{RD}$ (RTC Read Input; active low) - $\overline{RD}$ identifies the time period when the DS17885/DS17887 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

$\overline{WR}$ (RTC Write Input; active low) -The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed register.

$\overline{CS}$ (RTC Chip Select Input; active low) - The Chip Select signal must be asserted low during a bus cycle for DS17885/DS17887 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place with ALE asserted but without asserting $\overline{CS}$ will latch addresses. However, no data transfer will occur.

$\overline{IRQ}$ (Interrupt Request Output; open drain, active low) - The $\overline{IRQ}$ pin is an active low output of the DS17885/DS17887 that can be tied to the interrupt input of a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application software must clear all enabled flag bits contributing to $\overline{IRQ}$'s active state.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ pin is an open drain output and requires an external pull-up resistor.

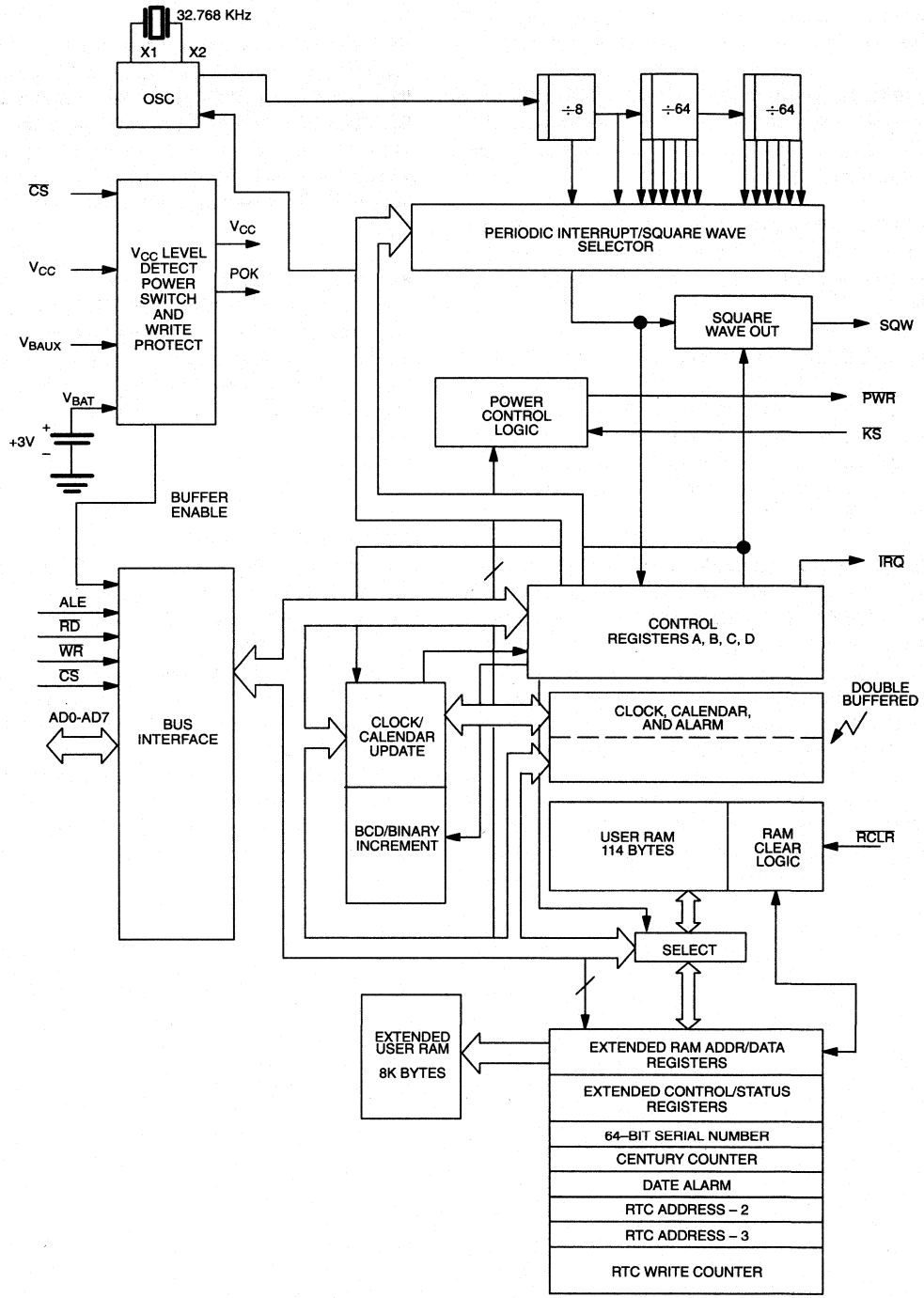
$\overline{PWR}$ (Power On Output; open drain, active low) - The $\overline{PWR}$ pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the DS17885/DS17887, $\overline{PWR}$ may be automatically activated from a Kickstart input via the $\overline{KS}$ pin or from a Wake Up interrupt. Once the system is powered on, the state of $\overline{PWR}$ can be controlled via bits in the Dallas registers.

$\overline{KS}$ (Kickstart Input; active low) - When V_{CC} is removed from the DS17885/DS17887, the system can be powered on in response to an active low transition on the $\overline{KS}$ pin, as might be generated from a key closure. V_{BAUX} must be present and Auxiliary Battery Enable bit (ABE) must be set to 1 if the kickstart function is used, and the $\overline{KS}$ pin must be pulled up to the V_{BAUX} supply. While V_{CC} is applied, the $\overline{KS}$ pin can be used as an interrupt input.

$\overline{RCLR}$ (RAM Clear Input; active low) - If enabled by software, taking $\overline{RCLR}$ low will result in the clearing of the 114 bytes of user RAM. When enabled, $\overline{RCLR}$ can be activated whether or not V_{CC} is present.

V_{BAUX} - Auxiliary battery input required for kickstart and wake up features. This input also supports clock/calendar and user RAM if V_{BAT} is at lower voltage or is not present. A standard +3 volt lithium cell or other energy source can be used. Battery voltage must be held between +2.5 and +3.7 volts for proper operation. If V_{BAUX} is not going to be used it should be grounded and auxiliary battery enable bit bank 1, register 4BH, should=0.

DS17885/DS17887 BLOCK DIAGRAM Figure 1



DS17885 ONLY

X1, X2 - Connections for a standard 32.768 KHz quartz crystal. For greatest accuracy, the DS17885 must be used with a crystal that has a specified load capacitance of either 6 pF or 12.5 pF. The Crystal Select (CS) bit in Extended Control Register 4B is used to select operation with a 6 pF or 12.5 pF crystal. The crystal is attached directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area.

For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks". The DS17885 can also be driven by an external 32.768 KHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

V_{BAT} - Battery input for any standard 3 Volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation.

POWER–DOWN/POWER–UP CONSIDERATIONS

The real-time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS17885/DS17887 and reaches a level of greater than V_{PF} (power fail trip point), the device becomes accessible after t_{REC}, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied.

The DS17885/DS17887 is available in either a 3 volt or a 5 volt device.

The 5 volt device is fully accessible and data can be written and read only when V_{CC} is greater than 4.5 volts. When V_{CC} is below 4.5 volts, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below the greater of V_{BAT} and V_{BAUX}, the RAM and timekeeper are switched over to a lithium battery connected either to the V_{BAT} pin or V_{BAUX} pin.

The 3 volt device is fully accessible and data can be written or read only when V_{CC} is greater than 2.7 volts. When V_{CC} falls below V_{PF}, access to the device is inhibited. If V_{PF} is less than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply (the greater of V_{BAT} and V_{BAUX}) when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply when V_{CC} drops below the larger of V_{BAT} and V_{BAUX}.

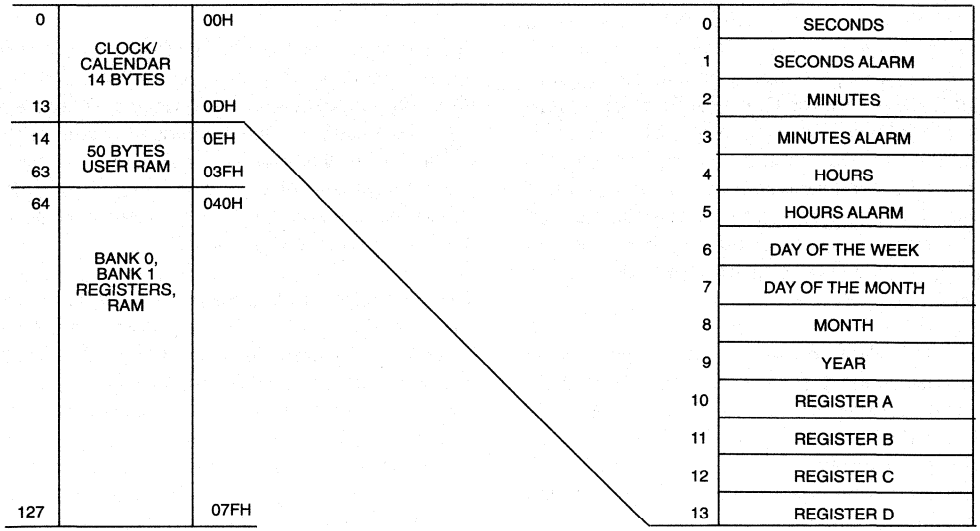
When V_{CC} falls below V_{PF}, the chip is write-protected. With the possible exception of the $\overline{KS}$, $\overline{PWR}$, $\overline{RCLR}$ and SQW pins, all inputs are ignored and all outputs are in a high impedance state.

RTC ADDRESS MAP

The address map for the RTC registers of the DS17885/DS17887 is shown in Figure 2. The address map consists of the 14 clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and four bytes are used for control and status. All registers can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

DS17885 REAL TIME CLOCK ADDRESS MAP Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching will be explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The four alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second use condition is to insert a "don't care" state in one or more of the four alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second. The three alarm bytes may be used in conjunction with the date alarm as described in the Wakeup/Kickstart section. The century counter will be discussed later in this text.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
00H	Seconds	0-59	00-3B	00-59
01H	Seconds Alarm	0-59	00-3B	00-59
02H	Minutes	0-59	00-3B	00-59
03H	Minutes Alarm	0-59	00-3B	00-59
04H	Hours 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours 24-Hour Mode	0-23	00-17	00-23
05H	Hours Alarm 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92 PM
	Hours Alarm 24-hr. Mode	0-23	00-17	00-23
06H	Day of Week Sunday=1	1-7	01-07	01-07
07H	Date of Month	1-31	01-1F	01-31
08H	Month	1-12	01-0C	01-12
09H	Year	0-99	00-63	00-99
BANK 1, 48H	Century	0-99	00-63	00-99
BANK 1, 49H	Date Alarm	1-31	01-1F	01-31

CONTROL REGISTERS

The four control registers; A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

NONVOLATILE RAM - RTC

The general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS17885/DS17887. They can be used by the application program as nonvolatile memory and are fully available during the update cycle.

The user RAM is divided into two separate memory banks. When the bank 0 is selected, the 14 real time clock registers and 114 bytes of user RAM are accessible. When bank 1 is selected, an additional 8K bytes of user RAM are accessible through the extended RAM address and data registers.

INTERRUPT CONTROL

The DS17885/DS17887 includes six separate, fully automatic sources of interrupt for a processor:

1. Alarm interrupt
2. Periodic interrupt
3. Update-ended interrupt
4. Wake up interrupt
5. Kickstart interrupt
6. RAM clear interrupt

The conditions which generate each of these independent interrupt conditions are described in greater detail elsewhere in this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are a total of six bits including three bits in Register B and three bits in Extended Register B which enable the interrupts. The extended register locations are described later. Writing a logic 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ will immediately be set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As

a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits which are set remain stable throughout the read cycle. All bits which were set are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the $\overline{IRQ}$ line will be driven low when an interrupt flag bit is set and its corresponding enable bit is also set. $\overline{IRQ}$ will be held low as long as at least one of the six possible interrupt sources has it s flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS17885/DS17887 initiated an interrupt is accomplished by reading Register C and finding IRQF=1. IRQF will remain set until all enabled interrupt flag bits are cleared to 0.

SQUARE WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768 KHz crystal tied to X1 and X2. The square wave output is enabled and disabled via the SQWE bit in Register B or the E32K bit in extended register 4Bh. If the square wave is enabled (SQWE=1 or E32K=1), then the output frequency will be determined by the settings of the E32K bit in Extended Register 4Bh and by the RS3-0 bits in Register A. If E32K=1, then a 32.768 KHz square wave will be output on the SQW pin regardless of the settings of RS3-0 and SQWE.

If E32K = 0, then the square wave output frequency is determined by the RS3-0 bits. These bits control a 1-of-15 decoder which selects one of thirteen taps that divide the 32.768 KHz frequency. The RS3-0 bits establish the SQW output frequency as shown in Table 2. In addition, RS3-0 bits control the periodic interrupt selection as described below.

If E32K=1, and the Auxiliary Battery Enable bit (ABE, bank 1; register 04BH) is enabled, and voltage is applied to V_{BAUX} then the 32 KHz square wave output signal will be output on the SQW pin in the absence of V_{CC}. This facility is provided to clock external power management circuitry. If any of the above requirements are not met, no square wave output signal will be generated on the SQW pin in the absence of V_{CC}.

A pattern of 01X in the DV2, DV1, and DV0, bits respectively, will turn the oscillator on and enable the countdown chain. Note that this is different than the DS1287, which required a pattern of 010 in these bits. DV0 is now a "don't care" because it is used for selection between register banks 0 and 1.

A pattern of 11X will turn the oscillator on, but the oscillator's countdown chain will be held in reset, as it was in the DS1287. Any other bit combination for DV2 and DV1 will keep the oscillator off.

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3-0 bits in Register A which select the square wave frequency (see Table 2). Changing the bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE and E32K bits control the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The Serialized RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, alarm and elapsed time byte is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows the time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all alarm locations.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

3

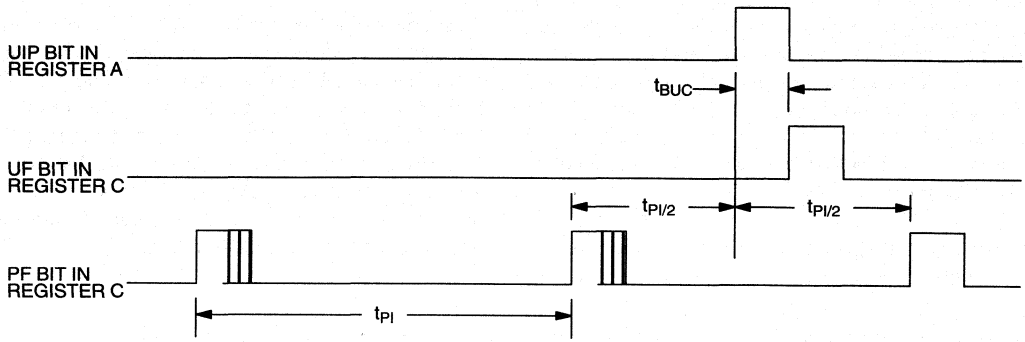
PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

EXT. REG. B	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
E32K	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625 ms	256 Hz
0	0	0	1	0	7.8125 ms	128 Hz
0	0	0	1	1	122.070 µs	8.192 KHz
0	0	1	0	0	244.141 µs	4.096 KHz
0	0	1	0	1	488.281 µs	2.048 KHz
0	0	1	1	0	976.5625 µs	1.024 KHz
0	0	1	1	1	1.953125 ms	512 Hz
0	1	0	0	0	3.90625 ms	256 Hz
0	1	0	0	1	7.8125 ms	128 Hz
0	1	0	1	0	15.625 ms	64 Hz
0	1	0	1	1	31.25 ms	32 Hz
0	1	1	0	0	62.5 ms	16 Hz
0	1	1	0	1	125 ms	8 Hz
0	1	1	1	0	250 ms	4 Hz
0	1	1	1	1	500 ms	2 Hz
1	X	X	X	X	*	32.768 KHz

*RS3-RS0 determine periodic interrupt rates as listed for E32K=0.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within (t_{PI} / 2+t_{BUC}) to ensure that data is not read during the update cycle.

UPDATE–ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1
t_{BUC} = DELAY TIME BEFORE UPDATE CYCLE = 244 µs

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These bits are defined as follows:

DV2 = Countdown Chain
- 1 - resets countdown chain only if DV1=1
- 0 - countdown chain enabled

DV1 = Oscillator Enable
- 0 - oscillator off
- 1 - oscillator on, V_{CC} power–up state

DV0 = Bank Select
- 0 - original bank
- 1 - extended registers

A pattern of 01X is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 01X is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

Enable the interrupt with the PIE bit;

Enable the SQW output pin with the SQWE or E32K bits;

Enable both at the same time and the same rate; or

Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS17885/DS17887.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS17885/DS17887 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS17885/DS17887 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one and E32K=0, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to zero and E32K=0, the SQW pin is held low. SQWE is a read/write bit. SQWE is set to a one when V_{CC} is powered up.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

3

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 WF = WIE = 1
AF = AIE = 1 KF = KSE = 1
UF = UIE = 1 RF = RIE = 1

i.e., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE) + (WF • WIE) + (KF • KSE) + (RF • RIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 3 THROUGH BIT 0 - These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit indicates the condition of the battery connected to the V_{BAT} pin or the battery connected to V_{BAUX}, whichever is at a higher voltage. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

EXTENDED FUNCTIONS

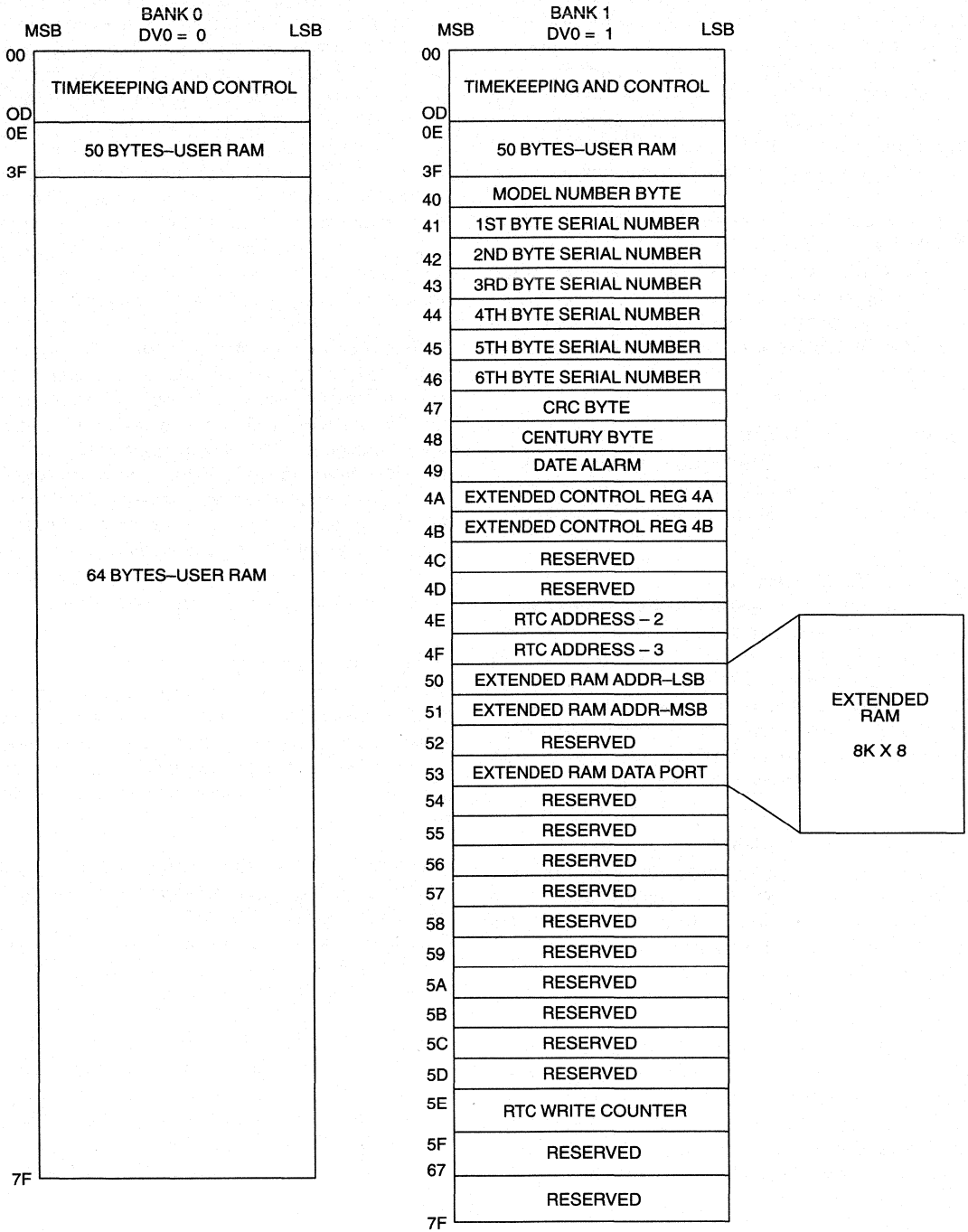
The extended functions provided by the DS17885/DS17887 that are new to the RAMified RTC family are accessed via a software controlled bank switching scheme, as illustrated in Figure 4. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS17885/DS17887 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers which provide control and status for the extended functions will be accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

1. 64–bit Silicon Serial Number
2. Century counter
3. Date Alarm
4. Auxiliary Battery Control/Status
5. Wake Up
6. Kickstart
7. RAM Clear Control/Status
8. 8K bytes Extended RAM Access

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and will return a 0 if read.

DS17885/DS17887 EXTENDED REGISTER BANK DEFINITION Figure 4



SILICON SERIAL NUMBER

A unique 64–bit lasered serial number is located in bank 1, registers 40h – 47h. This serial number is divided into three parts. The first byte in register 40h contains a model number to identify the device type and revision of the DS17885/DS17887. Registers 41h – 46h contain a unique binary number. Register 47h contains a CRC byte used to validate the data in registers 40h – 46h. All eight bytes of the serial number are read–only registers.

The DS17885/DS17887 is manufactured such that no two devices will contain an identical number in locations 41h – 47h. Blocks of numbers for these locations can be reserved by the customer. Contact Dallas Semiconductor for special ordering information for DS17885/DS17887's with reserved blocks of serial numbers.

CENTURY COUNTER

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

RTC WRITE COUNTER

An eight bit counter located in extended register bank 1, 5Eh, will count the number of times the RTC is written to. This counter will be incremented on the rising edge of the $\overline{WR}$ signal every time that the $\overline{CS}$ signal qualifies it. This counter is a read–only register and will roll–over after 256 RTC write pulses. This counter can be used to determine if and how many RTC writes have occurred since the last time this register was read.

8K X 8 EXTENDED RAM

The DS17885/DS17887 provides 8K x 8 of on–chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power–up, the RAM is taken out of write protect status by the internal power OK signal (POK) generated from the write protect circuitry.

The on–chip 8K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7 to AD0. Access to the SRAM is controlled by three on–chip latch registers. Two registers are used to hold the SRAM address, and the other register is used to hold read/write data. The SRAM address space is from 00h to 01FFFh.

Access to the extended 8K x 8 RAM is controlled via three of the Dallas registers shown in Figure 4. The Dallas registers in bank 1 must first be selected by setting the DV0 bit in register A to a logic 1. The 12–bit address of the RAM location to be accessed must be loaded into the extended RAM address registers located at 50h and 51h. The least significant address byte should be written to location 50h, and the most significant 5–bits (right–justified) should be loaded in location 51h. Data in the addressed location may be read by performing a read operation from location 53h, or written to by performing a write operation to location 53h. Data in any addressed location may be read or written repeatedly without changing the address in location 50h and 51h.

To read or write consecutive extended RAM locations, a burst mode feature can be enabled to increment the extended RAM address. To enable the burst mode feature, set the BME bit in the extended control register 4Ah, to a logic 1. With burst mode enabled, write the extended RAM starting address location to registers 50h and 51h. Then read or write the extended RAM data from/to register 53h. The extended RAM address locations are automatically incremented on the rising edge of $\overline{RD}$ or $\overline{WR}$ only when register 53h is being accessed. Refer to the Burst Mode Timing Waveform.

AUXILIARY BATTERY

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS17885/DS17887 kickstart, wake up, and SQW output features in the absence of V_{CC}. This power source must be available in order to use these auxiliary features when no V_{CC} is applied to the device.

The Auxiliary Battery Enable (ABE; bank 1, register 04BH) bit in extended control register B is used to turn on and off the auxiliary battery for the above functions in the absence of V_{CC}. When set to a 1, V_{BAUX} battery power is enabled, and when cleared to 0, V_{BAUX} battery power is disabled to these functions.

In the DS17885/DS17887, this auxiliary battery may be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended external RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS17885 is to be backed-up using a single battery with the auxiliary fea-

tures enabled, then V_{BAUX} should be used and connected to V_{BAT}. If V_{BAUX} is not to be used, it should be grounded and ABE should be cleared to 0.

WAKE UP/KICKSTART

The DS17885/DS17887 incorporates a wake up feature which can power the system on at a pre-determined date through activation of the $\overline{PWR}$ output pin. In addition, the kickstart feature can allow the system to be powered up in response to a low going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin. As a result, system power may be applied upon such events as a key closure, or modem ring detect signal. In order to use either the wake up or the kickstart features, the DS17885/DS17887 must have an auxiliary battery connected to the V_{BAUX} pin and the oscillator must be running and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the $\overline{PWR}$ pin will not be driven low in response to a kickstart or wakeup condition, while in battery-backed mode.

The wake up feature is controlled through the Wake up Interrupt Enable bit in extended control register B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake up feature, clearing WIE to 0 disables it. Similarly, the kickstart feature is controlled through the Kickstart Interrupt Enable bit in extended control register B (KSE, bank 1, 04BH).

A wake up sequence will occur as follows: When wake up is enabled via WIE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar will monitor the current date for a match condition with the date alarm register (bank 1, register 049H). In conjunction with the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake up will occur at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm will occur regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the $\overline{PWR}$ pin will automatically be driven low. This output can be used to turn on the main system power supply which provides V_{CC} voltage to the DS17885/DS17887 as well as the other major components in the system. Also at this time, the Wake Up flag (WF, bank 1, register 04AH) will be set, indicating that a wake up condition has occurred.

A kickstart sequence will occur when kickstarting is enabled via KSE = 1. While the system is powered down, the $\overline{KS}$ input pin will be monitored for a low going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line will be pulled low, as it is for a wake up condition. Also at this time, the Kickstart Flag (KF, bank 1, register 04AH) will be set, indicating that a kickstart condition has occurred.

The timing associated with both the wake up and kickstarting sequences is illustrated in the Wake Up / Kickstart Timing Diagram in the Electrical Specifications section of this data sheet. The timing associated with these functions is divided into 5 intervals, labeled 1-5 on the diagram.

The occurrence of either a kickstart or wake up condition will cause the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS17885/DS17887 V_{CC} pin rises above the 3 volt power fail level before the power on timeout period (t_{POTO}) expires, then $\overline{PWR}$ will remain at the active low level. If V_{CC} does not rise above the 3 volt power fail voltage in this time, then the $\overline{PWR}$ output pin will be turned off and will return to its high impedance level. In this event, the $\overline{IRQ}$ pin will also remain tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power on sequence will remain set until cleared by software during a subsequent system power on.

If V_{CC} is applied within the timeout period, then the system power on sequence will continue as shown in intervals 2-5 in the timing diagram. During interval 2, $\overline{PWR}$ will remain active and $\overline{IRQ}$ will be driven to its active low level, indicating that either WF or KF was set in initiating the power on. In the diagram $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit will be automatically cleared to 0 in response to a successful power on. The $\overline{PWR}$ line will remain active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing zeroes to both of these control bits. As long as no other interrupt within the DS17885/DS17887 is pending, the $\overline{IRQ}$ line will be taken inactive once these bits are reset. Execution of the application software may proceed. During this time, both the wake up and kickstart functions may be used to

generate status and interrupts. WF will be set in response to a date, hours, minutes, and seconds match condition. KF will be set in response to a low going transition on $\overline{KS}$. If the associated interrupt enable bit is set (WIE and/or KSE) then the $\overline{IRQ}$ line will driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS17885/DS17887 may cause $\overline{IRQ}$ to be driven low. While system power is applied, the on chip logic will always attempt to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake up or kickstart.

The system may be powered down under software control by setting the PAB bit to a logic 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ}$ output pin will be placed in a high impedance state when V_{CC} goes below V_{PF}. If the system is to be again powered on in response to a wake up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and nonvolatile RAM is in effect and $\overline{IRQ}$ is tri-stated, and monitoring of wake up and kickstart takes place. If PRS=1, $\overline{PWR}$ stays active, otherwise if PRS=0 $\overline{PWR}$ is tri–stated.

RAM CLEAR

The DS17885/DS17887 provides a RAM clear function for the 114 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V_{CC} pin.

The RAM clear function is enabled or disabled via the RAM Clear Enable bit (RCE; bank 1, register 04BH). When this bit is set to a logic 1, the 114 bytes of user RAM will be cleared (all bits set to 1) when an active low transition is sensed on the $\overline{RCLR}$ pin. This action will have no effect on either the clock/calendar settings or upon the contents of the extended RAM. The RAM clear Flag (RF, bank 1, register 04AH) will be set when the RAM clear operation has been completed. If V_{CC} is present at the time of the RAM clear and RIE=1, the $\overline{IRQ}$ line will also be driven low upon completion. The interrupt condition can be cleared by writing a zero to the RF bit. The $\overline{IRQ}$ line will then return to its inactive high level provided there are no other pending interrupts. Once the $\overline{RCLR}$ pin is activated, all read/write accesses are locked out for a minimum recover time, specified as t_{REC} in the Electrical Characteristics section.

When RCE is cleared to zero, the RAM clear function is disabled. The state of the $\overline{RCLR}$ pin will have no effect on the contents of the user RAM, and transitions on the $\overline{RCLR}$ pin have no effect on RF.

EXTENDED CONTROL REGISTERS

Two extended control registers are provided to supply controls and status information for the extended features offered by the DS17885/DS17887. These are designated as extended control registers A and B and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows.

EXTENDED CONTROL REGISTER 4A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	BME	*	PAB	RF	WF	KF

VRT2 - This status bit gives the condition of the auxiliary battery. It is set to a logic 1 condition when the external lithium battery is connected to the V_{BAUX}. If this bit is read as a logic 0, the external battery should be replaced.

INCR - Increment in Progress status bit. This bit is set to a 1 when an increment to the time/date registers is in progress and the alarm checks are being made. INCR will be set to a 1 at 122 µs before the update cycle starts and will be cleared to 0 at the end of each update cycle.

BME – Burst Mode Enable. The burst mode enable bit allows the extended user RAM address registers to automatically increment for consecutive reads and writes. When BME is set to a logic one, the automatic incrementing will be enabled and when BME is set to a logic zero, the automatic incrementing will be disabled.

PAB - Power Active Bar control bit. When this bit is 0, the $\overline{PWR}$ pin is in the active low state. When this bit is 1, the $\overline{PWR}$ pin is in the high impedance state. This bit can be written to a logic 1 or 0 by the user. If either WF AND WIE = 1 OR KF AND KSE = 1, the PAB bit will be cleared to 0.

RF - Ram Clear Flag. This bit will be set to a logic 1 when a high to low transition occurs on the $\overline{RCLR}$ input if RCE=1. The RF bit is cleared by writing it to a logic 0. This bit can also be written to a logic 1 to force an interrupt condition.

WF - Wake up Alarm Flag - This bit is set to 1 when a wake up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

KF - Kickstart Flag - This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

EXTENDED CONTROL REGISTER 4B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32K	CS	RCE	PRS	RIE	WIE	KSE

ABE - Auxiliary Battery Enable. This bit when written to a logic 1 will enable the V_{BAUX} pin for extended functions.

E32K - Enable 32.768 KHz output. This bit when written to a logic 1 will enable the 32.768 KHz oscillator frequency to be output on the SQW pin. E32K is set to a one when V_{CC} is powered up.

CS – Crystal Select Bit. When CS is set to a 0, the oscillator is configured for operation with a crystal that has a 6 pF specified load capacitance. When CS=1, the oscillator is configured for a 12.5 pF crystal.

RCE - RAM Clear Enable bit. When set to a 1, this bit enables a low level on $\overline{RCLR}$ to clear all 114 bytes of user RAM. When RCE = 0, $\overline{RCLR}$ and the RAM clear function are disabled.

PRS – PAB Reset Select Bit. When set to a 0 the $\overline{PWR}$ pin will be set hi–Z when the DS17885 goes into power fail. When set to a 1, the $\overline{PWR}$ pin will remain active upon entering power fail.

RIE - Ram Clear Interrupt Enable. When RIE is set to a 1, the $\overline{IRQ}$ pin will be driven low when a RAM clear function is completed.

WIE - Wake Up Alarm Interrupt Enable. When V_{CC} voltage is absent and WIE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a wake up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If WIE is set while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to WF being set to 1. When WIE is cleared to a 0, the WF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

KSE - Kickstart Interrupt Enable. When V_{CC} voltage is absent and KSE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If KSE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to KF being set to 1. When KSE is cleared to a 0, the KF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

* Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no effect on operation.

SYSTEM MAINTENANCE INTERRUPT (SMI) RECOVERY STACK

An SMI recovery register stack is located in the extended register bank, locations 4Eh and 4Fh. This register stack, shown below, can be used by the BIOS to recover from an SMI occurring during an RTC read or write.

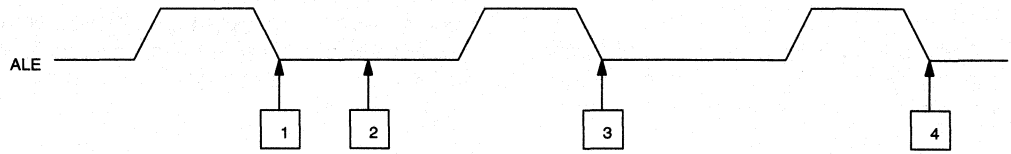
	RTC ADDRESS
	RTC ADDRESS – 1
4Eh	RTC ADDRESS – 2
4Fh	RTC ADDRESS – 3

SMI RECOVERY STACK

7	6	5	4	3	2	1	0
DV0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

REGISTER BIT DEFINITION

The RTC address is latched on the falling edge of the ALE signal. Each time an RTC address is latched, the register address stack is pushed. The stack is only four registers deep, holding the three previous RTC addresses in addition to the current RTC address being accessed. The following waveform illustrates how the BIOS could recover the RTC address when an SMI occurs.



1. The RTC address is latched.
2. An SMI is generated before an RTC read or write occurs.
3. RTC address 0Ah is latched and the address from "1" is pushed to the "RTC Address – 1" stack location. This step is necessary to change the bank select bit, DV0=1.
4. RTC address 4Eh is latched and the address from "1" is pushed to location 4Eh, "RTC Address – 2" while 0Ah is pushed to the "RTC Address – 1" location. The data in this register, 4Eh, is the RTC address lost due to the SMI.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature DS17885	–55°C to +125°C
Storage Temperature DS17887	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage 5 Volt Operation	V_{CC}	4.5	5.0	5.5	V	1
Power Supply Voltage 3 Volt Operation	V_{CC}	2.7	3.0	3.3	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		0.6	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	1
Auxiliary Battery Voltage	V_{BAUX}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		25	50	mA	2, 3
CMOS Standby Current ($\overline{CS}$=V_{CC}-0.2V)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
Output Leakage Current	I_{OL}	–1		+1	µA	6
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Power Fail Trip Point	V_{PF}	4.25	4.37	4.5	V	4
Battery Switch Voltage	V_{SW}		V_{BAT}, V_{BAUX}		V	9

DC ELECTRICAL CHARACTERISTICS (cont'd) (0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Leakage OSC ON	I_{BAT1}		0.50	1.5	µA	12
Battery Leakage OSC OFF	I_{BAT2}		0.050	1.0	µA	12
I/O Leakage	I_{LO}	–1		+1	µA	5
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			10.0	mA	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=3.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		15	30	mA	2, 3
CMOS Standby Current ($\overline{CS}$=V_{CC}-0.2)	I_{CC2}		0.5	2	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
Output Leakage Current	I_{OL}	–1		+1	µA	6
Output Logic 1 Voltage @ 0.4 mA	V_{OH}	2.4			V	
Output Logic 0 Voltage @ 0.8 mA	V_{OL}			0.4	V	
Power Fail Trip Point	V_{PF}	2.5	2.6	2.7	V	4
Battery Leakage OSC ON	I_{BAT1}		0.50	1.5	µA	12
Battery Leakage OSC OFF	I_{BAT2}		0.050	1.0	µA	12
I/O Leakage	I_{LO}	–1		+1	µA	5
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			4	mA	1

RTC AC TIMING CHARACTERISTICS

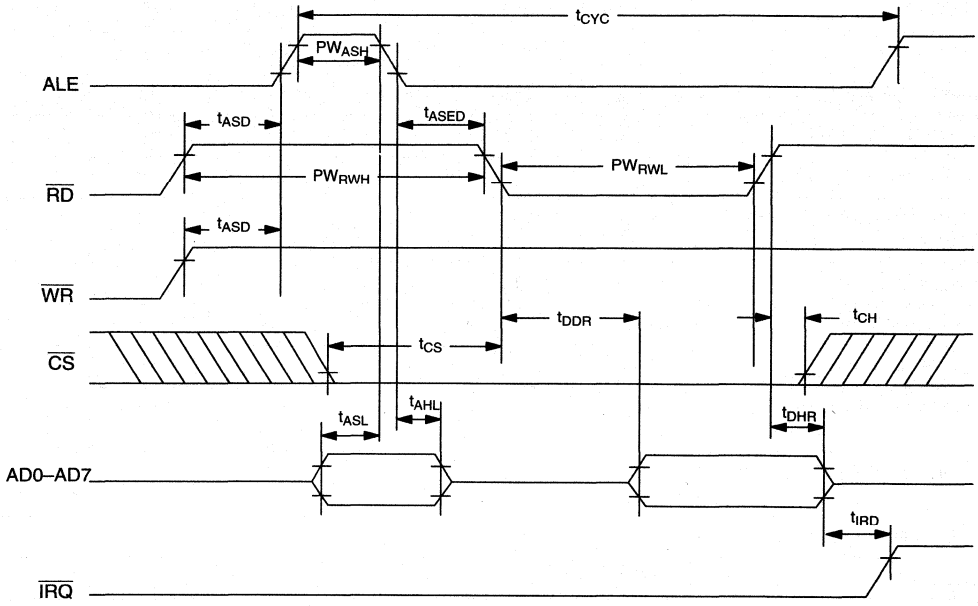
(0°C to 70°C; V_{CC} = 3.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	915		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{RWL}	375			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{RWH}	450			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	75			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		120	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	90			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	30			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	30			ns	
Pulse Width ALE High	PW_{ASH}	180			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	120			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		370	ns	7
Data Setup Time	t_{DSW}	180			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

AC TEST CONDITIONS

Output Load: 50 pF
Input Pulse Levels: 0–3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS17885/DS17887 BUS TIMING FOR READ CYCLE TO RTC

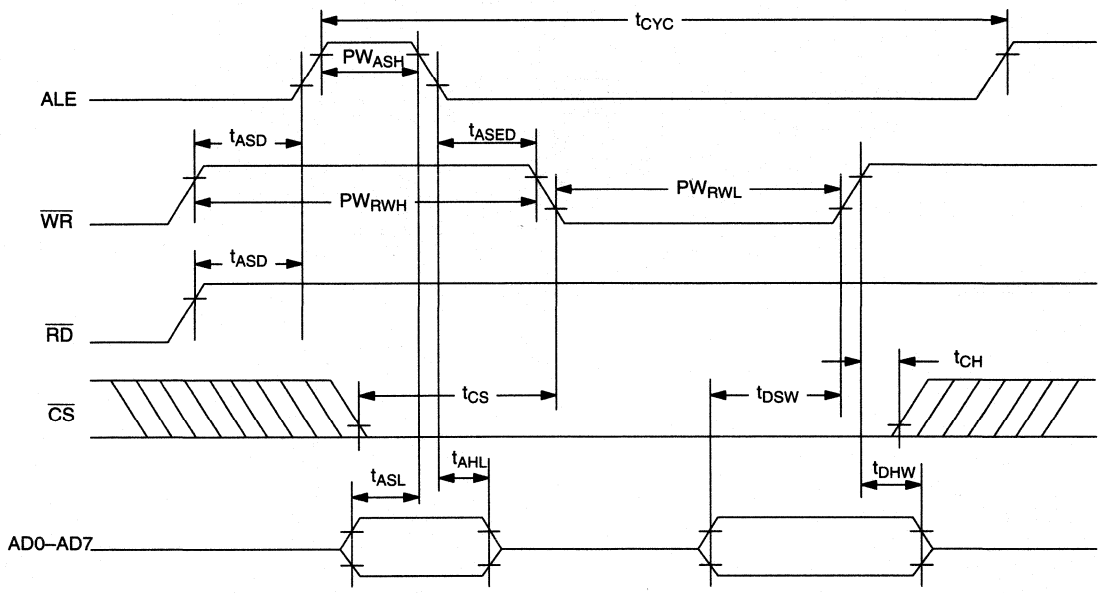


RTC AC TIMING CHARACTERISTICS

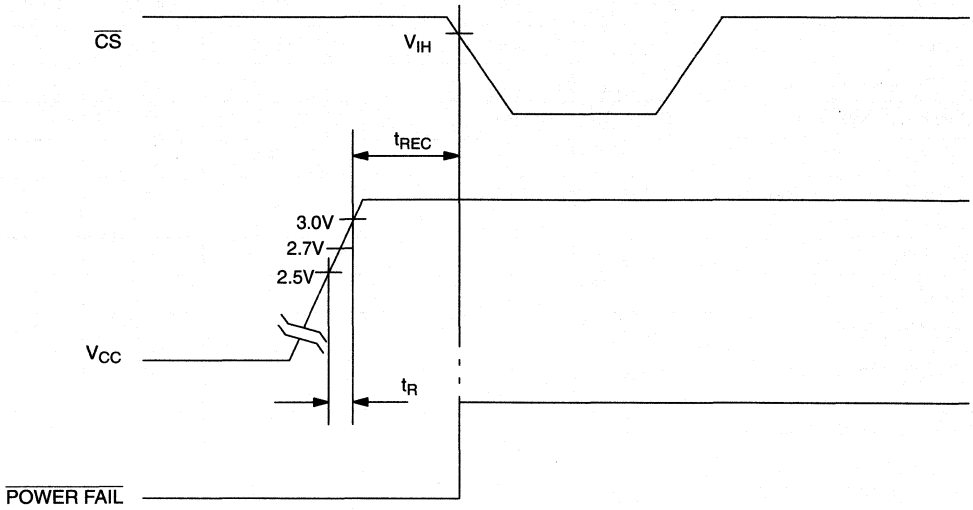
(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{RWL}	125			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{RWH}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	7
Data Setup Time	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

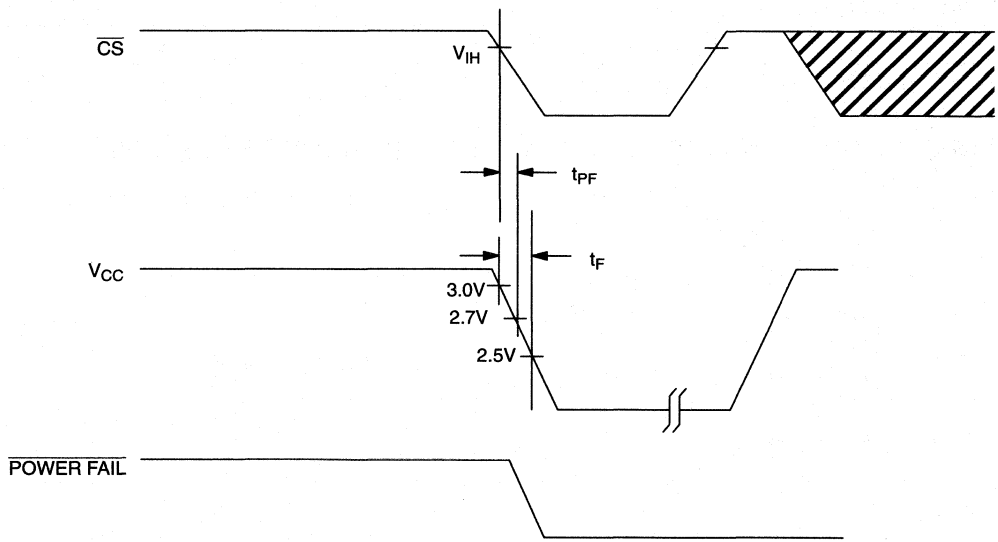
DS17885/DS17887 BUS TIMING FOR WRITE CYCLE TO RTC AND RTC REGISTERS



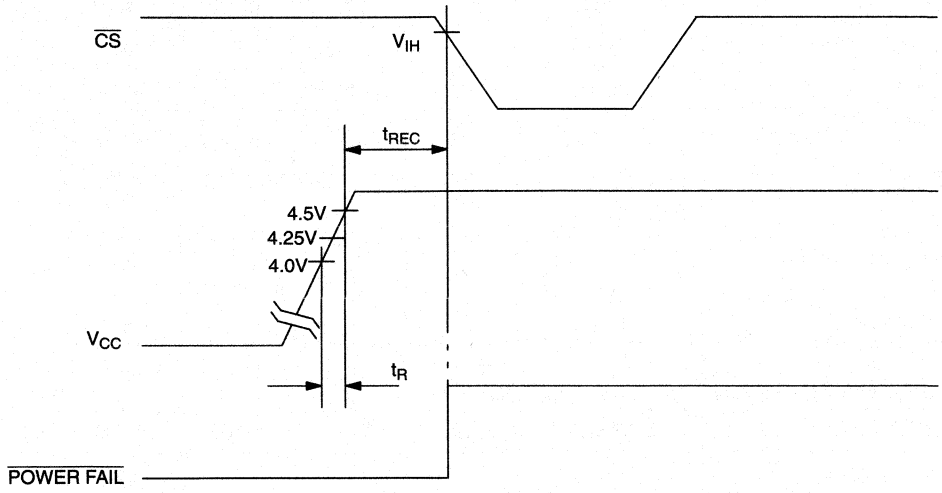
POWER–UP CONDITION 3 VOLT DEVICE



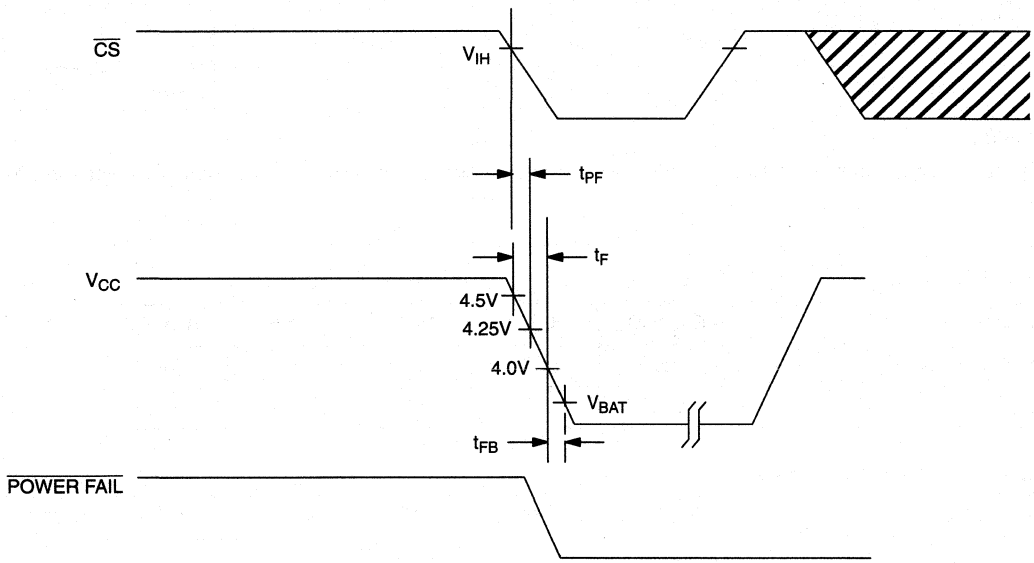
POWER–DOWN CONDITION 3 VOLT DEVICE



POWER–UP CONDITION 5.0 VOLT DEVICE



POWER–DOWN CONDITION 5.0 VOLT DEVICE



POWER-UP POWER-DOWN TIMING 5 VOLT DEVICE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	10, 11

POWER-UP POWER-DOWN TIMING 3 VOLT DEVICE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $2.5 \le V_{CC} \le 3.0V$	300			µs	
V_{CC} Slew Rate Power Up	t_R $3.0V \ge V_{CC} \ge 2.5V$	0			µs	
Expected Data Retention	t_{DR}	10			years	10, 11

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

(t_A = 25°C)

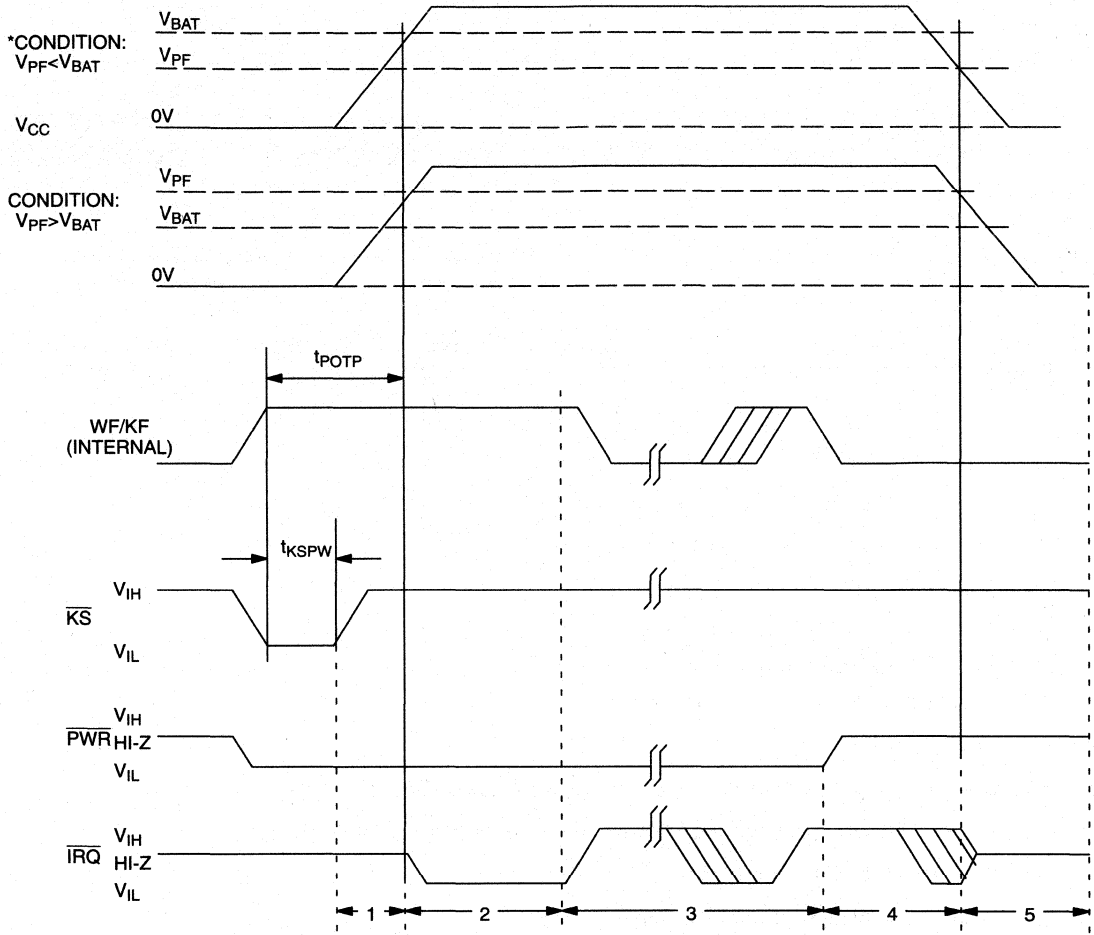
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

WAKE UP/KICKSTART TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t_{KSPW}	2			µs	
Wake up/Kickstart Power On Timeout	t_{POTO}	2			seconds	8

WAKE UP/KICKSTART TIMING

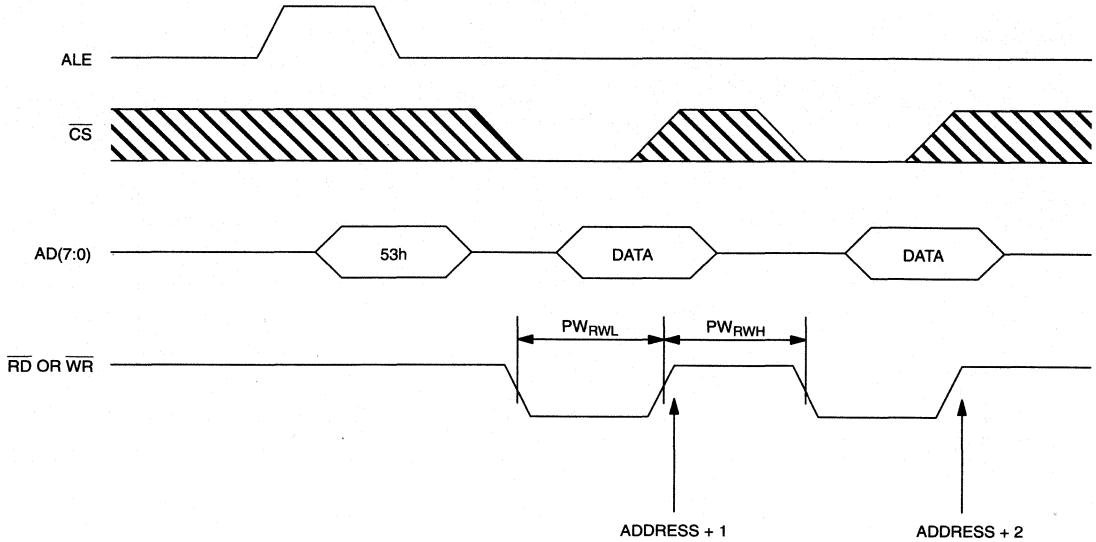


NOTE:

Time intervals shown above are referenced in Wake up/Kickstart section.

* This condition can occur with the 3 volt device.

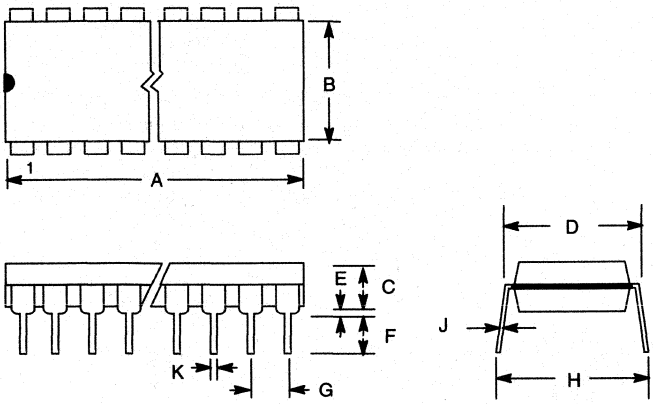
BURST MODE TIMING WAVEFORM



NOTES:

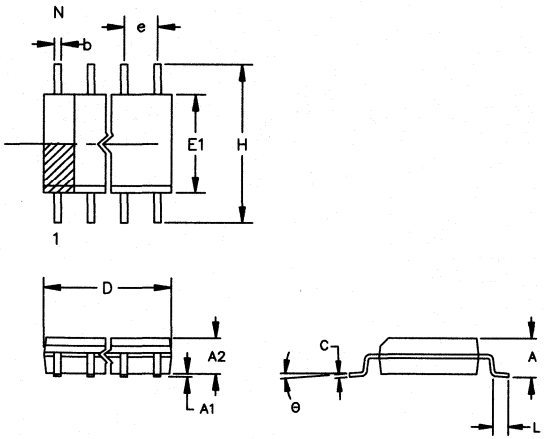
1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Write protection trip point occurs during power fail prior to switchover from V_{CC} to V_{BAT}.
5. Applies to the AD0–AD7 pins, and the SQW pin when each is in a high impedance state.
6. The $\overline{IRQ}$ and $\overline{PWR}$ pins are open drain.
7. Measured with a load of 50 pF + 1 TTL gate.
8. Wakeup kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.
9. V_{SW} is determined by the larger of V_{BAT} and V_{BAUX}.
10. The DS17887 will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
11. t_{DR} is the amount of time that the internal battery can power the internal oscillator and internal registers of the DS17887.
12. I_{BAT1} and I_{BAT2} are measured at V_{BAT} = 3.5V.

DS17885 24–PIN DIP



PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	1.245 31.62	1.270 32.25
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.380	0.050 1.27
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.625 15.88	0.675 17.15
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

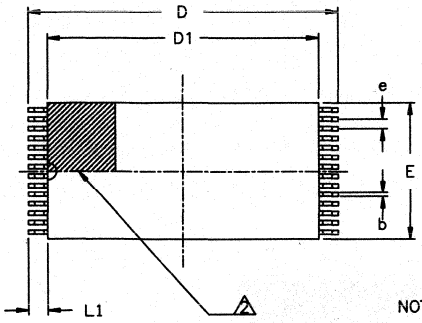
DS17885 24–PIN SOIC



The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

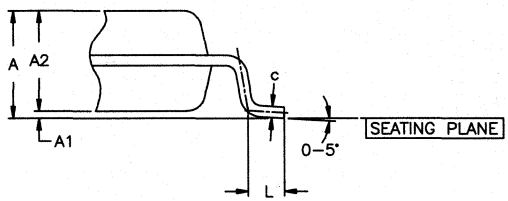
PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33
D IN. MM	0.598 15.19	0.612 15.54
e IN. MM	.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02
Θ	0°	8°

DS17885 28–PIN TSOP



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT ONE HALF OF ITS AREA MUST BE LOCATED WITHIN THE ZONE INDICATED.

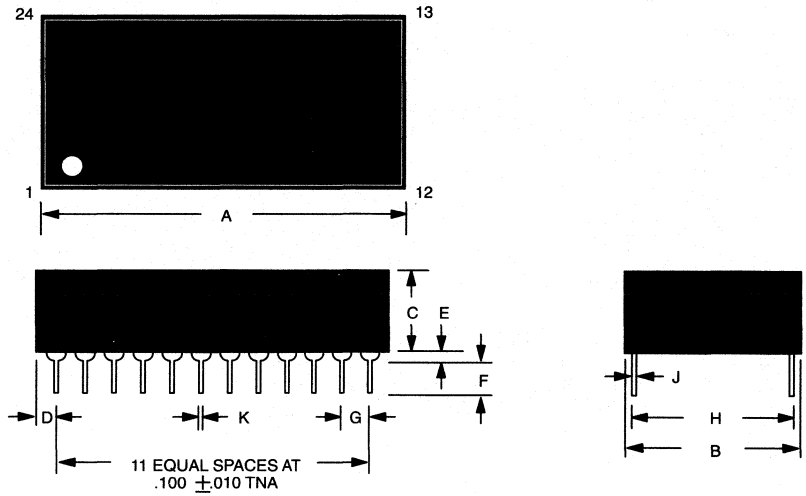


DETAIL A

PKG	28-PIN	
DIM	MIN	MAX
A	–	1.20
A1	0.05	–
A2	0.91	1.02
b	0.18	0.27
c	0.15	0.20
D	13.20	13.60
D1	11.70	11.90
E	7.90	8.10
e	0.55 BSC	
L	0.30	0.70
L1	0.80 BSC	

56–G5003–000

DS17887 REAL TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.720 18.29	0.740 18.80
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

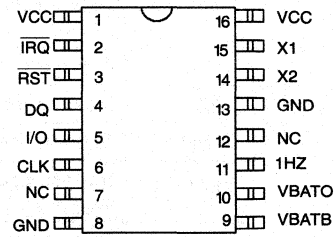
DS2404
EconoRAM Time Chip

3

FEATURES

- Unique 1-wire interface requires only one port pin for communication
- Contains real-time clock/calendar in binary format
- 4096 bits of SRAM organized in 16 pages, 256 bits per page
- Interval timer can automatically accumulate time when power is applied
- Programmable cycle counter can accumulate the number of system power-on/off cycles
- Programmable alarms can be set to generate interrupts for interval timer, real-time clock, and/or cycle counter
- Write protect feature provides tamper-proof time data
- Programmable expiration date that will limit access to SRAM and timekeeping
- Data integrity assured with strict read/write protocols
- 3-wire I/O available for high speed data communications
- Unique 64-bit factory lasered ROM available
- Space-saving 16-pin SOIC and SSOP packages
- Operating temperature range from -40°C to +85°C
- Operating voltage range from 2.8 to 5.5 Volts

PIN ASSIGNMENT



16–PIN DIP (.300 Mil)
16 PIN SOIC (300 Mil)
16–PIN SSOP

PIN DESCRIPTION

V_{CC}	–	2.8 to 5.5 Volts
$\overline{IRQ}$	–	Interrupt Output
$\overline{RST}$	–	3-Wire Reset Input
DQ	–	3-Wire Input/Output
I/O	–	1-Wire Input/Output
CLK	–	3-Wire Clock Input
NC	–	No Connection
GND	–	Ground
V_{BATB}	–	Battery Backup Input
V_{BATO}	–	Battery Operate Input
1 Hz	–	1 Hz Output
X_1, X_2	–	Crystal Connections

ORDERING INFORMATION

DS2404	16–pin DIP
DS2404S	16–pin SOIC
DS2404B	16–pin SSOP

DESCRIPTION

The DS2404 EconoRAM Time Chip offers a simple solution for storing and retrieving vital data and time information with minimal hardware. The DS2404 contains a unique lasered ROM, real-time clock/calendar, interval timer, cycle counter, programmable interrupts and 4096 bits of SRAM. Two separate ports are provided for communication, 1-wire and 3-wire. Using the 1-wire port, only one pin is required for communication, and the lasered ROM can be read even when the DS2404 is without power. The 3-wire port provides high speed communication using the traditional Dallas Semiconductor 3-wire interface. With either interface, a strict protocol for accessing the DS2404 insures data integrity. Utilizing backup energy sources, the data is nonvolatile and allows for stand-alone operation.

The DS2404 features can be used to create a stopwatch, alarm clock, time and date stamp, logbook, hour meter, calendar, system power cycle timer, expiration timer, and event scheduler.

DETAILED PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1, 16	V_{CC}	**Power input pins** for V_{CC} operate mode. 2.8 to 5.5 volts operation. Either pin can be used for V_{CC}. Only one is required for normal operation. (See V_{BATO} pin description and "Power Control" section).
2	$\overline{IRQ}$	**Interrupt output pin:** Open drain.
3	$\overline{RST}$	**Reset input pin** for 3-wire operation. (See "Parasite Power" section.)
4	DQ	**Data input/output pin** for 3-wire operation.
5	I/O	**Data input/output** for 1-wire operation: Open drain. (See "Parasite Power" section.)
6	CLK	**Clock input pin** for 3-wire operation.
7, 12	NC	**No connection pins.**
8, 13	GND	**Ground pin:** Either pin can be used for ground.
9	V_{BATB}	**Battery backup input pin:** Battery voltage can be 2.8 to 5.5 volts. (See V_{BATO} pin description and "Power Control" section.)
10	V_{BATO}	**Battery operate input pin** for 2.8 to 5.5 volt operation. The V_{CC} & V_{BATB} pins must be grounded when this pin is used to power the chip. (See "Power Control" section.)
11	1Hz	**1 Hz square wave output:** Open drain.
14, 15	X_1, X_2	**Crystal pins.** Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S (be sure to request 6 pF load capacitance). **NOTE:** X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area.

OVERVIEW

The DS2404 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) timekeeping registers. The timekeeping section utilizes an on-chip oscillator that is connected to an external 32.768 kHz crystal. The SRAM and timekeeping registers reside in one contiguous address space referred to hereafter as memory. All data is read and written least significant bit first.

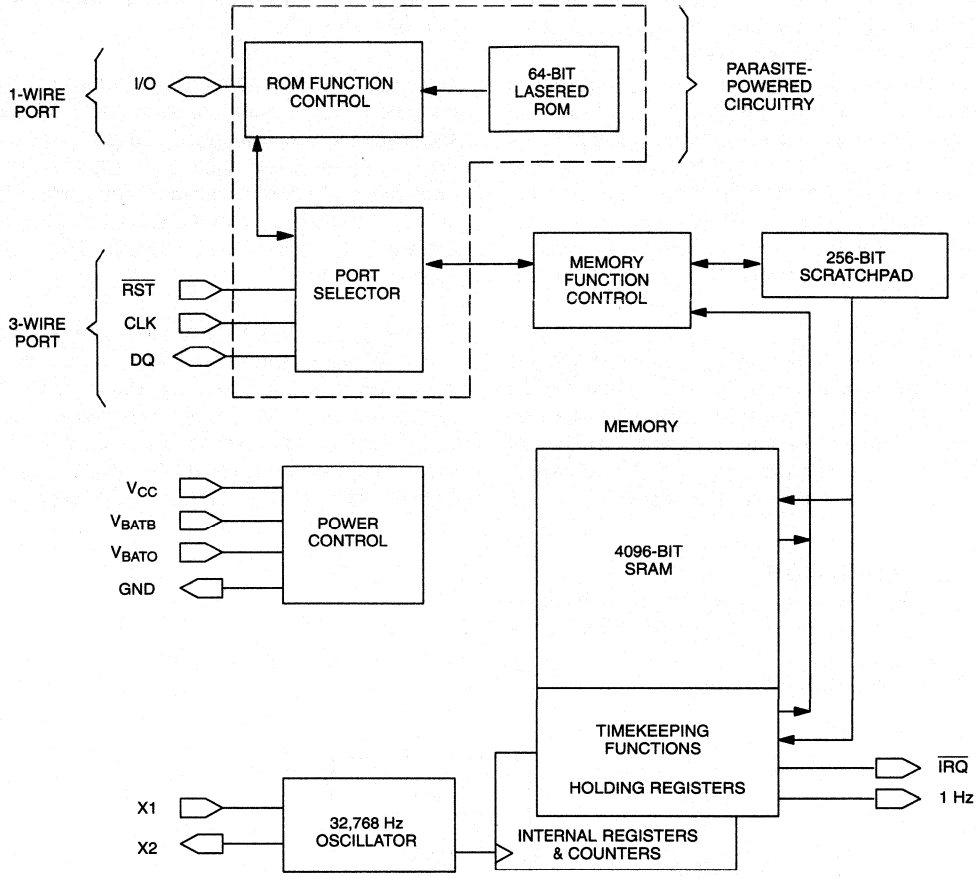
Two communication ports are provided, a 1-wire port and a 3-wire port. A port selector determines which of the two ports is being used. The communication ports and the ROM are parasite-powered via I/O, $\overline{RST}$, or V_{CC}. This allows the ROM to be read in the absence of power. The ROM data is accessible only through the 1-wire port. The scratchpad and memory are accessible via either port.

If the 3-wire port is used, the master provides one of four memory function commands: 1) read memory, 2) read scratchpad, 3) write scratchpad, or 4) copy scratchpad. The only way to write memory is to first write the scratchpad and then copy the scratchpad data to memory. (See Figure 6.)

If the 1-wire port is used, the memory functions will not be available until the ROM function protocol has been established. This protocol is described in the ROM functions flow chart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the master may then provide any one of the four memory function commands.

The "Power Control" section provides for two basic power configurations, battery operate mode and V_{CC} operate mode. The battery operate mode utilizes one supply connected to V_{BATO}. The V_{CC} operate mode may utilize two supplies; the primary supply connects to V_{CC} and a backup supply connects to V_{BATB}.

DS2404 BLOCK DIAGRAM Figure 1



COMMUNICATION PORTS

Two communication ports are provided, a 1–wire and a 3–wire port. The advantages of using the 1–wire port are as follows: 1) provides access to the 64–bit lasered ROM, 2) consists of a single communication signal (I/O), and 3) multiple devices may be connected to the 1–wire bus. The 1–wire bus has a maximum data rate of 16.6K bits/second and requires one 5KΩ external pullup.

The 3-wire port consists of three signals, $\overline{RST}$, CLK, and DQ. $\overline{RST}$ is an enable input, DQ is bidirectional serial data, and the CLK input is used to clock in or out the serial data. The advantages of using the 3-wire port are 1) high data transfer rate (2 MHz), 2) simple timing, and 3) no external pull-up required.

Port selection is accomplished on a first-come, first-serve basis. Whichever port comes out of reset first will obtain control. For the 3-wire port, this is done by bringing $\overline{RST}$ high. For the 1-wire port, this is done on the first falling edge of I/O after the reset and presence pulses. (See "1-Wire Signalling" section.)

PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the I/O, $\overline{RST}$, or V_{CC} pins are high. When using the 1–wire port in battery operate mode, $\overline{RST}$ and V_{CC} provide no power since they are low. However, I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off these pins, battery power is conserved and 2) the ROM may be read in absence of normal power. For instance, in battery-operate mode, if the battery fails, the ROM may still be read normally.

In battery-backed mode, if V_{CC} fails, the port switches in the battery but inhibits communication. In order to read the ROM, the parasite-powered circuitry must be allowed to power down. This may be done by insuring that I/O, $\overline{RST}$, and V_{CC} are all low for $\gg$1 s. The ROM may then be read normally over the 1-wire port.

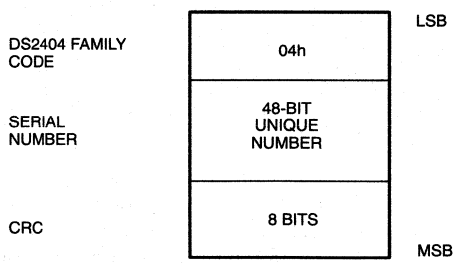
64-BIT LASERED ROM

Each DS2404 contains a unique ROM code that is 64 bits long. The first eight bits are a 1-wire family code (DS2404 code is 04h). The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 2.)

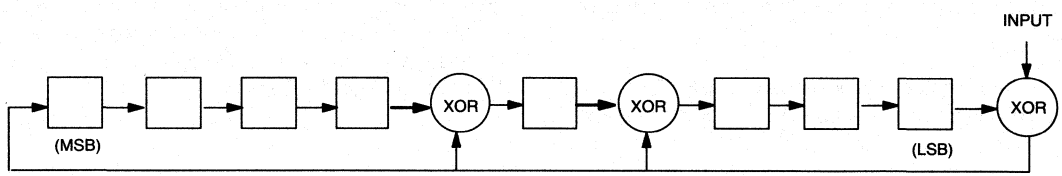
The 1-wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in an application note entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products".

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

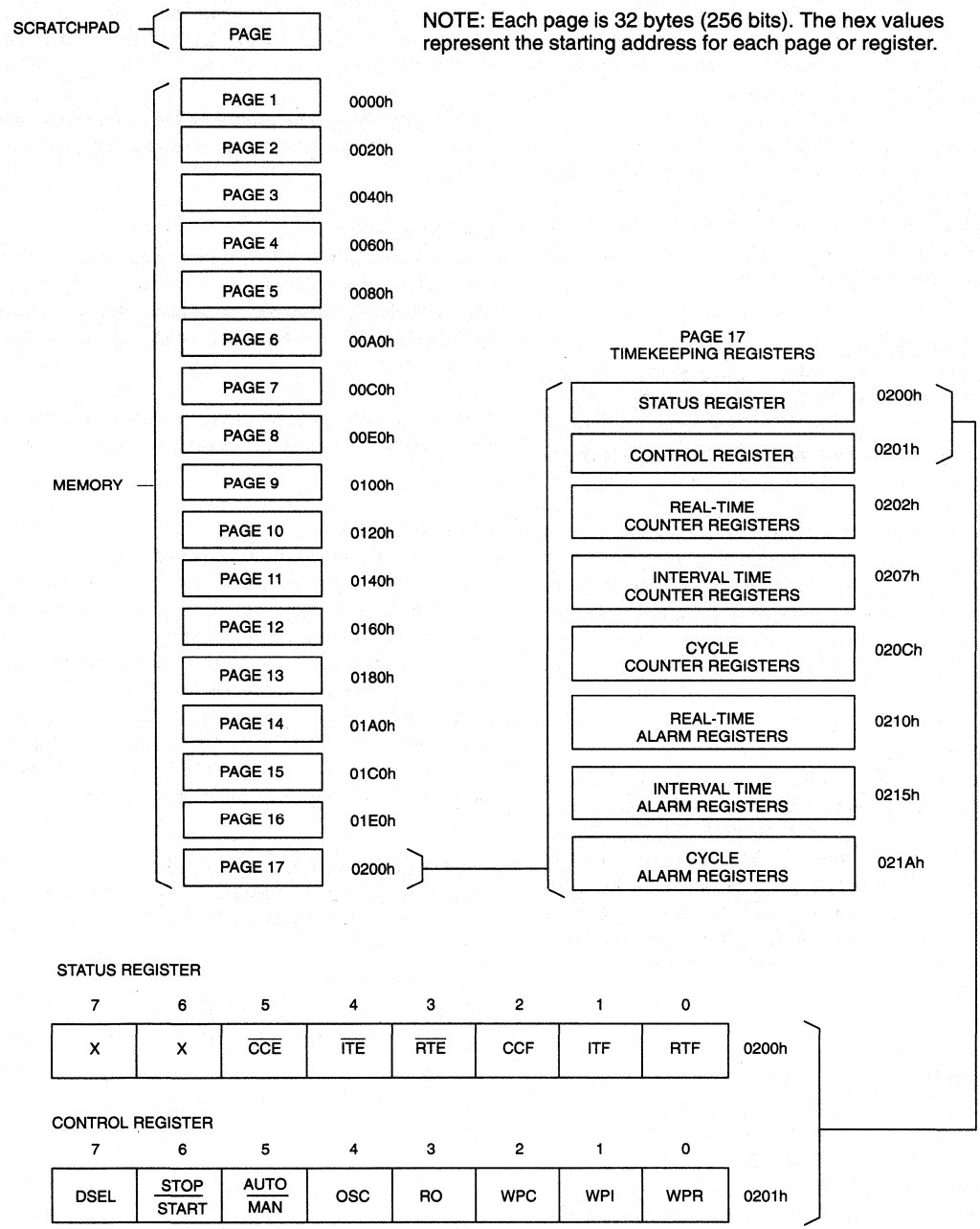
64-BIT LASERED ROM Figure 2



1-WIRE CRC CODE Figure 3



MEMORY MAP Figure 4



MEMORY

The memory map in Figure 4 shows a page (32 bytes) called the scratchpad and 17 pages called memory. Pages 1 through 16 each contain 32 bytes which make up the 4096-bit SRAM. Page 17 has only 30 bytes which contain the timekeeping registers.

The scratchpad is an additional page of memory that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process insures data integrity when modifying the memory.

TIMEKEEPING

A 32,768 Hz crystal oscillator is used as the time base for the timekeeping functions. The oscillator can be turned on or off by an enable bit in the control register. The oscillator must be on for the real time clock, interval timer, cycle counter and 1 Hz output to function.

The timekeeping functions are double buffered. This feature allows the master to read time or count without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers which the user accesses. This occurs after the eighth bit of the Read Memory Function command.

Real-Time Clock

The real-time clock is a 5-byte binary counter. It is incremented 256 times per second. The least significant byte is a count of fractional seconds. The upper four bytes are a count of seconds. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point which is determined by the user. For example, 12:00A.M., January 1, 1970 could be a reference point.

Interval Timer

The interval timer is a 5-byte binary counter. When enabled, it is incremented 256 times per second. The least significant byte is a count of fractional seconds. The interval timer can accumulate 136 years of seconds before rolling over. The interval timer has two modes of operation which are selected by the AUTO/$\overline{\text{MAN}}$ bit in the control register. In the auto mode, the interval timer will begin counting after the I/O line has been high for a period of time determined by the DSEL bit in the control register. Similarly, the interval timer will stop counting after the I/O line has been low for a period of time determined by the DSEL bit. In the manual mode, time accumulation is controlled by the STOP/$\overline{\text{START}}$ bit in the control register.

NOTE: For auto mode operation, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.

Cycle Counter

The cycle counter is a 4-byte binary counter. It increments after the falling edge of the I/O line if the appropriate I/O line timing has been met. This timing is selected by the DSEL bit in the control register. (See "Status/Control" section).

NOTE: For cycle counter operation, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.

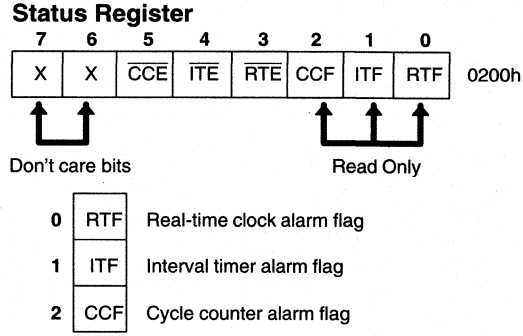
Alarm Registers

The alarm registers for the real-time clock, interval timer, and cycle counter all operate in the same manner. When the value of a given counter equals the value in its associated alarm register, the appropriate flag bit is set in the status register. If the corresponding interrupt enable bit(s) in the status register is set, an interrupt is generated. If a counter and its associated alarm register are write protected when an alarm occurs, access to the device becomes limited. (See "Status/Control", "Interrupts", and the "Programmable Expiration" sections.)

STATUS/CONTROL REGISTERS

The status and control registers are the first two bytes of page 17 (see "Memory Map", Figure 4).

Status Register



When a given alarm occurs, the corresponding alarm flag is set to a logic 1. The alarm flag(s) is cleared by reading the status register.

3	$\overline{RTE}$	Real-time interrupt enable
4	$\overline{ITE}$	Interval timer interrupt enable
5	$\overline{CCE}$	Cycle counter interrupt enable

Writing any of the interrupt enable bits to a logic 0 will allow an interrupt condition to be generated when its corresponding alarm flag is set (see "Interrupts" section).

Control Register

7	6	5	4	3	2	1	0	
DSEL	STOP/$\overline{START}$	AUTO/$\overline{MAN}$	OSC	RO	WPC	WPI	WPR	0201h

0	WPR	Write protect real-time clock/alarm registers
1	WPI	Write protect interval timer/alarm registers
2	WPC	Write protect cycle counter/alarm registers

Setting a write protect bit to a logic 1 will permanently write protect the corresponding counter and alarm registers, all write protect bits, and additional bits in the control register. The write protect bits can not be written in a normal manner (see "Write Protect/Programmable Expiration" section).

3	RO	Read Only

If a programmable expiration occurs and the read only bit is set to a logic 1, then the DS2404 becomes read only. If a programmable expiration occurs and the read only bit is a logic 0, then only the 64-bit lasered ROM can be accessed (see "Write Protect/Programmable Expiration" section).

4	OSC	Oscillator Enable

This bit controls the crystal oscillator. When set to a logic 1, the oscillator will start operation. When the oscillator bit is a logic 0, the oscillator will stop.

5	AUTO/$\overline{MAN}$	Automatic/$\overline{Manual}$ Mode

When this bit is set to a logic 1, the interval timer is in automatic mode. In this mode, the interval timer is enabled by the I/O line. When this bit is set to a logic 0, the interval timer is in manual mode. In this mode the interval timer is enabled by the STOP/$\overline{START}$ bit.

6	STOP/$\overline{START}$	Stop/$\overline{Start}$ (in Manual Mode)

If the interval timer is in manual mode, the interval timer will start counting when this bit is set to a logic 0 and will stop counting when set to a logic 1. If the interval timer is in automatic mode, this bit has no effect.

7	DSEL	Delay Select Bit

This bit selects the delay that it takes for the cycle counter and the interval timer (in auto mode) to see a transition on the I/O line. When this bit is set to a logic 1, the delay time is 123 ± 2 ms. This delay allows communication on the I/O line without starting or stopping the interval timer and without incrementing the cycle counter. When this bit is set to a logic 0, the delay time is 3.5 ± 0.5 ms.

MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the memory. Two examples follow the flowchart. Three address registers are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status byte (E/S).

The target address points to a unique byte location in memory. The first five bits of the target address (T4:T0) represent the byte offset within a page. This byte offset points to one of 32 possible byte locations within a given page. For instance, 00000b points to the first byte of a page where as 11111b would point to the last byte of a page.

The third register (E/S) is a read only register. The first five bits (E4: E0) of this register are called the ending offset. The ending offset is a byte offset within a page (1 of 32 bytes). Bit 5 (PF) is the partial byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

ADDRESS REGISTERS Figure 5

	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	OF	PF	E4	E3	E2	E1	E0

Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the user must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) will be set and the remaining data will be ignored. If the user writes an incomplete byte and an overflow has not occurred, the partial byte flag (PF) will be set.

Read Scratchpad Command [AAh]

This command may be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user may begin reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The user may read data until the end of the scratchpad after which the data read will be all logic 1's.

Copy Scratchpad [55h]

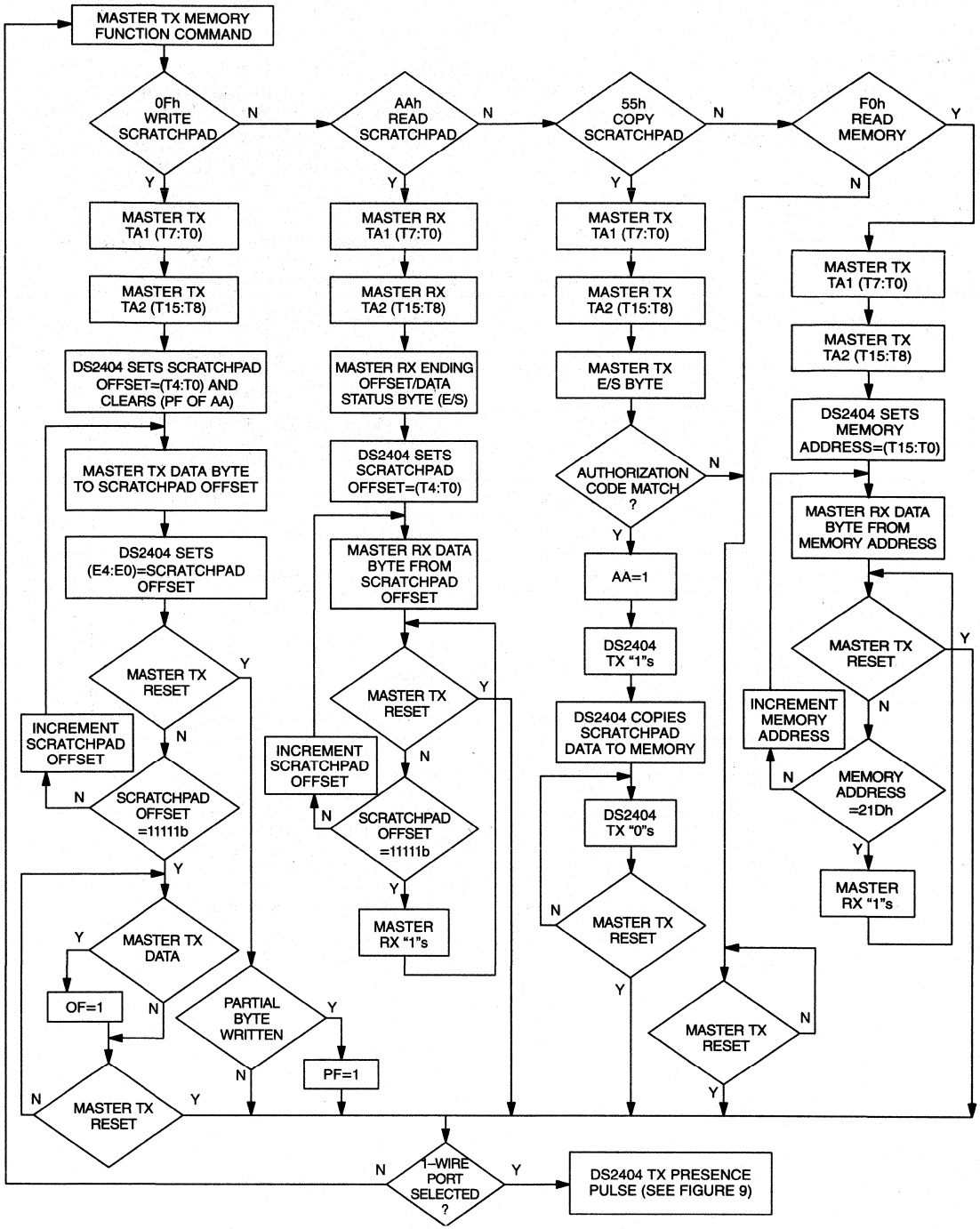
This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-byte authorization pattern. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. At this point, the part will go into a T_X mode, transmitting a logic 1 to indicate the copy is in progress. A logic 0 will be transmitted after the data has been copied. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30 µs.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 2 to 32 bytes may be copied to memory with this command. Whole bytes are copied even if only partially written. The AA flag will be cleared only by executing a write scratchpad command.

Read Memory [F0h]

The read memory command may be used to read the entire memory. After issuing the command, the user must provide the 2-byte target address. After the two bytes, the user reads data beginning from the target address and may continue until the end of page 17. After the end of page 17, logic 1's will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

MEMORY FUNCTION FLOW CHART Figure 6



MEMORY FUNCTION EXAMPLES

Example 1: Write one page of data to page 16
Read page 16 (3-wire port)

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Master pulses $\overline{RST}$ low
TX	0Fh	Issue "write scratchpad" command
TX	E0h	TA1, beginning offset=0
TX	01h	TA2, address=01E0h
TX	<32 data bytes>	Write 1 page of data to scratchpad
TX	Reset	Master pulses $\overline{RST}$ low
TX	AAh	Issue "read scratchpad" command
RX	E0h	Read TA1, beginning offset=0
RX	01h	Read TA2, address=01E0h
RX	1Fh	Read E/S, ending offset=31d, flags=0
RX	<32 data bytes>	Read scratchpad data and verify
TX	Reset	Master pulse $\overline{RST}$ low
TX	55h	Issue "copy scratchpad" command
TX	E0h	TA1 } AUTHORIZATION CODE
TX	01h	TA2 } AUTHORIZATION CODE
TX	1Fh	E/S } AUTHORIZATION CODE
RX	<busy indicator>	Wait until DQ=0 (~30 µs typical)
TX	Reset	Master pulse $\overline{RST}$ low
TX	F0h	Issue "read memory" command
TX	E0h	TA1, beginning offset=0
TX	01h	TA2, address=01E0h
RX	<32 data bytes>	Read memory page 16 and verify
TX	Reset	Master pulse $\overline{RST}$ low, done

Example 2: Write two data bytes to memory locations 0026h and 0027h (the seventh and eighth bytes of page 2). Read entire memory (1-wire port).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	0Fh	Issue "write scratchpad" command
TX	26h	TA1, beginning offset=6
TX	00h	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	AAh	Issue "read scratchpad" command
RX	26h	Read TA1, beginning offset=6
RX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7, flags=0
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	55h	Issue "copy scratchpad" command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
RX	<busy indicator>	Wait until 0
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	F0h	Issue "read memory" command
TX	00h	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX	<542 bytes>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

WRITE PROTECT/PROGRAMMABLE EXPIRATION

The write protect bits (WPR, WPI, WPC) provide a means of write protecting the timekeeping data and limiting access to the DS2404 when an alarm occurs (programmable expiration).

The write protect bits may not be written by performing a single copy scratchpad command. Instead, to write these bits, the copy scratchpad command must be performed three times. Please note that the AA bit will set, as expected, after the first copy command is successfully executed. Therefore, the authorization pattern for the second and third copy command should have this bit set. The read scratchpad command may be used to verify the authorization pattern.

The write protect bits, once set, permanently write protects their corresponding counter and alarm registers, all write protect bits, and certain control register bits as shown in Figure 7. The time/count registers will continue to count if the oscillator is enabled. If the user wishes to set more than one write protect bit, the user must set them at the same time. Once a write protect bit is set it cannot be undone, and the remaining write protect bits, if not set, cannot be set.

The programmable expiration takes place when one or more write protect bits have been set and a corresponding alarm occurs. If the RO (read only) bit is set, only the read scratch and read memory function commands are available. If the RO bit is a logic "0", no memory function commands are available. The ROM functions are always available.

WRITE PROTECT CHART Figure 7

WRITE PROTECT BIT SET:	WPR	WPI	WPC
Data Protected from User Modification:	Real Time Clock Real Time Alarm WPR WPI WPC RO OSC*	Interval Timer Interval Time Alarm WPR WPI WPC RO OSC* STOP/$\overline{\text{START}}$** AUTO/$\overline{\text{MAN}}$	Cycle Counter Cycle Counter Alarm WPR WPI WPC RO OSC* DSEL

* Becomes write "1" only, i.e., once written to a logic "1", may not be written back to a logic "0".
** Forced to a logic "0".

1-WIRE BUS SYSTEM

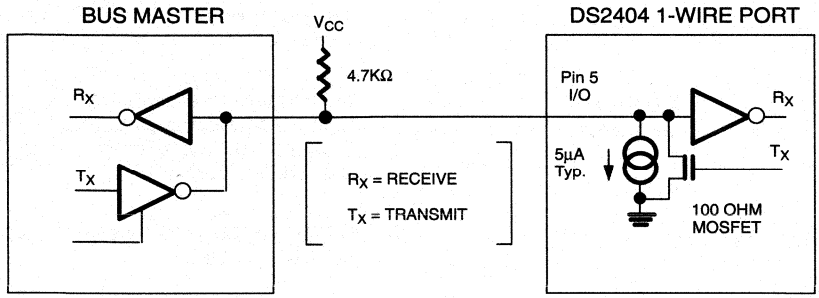
The 1-wire bus is a system which has a single bus master and one or more slaves. In most instances the DS2404 behaves as a slave. The exception is when the DS2404 generates an interrupt due to a timekeeping alarm. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-wire signalling (signal types and timing).

HARDWARE CONFIGURATION

The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain or 3-state outputs. The 1-wire port of the DS2404 (I/O pin 5) is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-wire bus with multiple slaves attached. The 1-wire bus requires a pull-up resistor of approximately 5KΩ.

The idle state for the 1-wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µS, all components on the bus will be reset.

HARDWARE CONFIGURATION Figure 8



TRANSACTION SEQUENCE

The protocol for accessing the DS2404 via the 1-wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2404 is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

Read ROM [33h]

This command allows the bus master to read the DS2404's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2404 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result).

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2404 on a multidrop bus. Only the DS2404 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wire-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus.

Example of a ROM Search

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1	00110101...
ROM2	10101010...
ROM3	11110101...
ROM4	00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.

2. The bus master will then issue the search ROM command on the 1-wire bus.

3. The bus master reads a bit from the 1-wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 0 onto the 1-wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1-wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the search ROM data command is being executed, all of the devices on the 1-wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 1 onto the 1-wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1-wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-wire bus that have a 0 in the first position and others that have a 1.

   The data obtained from the two reads of the 3-step routine have the following interpretations:

   00 - There are still devices attached which have conflicting bits in this position.

   01 - All devices still coupled have a 0 bit in this bit position.

   10 - All devices still coupled have a 1 bit in this bit position.

   11 - There are no devices attached to the 1-wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.

5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.

6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.

7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.

8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.

9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-wire bus.

10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.

11. The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.

12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.

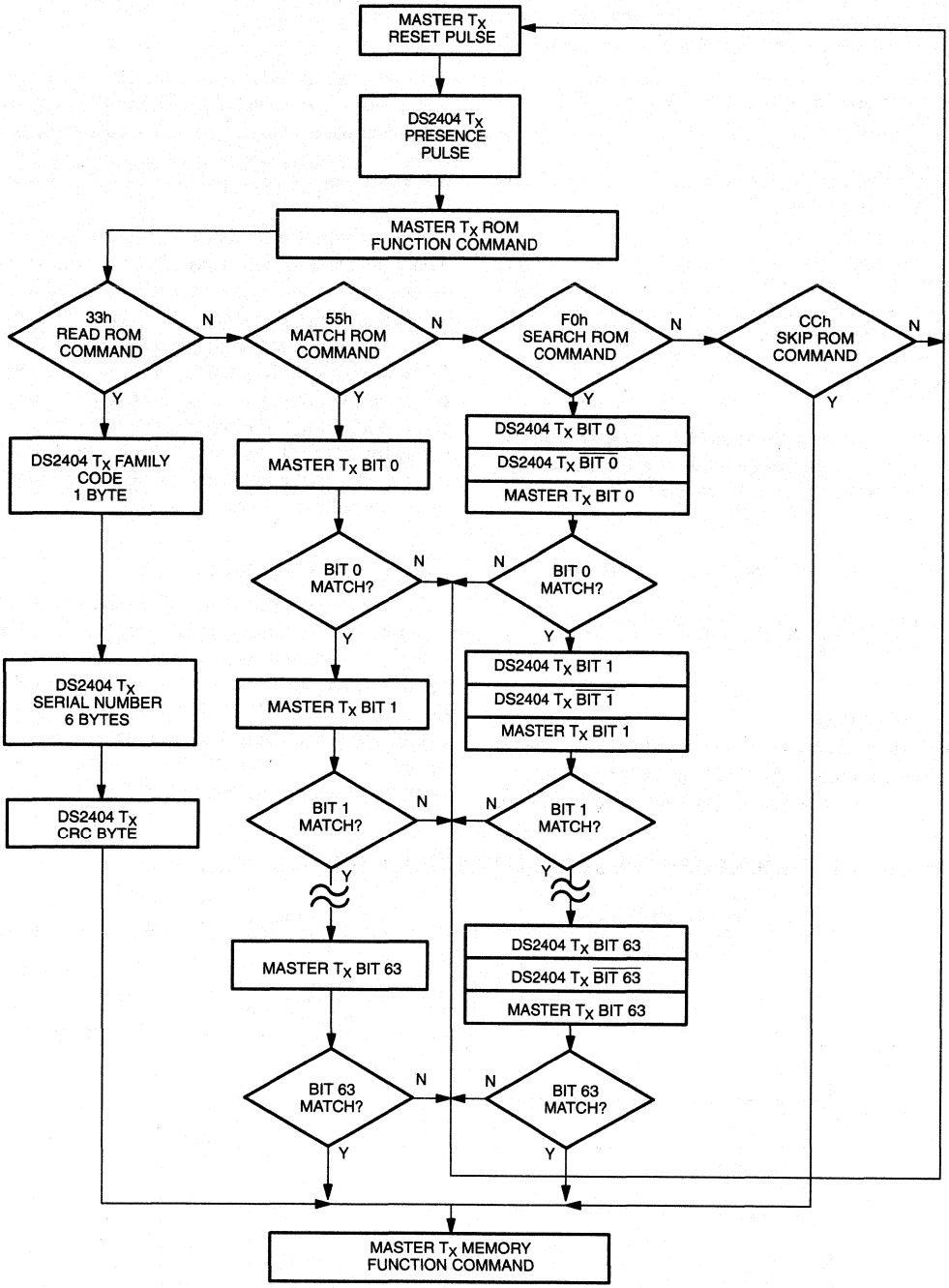
13. The bus master starts a new ROM search by repeating steps 1 through 3.

14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.

15. The bus master executes two read time slots and receives two zeros.

16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.

ROM FUNCTIONS FLOW CHART (1-WIRE PORT ONLY) Figure 9



17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.

18. The bus master starts a new ROM search by repeating steps 13 through 15.

19. The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.

20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

$$960\ \mu s + (8 + 3 \times 64)\ 61\ \mu s = 13.16\ ms$$

The bus master is therefore capable of identifying 75 different 1-wire devices per second.

I/O SIGNALLING

The DS2404 requires strict protocols to insure data integrity. The protocol consists of seven types of signalling on one line: reset pulse, presence pulse, write 0, write 1, read 0, read 1, and interrupt pulse. All these signals, with the exception of the interrupt pulse, are initiated by the bus master.

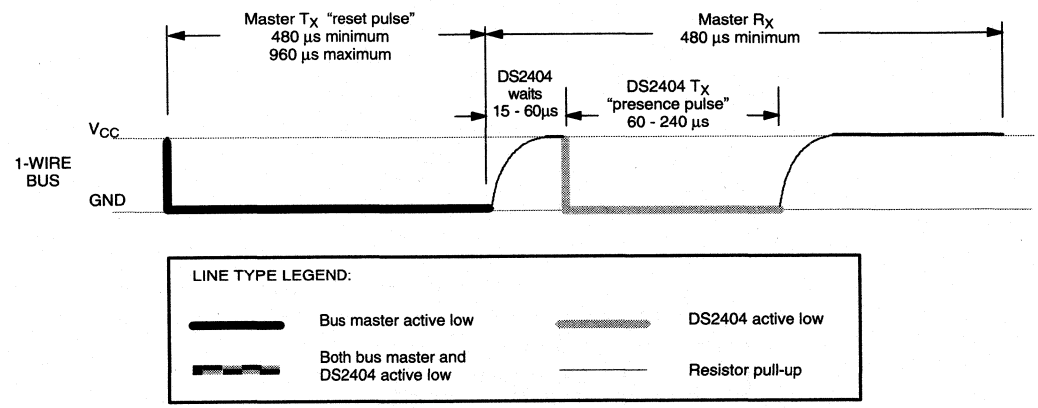
The initialization sequence required to begin any communication with the DS2404 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS2404 is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits (T_X) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into receive mode (R_X). The 1-wire bus is pulled to a high state via the 5K pull-up resistor. After detecting the rising edge on the I/O pin, the DS2404 waits 15-60 µs and then transmits the presence pulse (a low signal for 60 - 240 µs). There are special conditions if interrupts are enabled where the bus master must check the state of the 1-wire bus after being in the R_X mode for 480 µs. These conditions will be discussed in the "Interrupt" section.

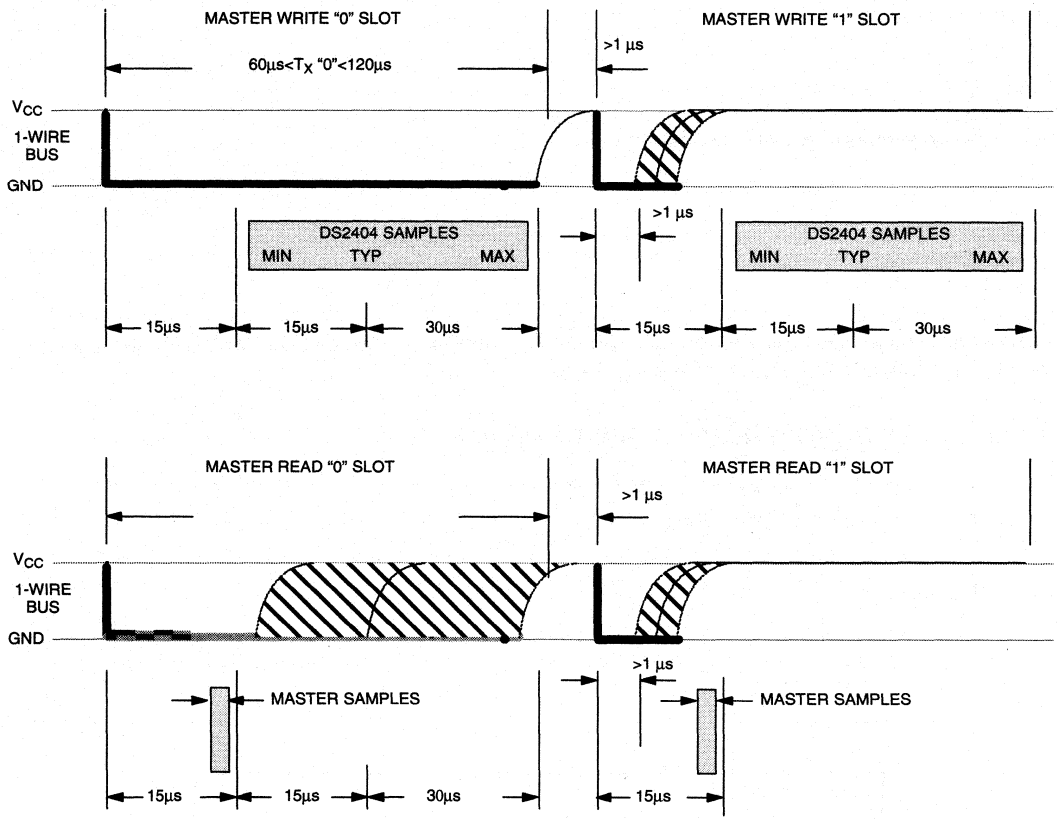
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the I/O line low. The falling edge of the I/O line synchronizes the DS2404 to the master by triggering a delay circuit in the DS2404. During write time slots, the delay circuit determines when the DS2404 will sample the I/O line. For a "read 0" time slot, the delay circuit determines how long the DS2404 will hold the I/O line low.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10



READ/WRITE TIMING DIAGRAM Figure 11



DETAILED MASTER READ "1" TIMING Figure 12

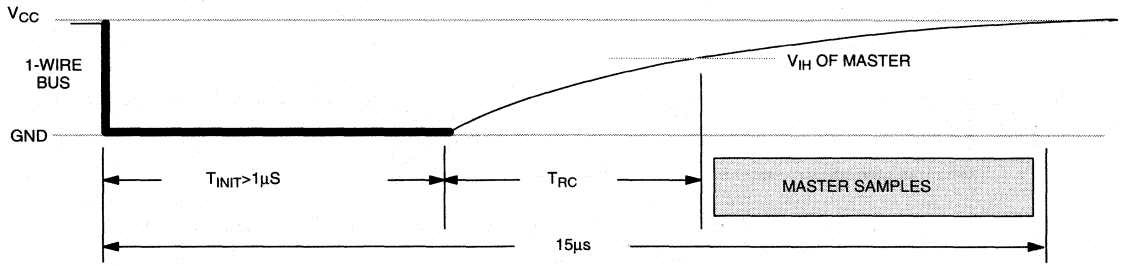
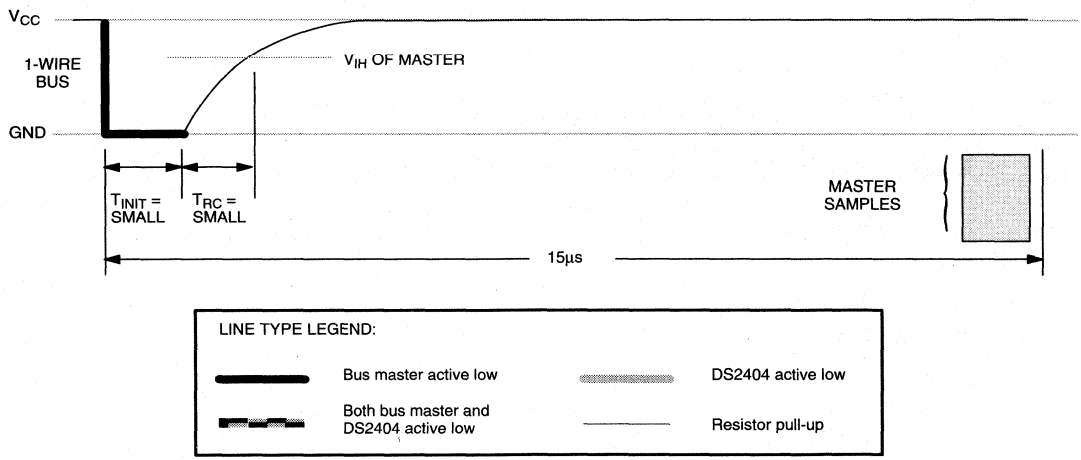


Figure 12 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15µs. Figure 13 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15µs period.

RECOMMENDED MASTER READ "1" TIMING Figure 13



Interrupts

An interrupt condition begins whenever any alarm flag is set and the flag's corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the flags are read) or if the corresponding interrupt enable bit(s) is disabled. An interrupt condition may be detected on either the $\overline{IRQ}$ pin or the I/O pin. During the interrupt condition, the open-drain $\overline{IRQ}$ pin is driven low and held low until the interrupt condition ceases.

On the 1-wire port, the part responds, in general, by driving the I/O pin low for an extended period of time and then releasing. The interrupt condition may produce two types of interrupts on the 1-wire port. A type 1 interrupt (Figure 14) occurs only when I/O is high and there has been no communication (i.e., there has not been a falling edge on I/O since the last presence pulse). If this is the case, I/O is driven low for a period of 960 µs to 3840 µs as soon as an interrupt condition begins. A presence pulse will follow the interrupt pulse.

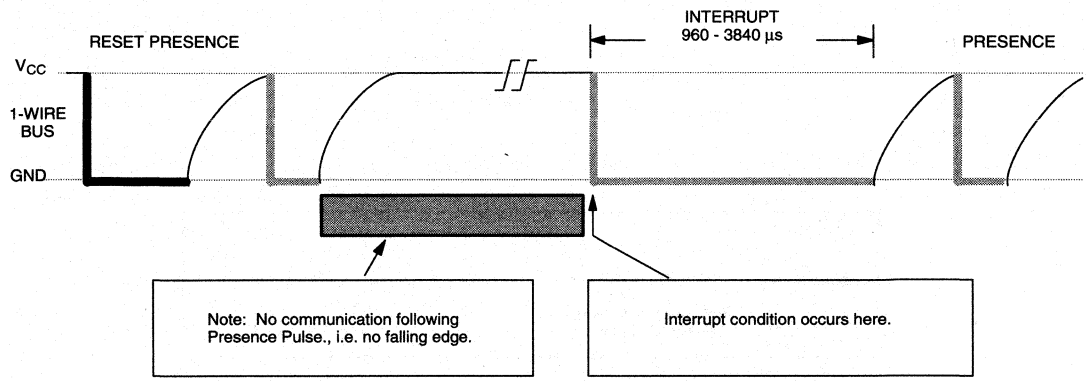
A type 2 interrupt (Figure 16) occurs if the host issues a reset pulse and an interrupt condition exists when the host releases the reset. If this is the case, I/O is driven low for an additional period of time, extending the reset pulse to a total period of 960 µs to 4800 µs. A presence pulse will follow the interrupt pulse. As long as the interrupt condition exists, the type 2 interrupt will occur with every reset pulse.

NOTE: If the interrupt condition begins during communication, a type 1 interrupt will not be issued. However, type 2 interrupts will occur during resets as expected.

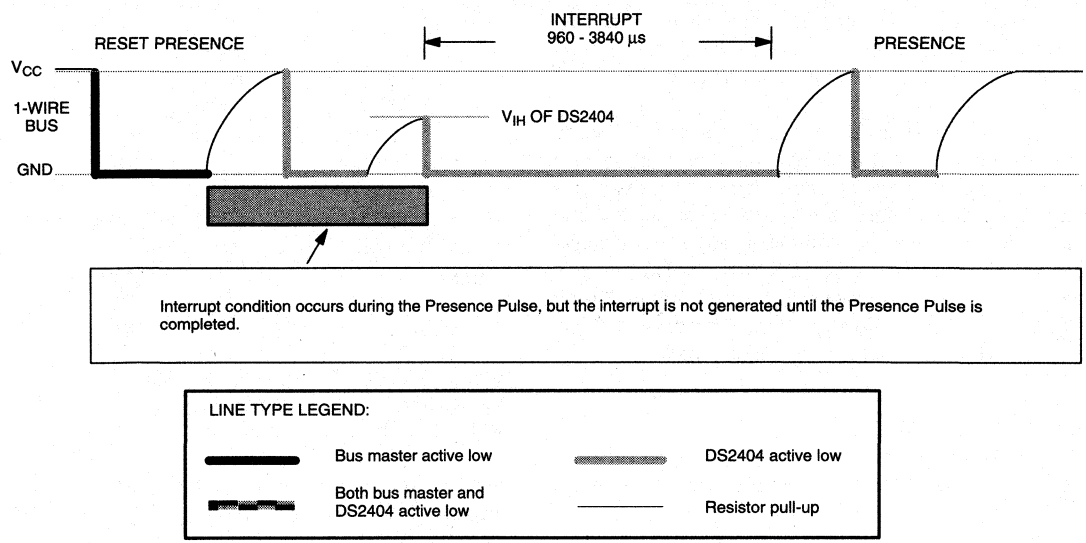
Special cases exist as follows:

Special Case A (Figure 15): If the interrupt condition begins during a presence pulse, the type 1 interrupt will be postponed until the presence pulse is over and I/O is a logic 1.

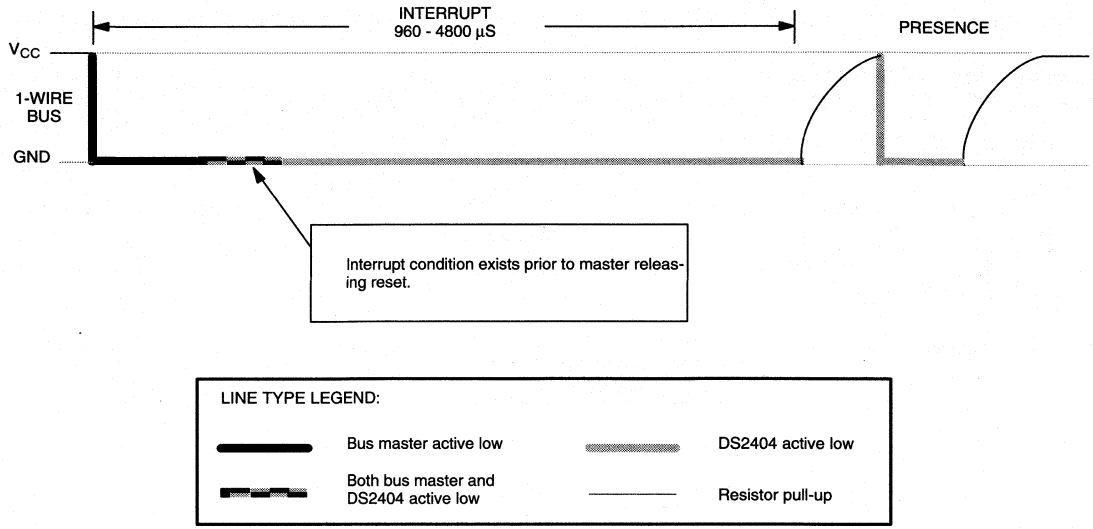
TYPE 1 INTERRUPT Figure 14



TYPE 1A INTERRUPT (SPECIAL CASE A) Figure 15



TYPE 2 INTERRUPT Figure 16



3-WIRE I/O COMMUNICATIONS

The 3-wire bus is comprised of three signals. These are the $\overline{RST}$ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{RST}$ input high. Driving the $\overline{RST}$ input low terminates communication. (See Figures 23 and 24.)

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. When reading data from the DS2404, the DQ pin goes to a high impedance state while the clock is high. Taking $\overline{RST}$ low will terminate any communication and cause the DQ pin to go to a high impedance state.

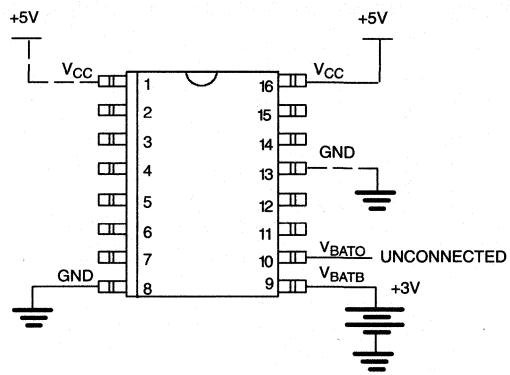
POWER CONTROL

There are two typical methods of supplying power to the DS2404, V_{CC} Operate mode and Battery Operate mode.

V_{CC} Operate Mode (Battery Backed)

Figure 17 shows the necessary connections for operating the DS2404 in V_{CC} Operate mode.

VCC OPERATE MODE Figure 17



V_{CC}	Pin 1 & 16	2.8 to 5.5 volts
V_{BATB}	Pin 9	2.8 to 5.5 volts*
V_{BATO}	Pin 10	must be unconnected

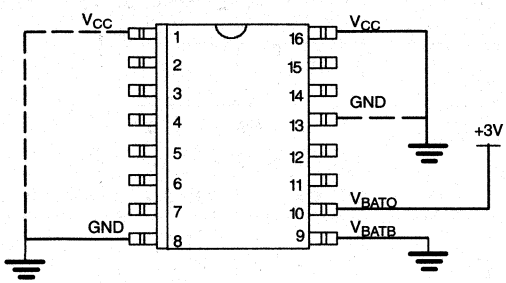
*While V_{BATB} may range from 2.8 to 5.5V, if the voltage on V_{BATB} ever exceeds the voltage on V_{CC}, the DS2404 will retain data, but will not allow access through the 1- or 3-wire port.

The V_{BATB} pin is normally connected to any standard 3-volt lithium cell or other energy source. As V_{CC} falls below V_{BATB}, the power switching circuit allows V_{BATB} to provide energy for maintaining clock functionality and data retention. No communication can take place while V_{BATB} is greater than V_{CC}. During power-up, when V_{CC} rises above V_{BATB} (~200 mV), the power switching circuit connects V_{CC} and disconnects V_{BATB}. If the oscillator is on, no communication can take place until V_{CC} has stayed (~200 mV) above V_{BATB} for 123 ± 2 ms.

Battery Operate Mode

Figure 18 shows the necessary connections for operating the DS2404 in Battery Operate mode.

BATTERY OPERATE MODE Figure 18



V_{CC}	Pin 1 & 16	Ground
V_{BATB}	Pin 9	Ground
V_{BATO}	Pin 10	2.8 to 5.5 volts

The V_{BATO} pin is normally connected to any standard 3-volt lithium cell or other energy source. Battery Operate mode provides low power consumption when used in conjunction with 1-wire interface.

Note: If the the 3-wire interface is used in Battery Operate mode, the voltage on DQ must never exceed the voltage on V_{BATO}.

3

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-20°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-20°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 9
Logic 0	V_{IL}	-0.3		+0.8	V	1
$\overline{RST}$ Logic 1		2.8		5.5	V	1
Supply	V_{CC}	2.8		5.5	V	1
Battery	V_{BATB}, V_{BATO}	2.8	3.0	5.5	V	1, 6

DC ELECTRICAL CHARACTERISTICS

(-20°C to +85°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			1	mA	
$\overline{RST}$ Resistance to Ground	Z_{RST}		65		KΩ	
D/Q Resistance to Ground	Z_{DQ}		65		KΩ	
CLK Resistance to Ground	Z_{CLK}		65		KΩ	
Active Current	I_{CC1}			2	mA	5
Standby Current	I_{CC2}			500	µA	11
I/O Operate Charge	Q_{BATO}			200	nC	10
Batt Current (OSC On)	I_{BAT1}			350	nA	7
Batt Current (OSC Off)	I_{BAT2}			200	nA	7

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			15	pF	
I/O (1-Wire)	$C_{IN/OUT}$			800	pF	8

AC ELECTRICAL CHARACTERISTICS: 3-WIRE INTERFACE (-20°C to +85°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
CLK to Data Hold	t_{CDH}	40			ns	2
CLK to Data Delay	t_{CDD}			100	ns	2,3,4
CLK Low Time	t_{CL}	250			ns	2
CLK High Time	t_{CH}	250			ns	2
CLK Frequency	t_{CLK}	DC		2.0	MHz	2
CLK Rise & Fall	t_R,t_F			500	ns	2
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	2
$\overline{RST}$ Inactive Time	t_{CWH}	250			ns	2
RST to I/O High Z	t_{CDZ}			50	ns	2

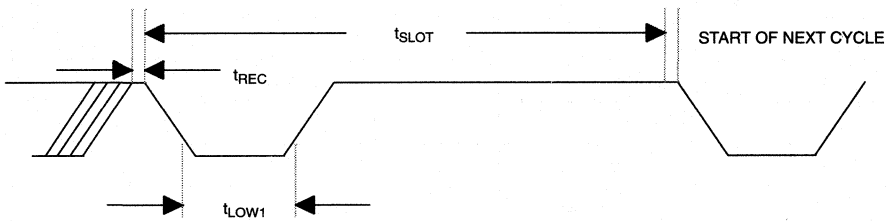
AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE (-20°C to +85°C; V_{CC}=2.8 to 5.5)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Interrupt	t_{INT}	960		4800	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		960	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

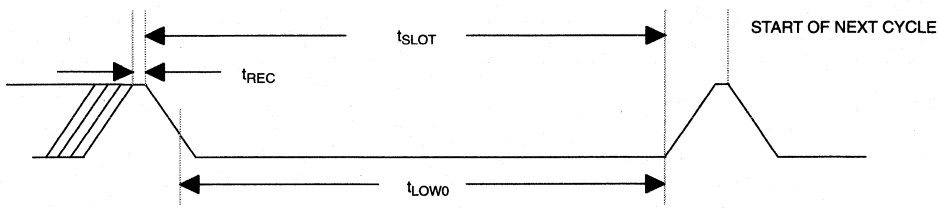
NOTES:

1. All voltages are referenced to ground.
2. V_{IH} = 2.0V or V_{IL} = 0.8V with 10 ns maximum rise and fall time.
3. V_{OH} = 2.4V and V_{OL} = 0.4V.
4. Load capacitance = 50 pF.
5. Measured with outputs open.
6. When battery is applied to V_{BATO} input, V_{CC} and V_{BATB} must be 0V.
7. V_{BATB}, or V_{BATO} = 3.0V; all inputs inactive state.
8. Capacitance on the I/O pin could be 800 pF when power is first applied. If a 5K resistor is used to pull-up the I/O line to V_{CC}, 5 µs after power has been applied, the parasite capacitance will not affect normal communications.
9. For auto-mode operation of the interval timer, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.
10. Read or write scratchpad (all 32 bytes) at 3.0V.
11. All other inputs at CMOS levels.

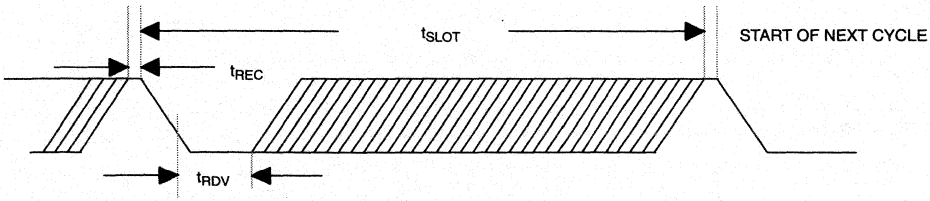
1-WIRE WRITE ONE TIME SLOT Figure 19



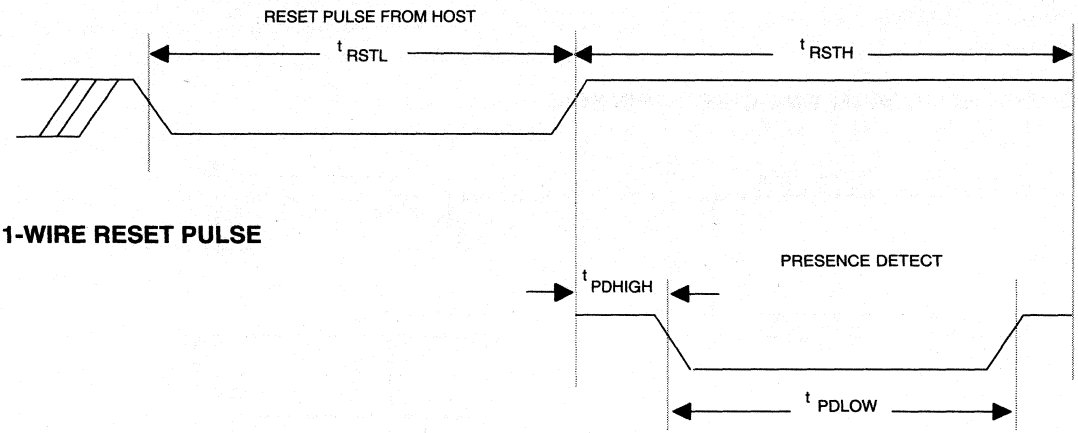
1-WIRE WRITE ZERO TIME SLOT Figure 20



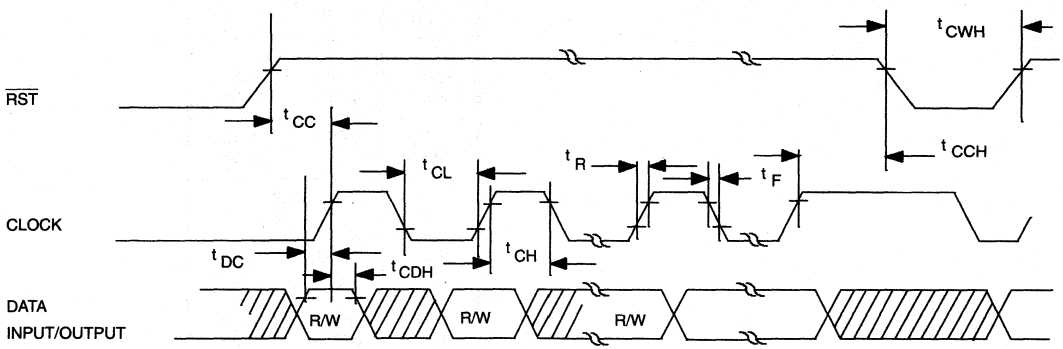
1-WIRE READ ZERO TIME SLOTS Figure 21



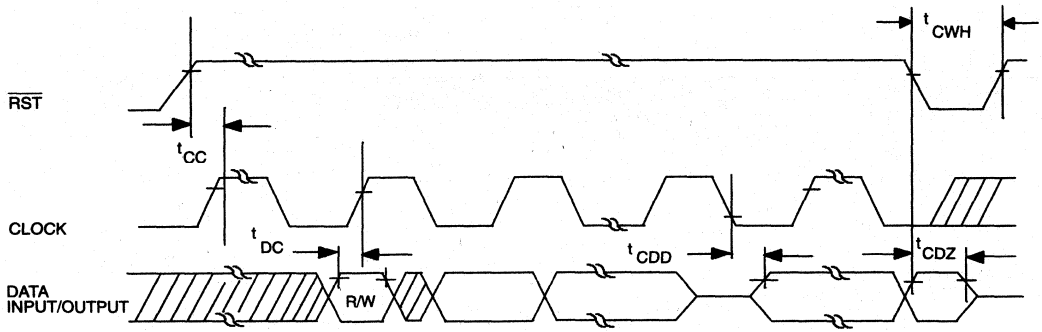
1-WIRE PRESENCE DETECT Figure 22



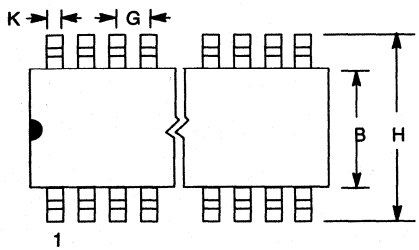
3-WIRE WRITE DATA TIMING DIAGRAM Figure 23

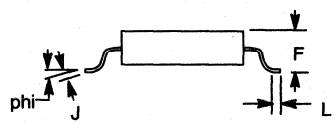


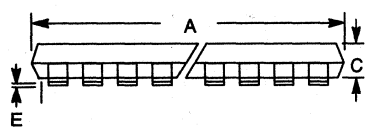
3-WIRE READ DATA TIMING DIAGRAM Figure 24



DS2404 ECONORAM TIME CHIP 16–PIN SOIC

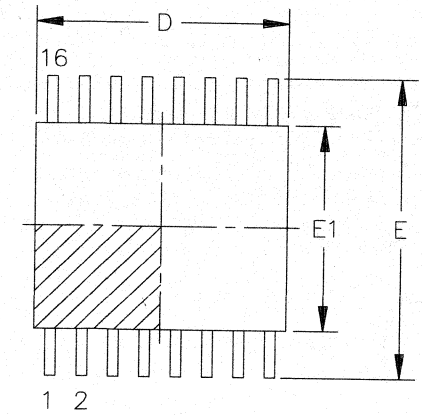


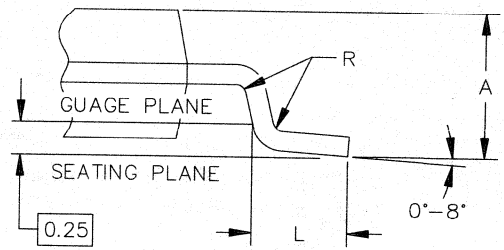




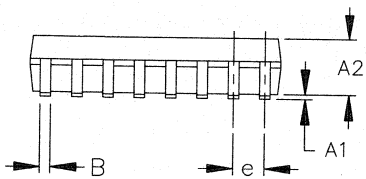
PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	.050 BSC 1.27 BSC	
H IN MM	0.398 10.11	0.416 10.57
J IN MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN MM	.016 .40	.040 1.02
PHI	0°	8°

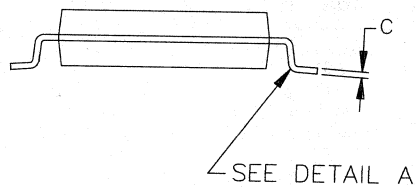
DS2404 ECONORAM TIME CHIP 16–PIN SSOP





DETAIL A

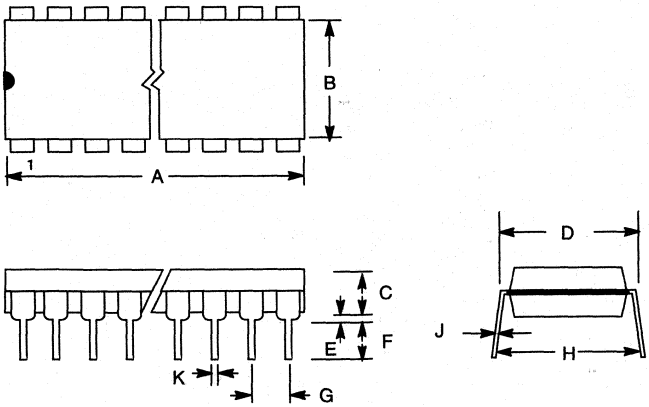




DIM.	MIN	MAX
A	–	2.13
A1	0.05	0.25
A2	1.62	1.88
B	0.22	0.38
C	0.09	0.20
D	5.90	6.50
E	7.40	8.20
E1	5.00	5.60
e	0.65 BSC	
L	0.63	1.03
R	0.09	–

NOTE: Units are in millimeters.

DS2404 ECONORAM TIME CHIP 16–PIN DIP

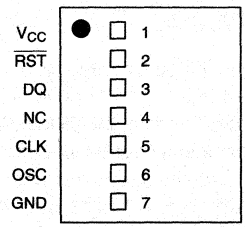


PKG	16-PIN	
DIM	MIN	MAX
A IN.	0.740	0.780
MM	18.80	19.81
B IN.	0.240	0.260
MM	6.10	6.60
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.300	0.325
MM	7.62	8.26
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.140
MM	3.04	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN	0.320	0.370
MM	8.13	9.40
J IN	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

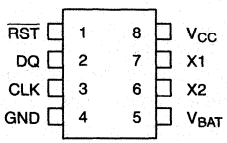
DALLAS SEMICONDUCTOR

Application Note 30
Recording Power Cycling Information Using the DS1602/DS1603

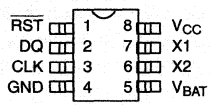
PIN ASSIGNMENT



DS1603 MODULE



DS1602
8 PIN DIP (300 mil)



DS1602S
8 PIN SOIC (200 mil)

DESCRIPTION

The DS1602 and DS1603 from Dallas Semiconductor offer a simplified hardware solution for keeping time as well as tracking powered up time of a system. The DS1602 and DS1603 can be read and written directly by a microprocessor or microcontroller using simple software; however, a more creative software algorithm can be used to track years, months, days, day of week, time of day, etc. In addition, power up time and number of power up cycles can also be tracked using the DS1602/DS1603 with appropriate software.

The continuous counter and power on counter in the DS1602/DS1603 are 32–bit counters which count in seconds and can be read and written through the DS1602/DS1603 3–wire serial interface. For the most basic implementation

1) the continuous counter will be set once and left to increment until it reaches its maximum value;

2) the powered up counter will be initially cleared once, and left to increment until it reaches its maximum value.

With these two assumptions, each counter has the ability to count up to a maximum value of (2^{32}–1) seconds, or 4.29 x 10^9 seconds (about 136 years).

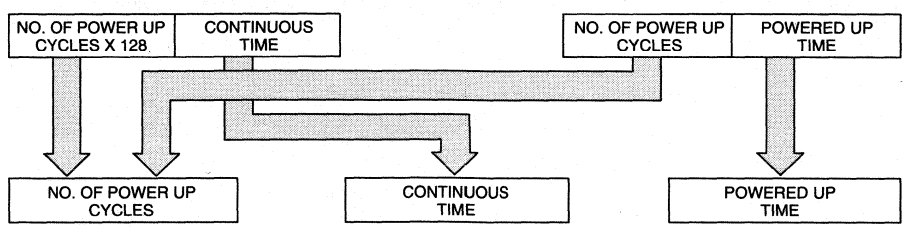
For a system that needs 100+ years of continuous timekeeping ability, the entire 32–bit counters may be required; but for users where the maximum continuous counter time required could be about 5 years, the unused counter bits space can be put to better use as memory bits for storing power up cycling information.

As seen in Figure 1, DS1602/1603 can be partitioned to provide a continuous time counter and a power up time counter with the capability to count up to 4.75 years, leaving the remaining higher bits of the counter available as a read/write non–volatile memory.

The software implementation requires the use of three registers so a third register must be mapped into the available two as in Figure 1.

An example of how the counters may be used to accomplish this task follows.

MAPPING THREE REGISTERS ONTO TWO Figure 25



CONTINUOUS COUNTER MAP

Bits 1–24: Remain as continuous timebase measurement, up to 16.7 x 10^6 seconds or 0.53 years.

Bit 25: Buffer or overflow bit; for when the continuous time counter reaches its maximum value and has not been read and reset by the processor. This bit also serves to separate the counter part of the register from the part which will be used as memory bits.

Bits 26–28: Number of years continuous time has been running, x 0.53.

Bits 29–32: Number of power cycles x 128. These four bits serve as a register which is incremented once for each full count reached in bits 26–32 of the power up counter.

POWERED UP COUNTER MAP

Bits 1–24: Remain as non-volatile seconds measurement of powered up seconds, storing up to 16.7 x 10^6 seconds, or 0.53 years.

Bit 25: Buffer or overflow bit; for when the power up counter reaches its maximum value and has not been read and reset by the processor. This bit also serves to separate the counter part of the register from the part which will be used as memory bits.

Bits 26–32: The high seven bits of the power up counter are the 1-127 count storage area for the number of power up cycles the DS1602 or DS1603 has seen.

With this discipline and the proper software algorithms in place, the DS1602 or DS1063, power on time and continuous time are maintained by the DS1602/DS1603's self-contained counters while the number of power up cycles and years of elapsed time x 0.53 is maintained in the higher order bits of the counters which are used as memory.

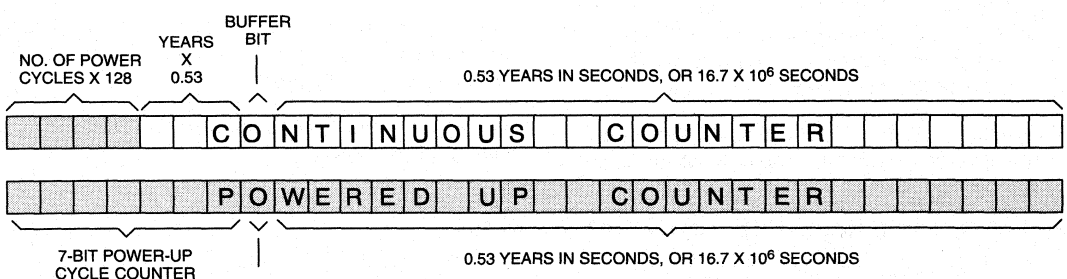
This implementation requires that a microcontroller must be prepared to read/write the DS1602 or DS1063 at least once every year.

For Continuous Time Tracking:

When the lower 24 bits of the continuous counter have exceeded 0.53 years and set bit 25 to 1, the controller must read the continuous counter, determine the status of bit 25, and if 1, clear the bit and increment the value in bits 26–28 by one half year. If bit 25 is not set, the lower 24 bits of the register have yet to reach 0.53 years and can continue counting.

Once the value in bits 26–28 has reached 111, or 7 x 0.53 years, the continuous time counter can continue to count up to 1.06 years in the lower 24 bits plus the overflow of 0.53 in bit 25 for a maximum value of 9 x 0.53 years.

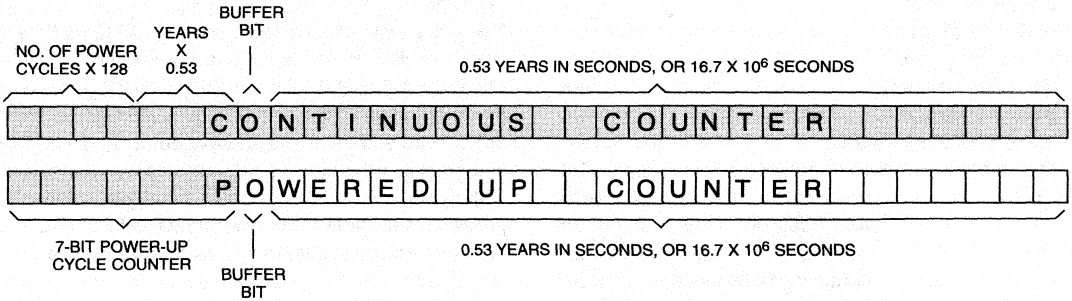
FOR CONTINUOUS TIME TRACKING Figure 26



For Power-up Time Tracking:

When the lower 24 bits of the power up counter have exceeded 0.53 years and set bit 25 of the counter to 1, the controller must read the power up counter, determine the status of bit 25, and if 1, clear the bit and store the value in external memory so that the power up counter can continue to count. The maximum power up time that can be stored in this way is 2 x 0.53 years within the DS1602/1603.

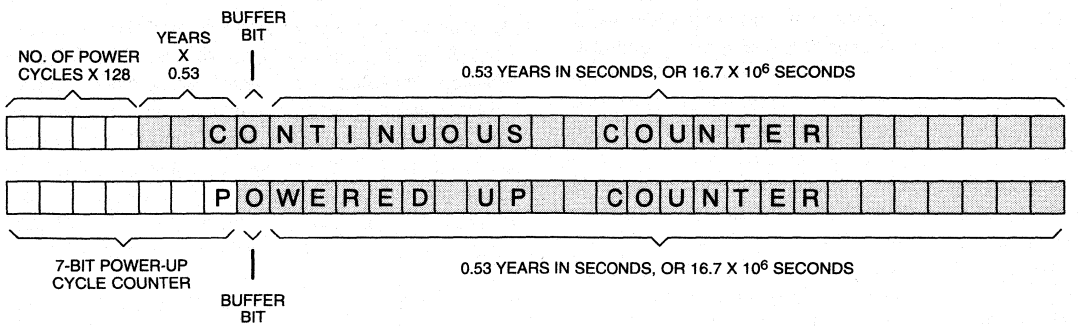
FOR POWER-UP TIME TRACKING Figure 27



For Number of Power-up Cycles Tracking:

Performing this function with the DS1603 or DS1602 is primarily a software task. When originally written with a start value or cleared, bits 25–32 of the power up counter must be set to 0. Upon each power up thereafter, the controller or processor connected to the DS1603 must read the power up counter and examine the value stored in the high seven bits. If the value is less than 1111111, then the controller must increment the value and write it back to the seven higher order bits. If the value in the higher order bits is 1111111, the controller must set the value of 0000000, read the value in the high four bits of the continuous time counter, increment it by one, and write the new value back to the high four bits. Using this software algorithm, the DS1063 or DS1602 can be used to record and store up to 2,047 power cycles.

FOR NUMBER OF POWER-UP CYCLES TRACKING Figure 28



DALLAS SEMICONDUCTOR

Application Note 52
Using the Dallas Phantom Real Time Clocks

DESCRIPTION

The Dallas Phantom Real Time Clocks are a family of devices that offer the combination of a transparent CMOS timekeeper and a nonvolatile static RAM meeting the standard JEDEC bytewide pinouts. Some varieties of the Dallas Phantom Real Time Clocks also provide a transparent CMOS timekeeper for use with ROM. The timekeeper is transparent to the RAM/ROM memory map because it does not occupy any of the existing RAM/ROM locations. These devices are termed "Phantom" because the timekeeper is accessed only when a predetermined 64–bit pattern has been received by the device. When the timekeeper is not being accessed, the RAM/ROM can be accessed normally. The timekeeper keeps track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. In the absence of power, a lithium energy source maintains the timekeeping operation and retains data in the CMOS static RAM.

FAMILY OVERVIEW

DS1215:

The heart of the Dallas Phantom Real Time Clock family is the DS1215 Phantom Time Chip. This integrated circuit is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and retains data in the CMOS static RAM. The watch keeps track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including correction for leap year every four years. The real time clock operates in one of two formats: 12–hour mode with an AM/PM indicator or a 24–hour mode . The nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can also be used to provide timekeeping functions with ROM.

DS1216:

Stemming from the DS1215 are the DS1216 SmartWatch Intelligent Sockets. The SmartWatch is a 600 MIL wide DIP socket with a built–in DS1215 (providing timekeeping functions and a nonvolatile RAM controller), an embedded lithium energy source, and a 32.768 kHz crystal. When the socket is mated with a bytewide CMOS static RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. The DS1216 can also be mated with a ROM to provide timekeeping capability only. Figures 1 and 2 show the basic interface of a SmartWatch with RAM inserted and a SmartWatch with ROM inserted, respectively.

DS1243Y, DS1244Y, DS1248Y:

The DS124X Nonvolatile SRAM with Phantom Time Clock modules are the final members of the Dallas Phantom Real Time Clock family. These devices are fully nonvolatile static RAM with a built–in Phantom clock, embedded lithium energy source, and 32.768 kHz crystal. These devices operate identical to a DS1216 with a RAM inserted. The DS124X Nonvolatile SRAM with Phantom Time Clock modules will maintain over 10 years of data retention in the absence of power.

Perhaps the best way to sum up the Dallas Phantom Real Time Clock family is as follows. The DS1215 Phantom Time Chip is the basic building block that provides timekeeping and a nonvolatile memory controller. The DS1216 then adds a crystal and lithium energy source to the DS1215 and encapsulates them all in a socket that will accept either a RAM or a ROM. Finally, the DS124X modules contain both nonvolatile RAM and timekeeping features in a ready–to–use package.

The entire Dallas Phantom Real Time Clock family is shown in Table 1.

Table 1

DS1215	Phantom Time Chip
DS1216B	SmartWatch/RAM 16K/64K
DS1216C	SmartWatch/RAM 64K/256K
DS1216D	SmartWatch/RAM 256K/1M
DS1216E	SmartWatch/ROM 64K/256K
DS1216F	SmartWatch/ROM 64K/256K/1M
DS1243Y	64K NV SRAM with Phantom Clock
DS1244Y	256K NV SRAM with Phantom Clock
DS1248Y	1024K NV SRAM with Phantom Clock

3

APPLICATION

The Dallas Phantom Real Time Clock family offers two features that will greatly enhance a system. The first feature is nonvolatile RAM capability. The second feature is that the Phantom Clock is transparent to the RAM and therefore timekeeping capacity can be added to a system without changing the existing hardware. All that is required is an existing bytewide memory socket. The retrofit capability is maximized through the transparent interfaces supported by the Phantom Time Chip. Also advantageous to the designer is that an upgrade path is provided to higher RAM densities with the DS124X modules or to higher RAM/ROM densities with the DS1216.

It should be mentioned that there is some software overhead that is associated with having timekeeping functions that are transparent to RAM as will be discussed in detail below. If it is determined that a transparent clock is not necessary, then the DS164X Nonvolatile Timekeeping RAM family could offer an excellent solution to your timekeeping and nonvolatile SRAM needs. These offer nonvolatile SRAM with the Real Time Clock registers located in the RAM address space. Another possible solution are the DS1386 or DS1486 RAMified Watchdog Timekeepers which offer nonvolatile RAM and Real Time Clock as well as a few extra features including alarm function and Watchdog timer.

OPERATION

Nonvolatile RAM Operation

One important feature of the Dallas Phantom Real Time Clocks is that the nonvolatile RAM can be used to store system configuration data and since the clock is transparent to the RAM, no memory is lost to timekeeping needs. When the Phantom Clock is not accessed, the $\overline{CE}$ signal is passed on to the chip enable of the memory. Reading and writing to the RAM is identical to that of a standard RAM chip. Figure 1 illustrates a typical RAM/Time Chip interface. Note that this is the basic interface used for the DS1216 SmartWatch/RAM and the DS124X.

The Phantom Real Time Clock family performs circuit functions required to make a CMOS RAM nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply depending on which is greater. The second function provided is power–fail detection. Power fail detection occurs when V_{CCI} falls below V_{TP}, which is equal to 1.26 x V_{BAT}. When V_{CCI} goes out of tolerance, a comparator outputs a power–fail signal to the chip enable logic. The third function accomplishes write protection by holding the chip enable signal to the memory ($\overline{CEO}$) within 0.2 volts of V_{CC} or battery as long as V_{CC} is out of tolerance. During nominal power supply conditions the memory chip enable signal ($\overline{CEO}$) will track the chip enable signal ($\overline{CEI}$) sent to the socket with a maximum propagation delay of 20 ns.

Finally, an important consideration when using the DS1216 is to select a RAM that draws no more than a maximum of 1 µA. If the RAM data retention current is larger than 1 µA, the device will not meet the data retention expectations of more than 10 years at 25°C. In the 10 year data retention calculation for the DS1216, it is assumed that system power will be on 20% of the time. Perhaps the best way to insure that a data retention of 10 years at 25°C is met is to use one of the DS124X modules with self–contained nonvolatile RAM. The DS124X modules will insure data retention for 10 years regardless of how often the system power is on.

ROM Operation

The DS1215 and DS1216(E/F) can also be used in conjunction with a ROM. A typical ROM/Time Chip interface is illustrated in Figure 2. In this configuration, the ROM/$\overline{RAM}$ pin is connected to V_{CCO} to select the ROM mode of operation. Since ROM is a read–only device that retains data in the absence of power, battery back–up and write protection is not required. As a

result, the chip enable logic will force $\overline{CEO}$ low when power fails. The real time clock does retain the same internal nonvolatility and write protection as described in the RAM mode.

Real Time Clock Operation

The block diagram of Figure 3 illustrates the main elements of the Phantom Clock. Communication with the Phantom Clock is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper write data as shown in Figure 4. All accesses which occur prior to recognition of the 64–bit pattern are directed to memory via the chip enable output pin ($\overline{CEO}$). After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock and $\overline{CEO}$ remains high during this time, disabling the connected memory.

Data transfer to and from the Phantom Clock is accomplished with a serial bit stream under the control of chip enable input ($\overline{CEI}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle using the $\overline{CEI}$ and $\overline{OE}$ control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64–bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CEI}$ and $\overline{WE}$ control of the Phantom Clock. These 64 write cycles are used only to gain access to the Phantom Clock. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a scratch pad for the Phantom Clock.

When the first write cycle is executed, it is compared to bit 0 of the 64–bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored until a read cycle is encountered which resets the comparison register pointer to the beginning of the 64–bit comparison register. If a read cycle occurs at any time during the pattern recognition process, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 4). With a correct match of the 64 bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed.

The next 64 cycles will cause the Phantom Clock to either receive or transmit data, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Data will either be written to or read from the eight Phantom Clock registers shown in Figure 5. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

Figure 6 offers an example of pseudo code for both accessing the Phantom Clock embedded in a RAM through pattern recognition and interfacing with the clock registers. Another source code example is given in Figure 7. This code is used for interfacing with the 8051 microcontroller. Also, refer to the data book for timing diagrams for both read and write cycles.

Interfacing the Phantom Time Clock with a ROM is somewhat different from that of a RAM. This is due to the fact that no writes are made to a ROM. Since there are no $\overline{WE}$ or data in signals associated with the ROM, the Phantom Time Clock instead uses two address lines to access the real time clock as can be seen in Figure 2.

In summary, the operation of the Phantom Clocks is best defined as operating in two different modes. The first being the pattern match mode. In this mode, the Phantom Clock is transparent to the system yet monitors communication to the RAM waiting for a match of it's 64–bit access pattern. When the 64–bit access pattern has been written, the Phantom Clocks enter the clock access mode. In this mode, the eight phantom clock registers are available to be written or read and will stay in this mode until all eight registers have been accessed, until a reset has been executed, or until a power fail.

TROUBLESHOOTING

The Dallas Phantom Real Time Clocks have proven to be highly reliable and meet the published specifications. However, in the course of development, several common difficulties could be experienced. To reduce these difficulties, Dallas Semiconductor has gathered the common difficulties and pitfalls into a troubleshooting guide to assist users.

COMMON DIFFICULTIES

Cannot Access Clock Registers

Several items can cause this phenomena.

1. Comparison register pointer has has not been set to the first bit. The Phantom Real Time Clock hides behind the SRAM and waits for a match to it's 64–bit access pattern. In this mode (the pattern match mode), every write operation to the RAM will be interpreted as an attempt to match the access pattern by matching the value written to DQ0 (D for the DS1215) to the pattern bit pointed to by the pattern match pointer. It is possible that a partial match of the pattern can occur during normal operation of a system. It is best to assume that there is a partial match of the access pattern and that the comparison register pointer is not pointing to the first bit of the match pattern. Therefore, the comparison register pointer must be reset to the first pattern bit before writing the match pattern. This is accomplished by performing one read operation of the RAM before writing the match pattern.
2. Device is in clock access mode after system reset or interrupt. It is possible that during the course of previous operation, the Phantom Clock had been accessed, but had not gone back into pattern match mode before a system reset or interrupt occurred. In other words, data bits would be written to or read from the Phantom Clock registers rather than the RAM. A solution to this problem is to execute 65 consecutive read cycles immediately after an interrupt or system reset. This will insure that the device is taken out of the clock access mode (by reading a maximum of 64 bits) and will reset the comparison register pointer.
3. Access pattern has been input in reverse order. Insure that the pattern is input in the following order. Start with bit 0 of byte 0 continuing to bit 7 of byte 7.
4. Device is being reset. Insure that the device is not accidentally being reset. This can especially be a problem with the DS1216C, DS1216D, and DS1244Y where the reset pin is shared with an address pin. In this situation, that particular address line must never be taken low unless the reset bit (byte 4, bit 4) of the Phantom Clock is disabled, otherwise the device will be reset and the data transfer will be aborted.
5. Device is in constant write protect mode. If only one battery is being used for the DS1215, ensure that the BAT2 pin is grounded. If this pin remains floating it is possible that the device will think that a power fail condition has occurred. This is due to the method in which power fail is detected. A power fail is determined to have occurred when V_{CC} is less than V_{TP}, which is equal to 1.26 x V_{BAT}. If V_{BAT2} is floating, it is possible that the node could float to a value such that V_{TP} is equal to V_{CC} and thus the device will always be in a write protect mode.

Device Will Not Oscillate

1. Oscillator enable bit is disabled. Insure that the oscillator enable bit (bit 5 of byte 4) is at logic 0.
2. Wrong crystal used (DS1215). Insure that the correct crystal is being used. It is very important that a crystal with a load capacitance of 6 pF is used. Dallas Semiconductor recommends Seiko part number DS–VT–200, Daiwa part number DT–26S, or equivalent.
3. Poor crystal connection (DS1215). To insure the greatest performance, insure that the crystal is placed as close as possible to the crystal input pins. It should also be mentioned that the DS1215 does not require load capacitors or feedback resistors.

Note: It should also be mentioned that it is difficult to determine if the device is oscillating by trying to measure the frequency with an oscilloscope probe. This is because of the loading caused by the scope probe which can kill the oscillator.

Timekeeping Inaccurate

1. Input pins driven higher than V_{CC}. It is very important to insure that input pins never go above V_{CC}. If any input is allowed to go above V_{CC}, it is possible that the oscillator may be briefly stopped which will cause the device to lose time.
2. Wrong crystal used (DS1215). For best accuracy, insure that the correct crystal is used.

RAM is losing data when powered down.

This problem can occur especially in NMOS processors which become unstable at a higher voltage than CMOS processors. This problem manifests itself in the method in which power fail is determined. Write protection is asserted when V_{CC} drops below V_{TP}, which is equal to 1.26 x V_{BAT}. Typically, the battery has a voltage of ~3.0V which leads to a V_{TP} of 3.78V. Therefore, in a power down situation, if the processor becomes unstable at a V_{CC} of greater than ~3.78V (which is often the case for an NMOS processor), a spurious write cycle could corrupt the data in the Phantom Clock. The solution to this problem is to ensure that the processor is reset before it becomes unstable and thus prevent any unwanted writes from being executed. This can be accomplished by monitoring V_{CC} by one of Dallas Semiconductor's power monitors (the DS123X family) which generate a reset signal when V_{CC} is out of tolerance.

Can not read consecutive hundredths of seconds.

It is not possible to read consecutive hundredths of seconds because the access time to read the clock registers is too long.

COMMON PITFALLS

Device needs separate read and write signals. The Dallas Phantom Real Time Clocks were designed with Intel timing in mind. Therefore it is necessary to have separate read and write signals. It should be further stressed that simply complementing one signal to arrive at the other is not sufficient because this will cause the pattern match pointer to be reset during each write cycle since the $\overline{OE}$ signal will toggle whenever the $\overline{WE}$ signal toggles.

Battery attachment (DS1215). Any battery attached to the BAT1 or BAT2 pins must be connected directly to the pin. It should be noted that a diode should not be connected between the battery input pin and the battery. This is not necessary because internal reverse charging current protection circuitry is provided and is UL recognized (#E99151).

ROM/$\overline{RAM}$ pin (DS1215). Insure that the ROM/$\overline{RAM}$ pin is set to the correct value.

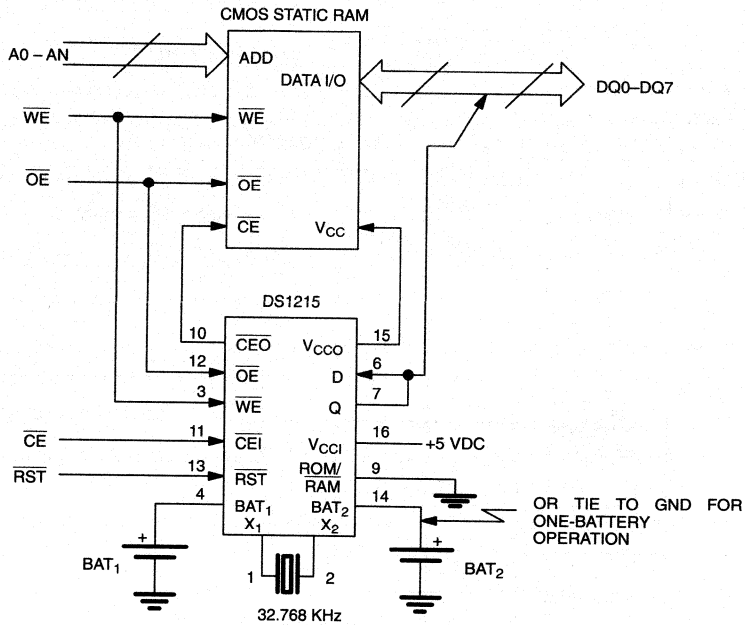
Reading and writing to clock registers. It is important that all 64 bits be read or written to when the clock registers have been accessed. If this is not done, the device will remain in the clock access mode.

Do not water wash DS1216 Intelligent Sockets. Water washing for flux removal must not be performed on the DS1216 Intelligent Sockets because contaminants in the water can cause discharging of the internal lithium energy source.

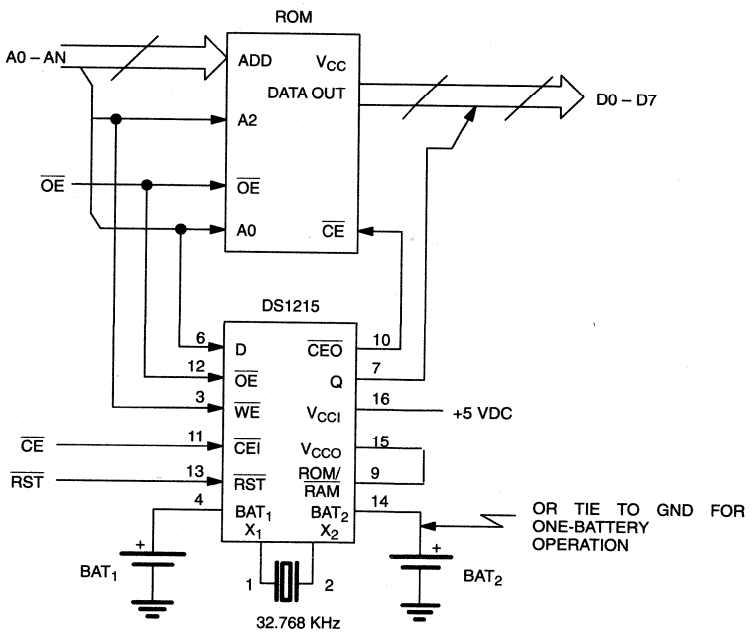
Crystal selection (DS1215). A 32.768 kHz quartz crystal, Seiko part number DS–VT–200, Daiwa part number DT–26S, or equivalent should be used. The crystal selected for use must have a specified load capacitance of 6 pF. The use of an incorrect crystal can kill the oscillator or cause accuracy problems. Also, the use of an external trim capacitor to adjust the oscillator is discouraged.

It is recommended that one of the Dallas SmartWatch or Nonvolatile SRAM with Phantom Time Clock devices be selected for the highest accuracy (±1 minute/month).

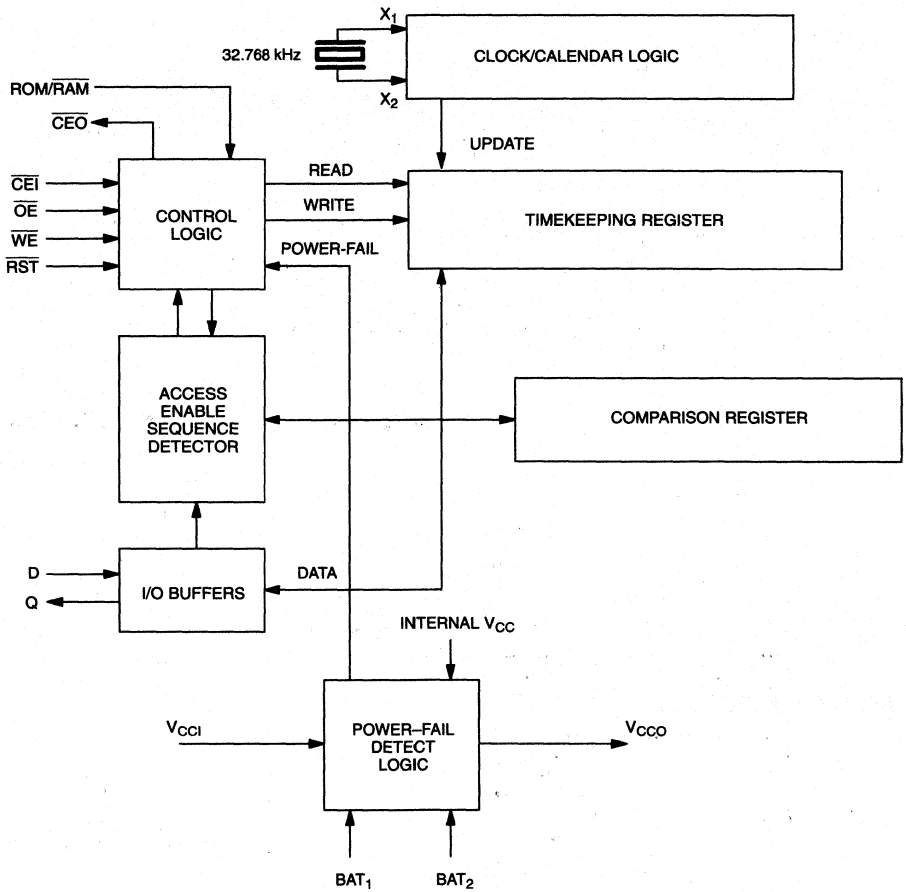
RAM/TIME CHIP INTERFACE Figure 1



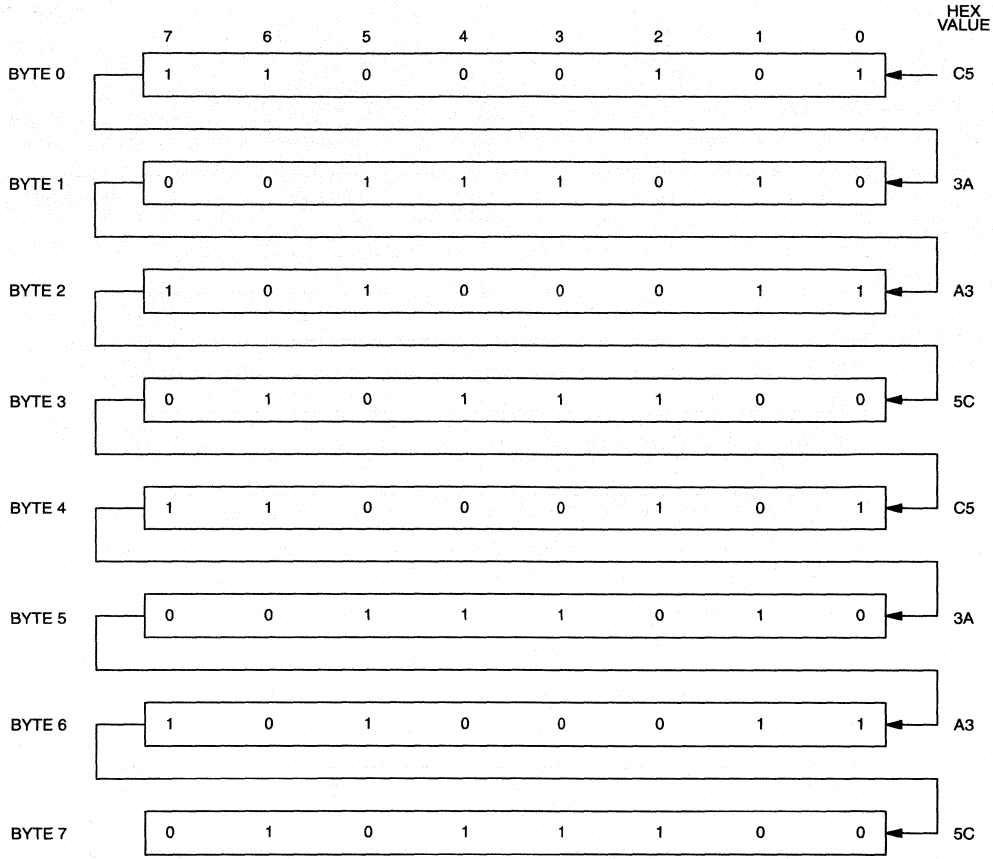
ROM/TIME CHIP INTERFACE Figure 2



TIMING BLOCK DIAGRAM Figure 3



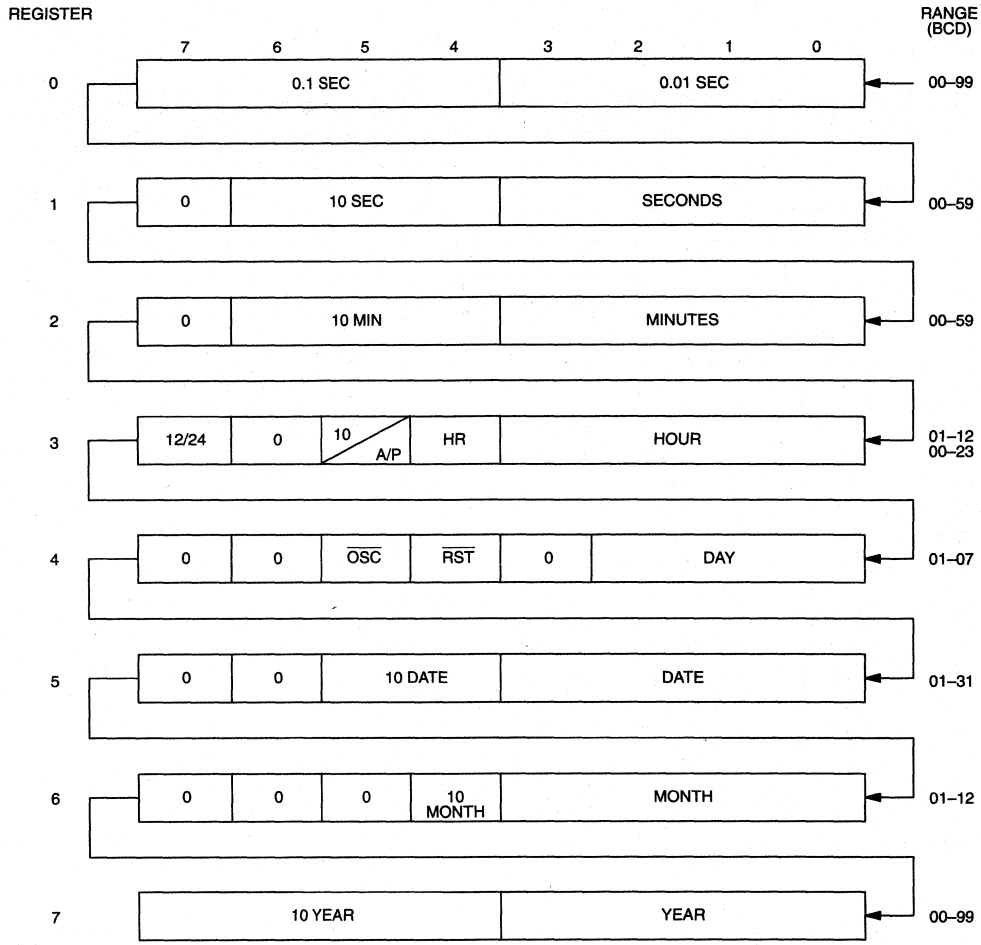
TIME CHIP COMPARISON REGISTER DEFINITION Figure 4



NOTE:

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Time Chip are less than 1 in 10^{19}. This pattern is sent to the Phantom Clock LSB to MSB.

TIME CHIP REGISTER DEFINITION Figure 5



PSEUDO CODE Figure 6

```
* This code will access the Phantom Time Clock by sending the 64-bit    *
* access pattern.  Then the time data will be written to the clock and *
* finally the Phantom Time Clock will be accessed again and it will be *
* read.  The time information to be written is 12:00 PM Wednesday,      *
* January 1, 1992.  Also note that the oscillator has been enabled and *
* reset has been disabled.                                             *

A :  Array[0..7] = (C5, 3A, A3, 5C, C5, 3A, A3, 5C)  (access pattern)
T :  Array[0..7] = (00, 00, 00, B2, 14, 01, 01, 92)  (time data)
X :  Byte at 1000                                    (memory location 1000H)
D :  Array [0..7]
S :  Byte

* Send access pattern to Phantom Time Clock *
  FOR I = 0 TO 64  S = x                    (perform 65 consecutive reads from x)
  FOR I = 0 TO 7                            (loop for 8 bytes)
      FOR J = 0 TO 7                        (loop for 8 bits)
          X = A[I] SHR J                    (write to X, shift bits right J)
      NEXT J
  NEXT I

* Write time data to Phantom Time Clock registers *
  FOR I = 0 TO 7                            (loop for 8 bytes)
      FOR J = 0 TO 7                        (loop for 8 bits)
          X = T[I] SHR J                    (write to X, shift bits right J)
      NEXT J

* Send access pattern to Phantom Time Clock *
  FOR I = 0 TO 64  S = X                    (perform 65 consecutive reads from X)
  FOR I = 0 TO 7                            (loop for 8 bytes)
      FOR J = 0 TO 7                        (loop for 8 bits)
          X = A[I] SHR J
      NEXT J
  NEXT I

* Read Phantom Time Clock registers *
  FOR I = 0 TO 7                            (loop for 8 bytes)
      D[I] = 0                              (initiate the byte)
      FOR J = 0 TO 7                        (loop for 8 bits)
          D[I] = D[I] or (X and 1) SHL J    (position bits in byte)
      NEXT J
  NEXT I
```

EXAMPLE SOURCE CODE FOR 8051 MICROCONTROLLER Figure 7

```
; 8051CODE.DOC
; RTC procedure to access the DS1215 Serial Timekeeper, or DS1216
; SmartWatch using 8031, 8051 or 80C196
;
BIT_SEG SEGMENT BIT
        RSEG    BITSEG
WF:     DBIT    1
BYTE_SEG        SEGMENT DATA
        RSEG    BYTE_SEG
BUFF:   DS      8           ;Centi-sec:  00-99
;                           ;Seconds:  00-59
;                           ;Minutes:  00-59
;                           ;Hours:  01-12 / 00-23
;                           ;Day:1nHEX % RST off, n=DAY# 01-07
;                           ;Date:  01-31
;                           ;Month:  01-12
;                           ;Year:  00-99
CODESEG SEGMENT CODE
        RSEG    CODE_SEG
;**************************
;*** MAIN PROGRAM GOES HERE
;**************************
;
; Main program SETS WF for Read Mode and on return from RTC the BUFF will
; contain the 8 bytes of data read from the clock.  If WF is CLEARED then
; RTC will return after writing the 8 byte BUFF to the clock.
;
;    NOTE  !!! : Refer to the DS1215 (RAM MODE) or DS1216 data sheet.
;
RTC:    PUSH    PSW                 ;Save user registers.
        PUSH    ACC
        PUSH    B
        MOV     B, RO
        PUSH    B
        MOV     RO, #BUFF           ;Load pointer to start of table.
        LCALL   OPEN                ;Set up to open the DS1216.
        MOV     B, #8H              ;Load loop counter for 8 bytes.
        JNB     WF, WRITETIME       ;Read/Write mode check.
;
READTIME:       LCALL   RBYTE       ;Read one byte.
        MOV     @RO, A              ;Save in RTn temporary register.
        INC     R0                  ;Temporary data register pointer.
        DJNZ    B, READTIME         ;Loop to read 8 bytes.
        SJMP    ENDTIME             ;Done reading goto finish.
;
WRITETIME:      MOV     A, @R0      ;Load byte of data to be written.
        LCALL   WBYTE               ;Write one byte.
        INC     R0                  ;Temporary data register pointer.
        DJNZ    B, WRITETIME        ;Loop to write 8 bytes.
```

```
;
ENDTIME:          POP     B                 ;Restore registers.
          MOV     R0, B
          POP     B
          POP     ACC

          POP     PSW
          RET                               ;Return to main calling program.
;
;
;
;
;*************************************
; SUBROUTINE TO OPEN THE CLOCK/CALENDAR
;*************************************
;
; This subroutine executes the sequence of reads and writes which
; is required in order to open communication with the timekeeper.
;
OPEN:     LCALL   CLOSE                     ;Make sure it is closed.
          MOV     B, #4                     ;Set pattern period count.
          MOV     A, #0C5H                  ;Load first byte of pattern.
OPENA:    LCALL   WBYTE                     ;Send out the byte.
          XRL     A, #0FFH                  ;Generate next pattern byte.
          LCALL   WBYTE                     ;Send out the byte.
          SWAP    A                         ;Generate next pattern byte.
          DJNZ    B, OPENA                  ;Repeat until 8 bytes sent.
          RET                               ;Return.
;
;*****************************
;*** SUBROUTINE TO CLOSE CLOCK
;*****************************
;
; This subroutine insures that the registers of the timekeeper
; are closed by executing 72 successive reads of the date and time
; registers.
;
CLOSE:    MOV     B, #9                     ;Set up to read 9 bytes.
CLOSEA:   LCALL   RBYTE                     ;Read a byte.
          DJNZ    B, CLOSEA                 ;Loop for 9 byte reads.
          RET                               ;Return
;
;***********************************
:*** SUBROUTINE TO READ A DATA BYTE
;***********************************
;
RBYTE:    PUSH    DPL                       ;Save the data
          PUSH    DPH                       ; pointer on stack.
          PUSH    B                         ;Save the B register.
          MOV     DPTR, #RTCADDR            ;Enable the clock.
          MOV     B, #8                     ;Set the bit count.
```

```
LI:       PUSH     ACC                  ;Save the accumulator.
          MOVX     A, @DPTR             ;Input the data bit.
          RRC      A                    ;Move it to carry.
          POP      ACC                  ;Get the accumulator.
          RRC      A                    ;Save the data bit.
          DJNZ     B, LI                ;Loop for a whole byte.
          POP      B                    ;Restore the B register.
          POP      DPH                  ;Restore the data
          POP      DPL                  ; pointer from stack.
          RET                           ;Return.
;
;
;
;**********************************
;*** SUBROUTINE TO WRITE A DATA BYTE
;**********************************
;
WBYTE:    PUSH     DPL                  ;Save the data
          PUSH     DPH                  ; pointer on stack.
          PUSH     B                    ;Save the B register.
          MOV      DPTR, #RTCADDR       ;Enable the clock.
          MOV      B, #8                ;Set the bit count.
LO:       PUSH     ACC                  ;Save the accumulator.
          ANL      A, #1                ;Set up bit for output.
          MOVX     @DPTR, A             ;Output the data bit.
          POP      ACC                  ;Restore the accumulator.
          RR       A                    ;Position next bit.
          DJNZ     B, LO                ;Loop for a whole byte.
          POP      B                    ;Restore the B register.
          POP      DPH                  ;Restore the data
          POP      DPL                  ; pointer from stack.
          RET                           ;Return.
;
;***************
;END OF PROGRAM
;***************
;
          END                           ;End of program.
```

DALLAS SEMICONDUCTOR

Application Note 58
Crystal Considerations with Dallas Real Time Clocks

Dallas Semiconductor offers a variety of real time clocks. The majority of these are available either as integrated circuits or modules. Modules include a real–time clock integrated circuit, crystal, and lithium energy source encapsulated in one package.

This application note is intended to help those customers who choose to use Dallas Semiconductor real–time clock integrated circuits rather than modules and therefore need to attach their own crystal. The information contained in this article will be beneficial in maximizing accuracy and insuring proper operation of Dallas real time clocks by helping the customer to select the correct crystal to use and by providing a few basic guidelines that should be followed when placing the crystal on a PCB layout. This application note will also include an elementary discussion of the effect of temperature on the accuracy of real time clocks.

CRYSTAL SELECTION

In any crystal based oscillator circuit, the oscillator frequency is based almost entirely on the characteristics of the crystal that is used. It is important to select a crystal that meets the design requirements. In particular, the specified load capacitance (C_L) is a critical crystal parameter that is often overlooked. This parameter specifies the capacitive load that must be placed across the crystal pins in order for the crystal to oscillate at its specified frequency. The crystal manufacturer actually "trims" the crystal to oscillate at its nominal frequency for the given specified load capacitance. Note that the C_L is the capacitance that the crystal needs to "see" from the oscillator circuit, it is **not** the capacitance of the crystal itself.

As previously stated, the load capacitance that the crystal "sees" is due to the capacitance of the oscillator circuit itself. Any change in the load capacitance of the oscillator circuit will therefore have an affect on the frequency of that oscillator. Likewise, using a crystal that has a C_L that is different than the actual load capacitance of the circuit will also affect the frequency of the oscillator. Most of Dallas Semiconductor real time clocks have an internal capacitance of 6 pF across the crystal input pins.

In general, using a crystal with a C_L that is larger than the load capacitance of the oscillator circuit will cause the oscillator to run faster than the specified nominal frequency of the crystal. Conversely, using a crystal with a C_L that is smaller than the load capacitance of the oscillator circuit will cause the oscillator to run slower than the specified nominal frequency of the crystal.

All Dallas Semiconductor real time clocks have been designed to operate with a 32.768 KHz crystal that has a C_L of 6 pF. For proper operation and accuracy, a crystal that meets these requirements should be used. As mentioned above, using a crystal with the wrong C_L will cause the oscillator to run fast or slow. Limited characterization at Dallas Semiconductor has confirmed this. For example, limited characterization on the DS1485 has revealed that the device will run approximately 4 minutes/month fast at room temperature (25°C) when a 12 pF crystal is used. The device had an accuracy within ±30 seconds/month when a 6 pF crystal was used.

Several vendors offer crystals that can be used with Dallas Semiconductor real time clocks. These vendors include Epson (part number DS–VT–200) and Daiwa (part number DS–26S). If surface mount crystals are needed, Epson also offers the MC–405 or MC–406. Equivalent crystals from other crystal manufacturers can also be used. As a reference, see Table 1 for the characteristics of the Daiwa DS–26S crystal.

CRYSTAL SPECIFICATIONS Table 1

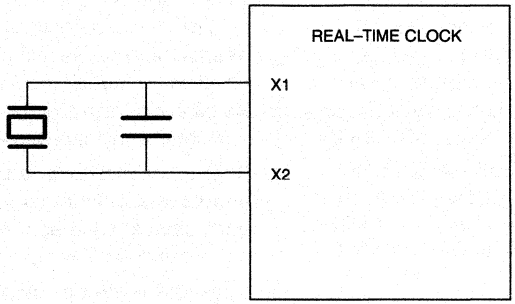
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Nominal Frequency	F_0		32.768		kHz	
Load Capacitance	C_L		6		pF	
Temperature Turnover Point	T_0	20	25	30	°C	
Parabolic Curvature Constant	k			0.042	ppm/°C	
Quality Factor	Q	40,000	70,000			
Series Resistance	R1			45	KΩ	
Shunt Capacitance	C_0		1.1	1.8	pF	
Capacitance Ratio	C_0/C_1		430	600		
Drive Level	D_L			1	µW	

STANDARD 6pF RTC CRYSTALS

MANUFACTURER	MODEL	C_L	PACKAGE
KDS/Daiw Crystral Corp	DT–38 DT–381 DT–26S DT–261S DT–14 DT–26S 32.768 Hz DMX–2632.768 KHz DS–VT–200 MC–405 MC–406	6pF	Cylinder SMT SMT
Epson Crystal Corp.	C–001R C–002RX C–004R C–005R MC–30632.768K E	6pF	Cylinder SMT

Dallas Semiconductor does not recommend using crystals that do not have a C_L of 6 pF because this will decrease the accuracy of the clock. However, it is possible to improve the decreased accuracy caused by using a crystal with a C_L that is greater than 6 pF. This can be accomplished by increasing the load capacitance that the crystal "sees" by connecting a capacitor in parallel with the crystal as shown in Figure 1. As a rule of thumb, the approximate capacitor value is equal to the specified load capacitance (C_L) of the crystal minus 6 pF (the approximate load capacitance of the real time clock oscillator circuit). For example, if a 12 pF crystal is being used, a 6 pF capacitor should be placed in parallel with it to improve the accuracy of the oscillator. A 12 pF crystal is adjusted by the crystal manufacturer to oscillate at its specified nominal frequency when a 12 pF load is present. A 6 pF capacitor is therefore added to the 6 pF load of the oscillator circuit to compensate for the additional load that the crystal needs in order to oscillate at it's specified nominal frequency.

CRYSTAL CONFIGURATION WHEN 6 PF CRYSTAL IS NOT USED Figure 1



As mentioned, a crystal with a C_L of greater than 6 pF can be compensated with an external capacitor to improve the accuracy. However, it should be noted that the oscillator start–up time (the time it takes during initial power up for the oscillator to stabilize) will increase due to the increased capacitance in the feedback path of the oscillator. This capacitance decreases the loop gain of the oscillator which in turn increases the start–up time. For example, limited characterization has shown that the start–up time for a 6 pF crystal is typically less than a couple hundred milliseconds, but can increase to one or two seconds when a 12 pF crystal with a 6 pF capacitor in parallel are used.

NOISE AND CRYSTAL LAYOUT GUIDELINES

Since the crystal inputs of the Dallas Semiconductor real time clocks have a very high impedance (about 10^9 ohms), the leads to the crystal act like a very good antennae, coupling high frequency signals from the rest of the system. If a signal is coupled onto the crystal pins, it can either cancel out or add pulses. Since most of the signals on a board are much higher frequency than the 32.768 KHz crystal, it is more likely to add pulses where none are wanted. These noise pulses get counted as extra clock "ticks" and make the clock appear to run fast.

It is very simple to determine if noise is the cause of the inaccuracy of a real time clock. The following steps illustrate how this can be done.

1. Power the system up and synchronize the real time clock to a known accurate clock.
2. Turn system power off.
3. Wait for a period of time (2 hours, 24 hours, etc.). The longer the time period, the easier it will be to measure the accuracy of the clock.
4. Turn system on again, read clock, and compare to the known accurate clock.
5. Re–synchronize the real time clock to the known accurate clock.
6. Keep system powered up and wait for a period of time equal to the period in step 3.
7. Read clock after waiting for the above period of time and compare to the known accurate clock.

By using the above steps, the accuracy of the clock can be determined both when the system is powered up and when the system is powered down. If the clock proves to be inaccurate when the system is powered up, but is accurate when the system is powered down, the problem is most likely due to noise from other signals in the system. However, if the clock is inaccurate both when the system is powered up and when it is powered down, then the problem is not due to noise from the system.

Since it is possible for noise to be coupled onto the crystal pins, care must be taken when placing the external crystal on a PCB layout. It is very important to follow a few basic layout guidelines concerning the placement of the crystal on the PCB layout to insure that extra clock "ticks" do not couple onto the crystal pins.

1. It is important to place the crystal as close as possible to the X1 and X2 pins. Keeping the trace lengths between the crystal and the real time clock as small as possible reduces the probability of noise coupling by reducing the length of the "antennae". Keeping the trace lengths small also decreases the amount of stray capacitance.
2. Keep the crystal bond pads and trace width to the X1 and X2 pins as small as possible. The larger these bond pads and traces are, the more likely it is that noise can couple from adjacent signals.
3. If possible, place a guard ring (tied to ground) around the crystal. This helps to isolate the crystal from noise coupled from adjacent signals. See Figure 2 for an illustration of using a guard ring around a crystal.
4. Try to insure that no signals on other PCB layers run directly below the crystal or below the traces to the X1 and X2 pins. The more the crystal is isolated from other signals on the board, the less likely it is that noise will be coupled into the crystal.
5. It may also be helpful to place a local ground plane on the PCB layer immediately below the crystal guard ring. This helps to isolate the crystal from noise coupling from signals on other PCB layers. Note that the ground plane needs to be in the vicinity of the crystal only and not on the entire board. See Figure 2 for an illustration of a local ground plane. Note that the perimeter of the ground plane does not need to be larger than the outer perimeter of the guard ring.

   Note that care must be taken concerning the use of a local ground plane because of the stray capacitance that it introduces. This capacitance will be added to the crystal pins and if large enough could slow the clock down. Therefore, some factors must be taken into account when considering adding a local ground plane. For example, the capacitance due to the ground plane may be approximated by

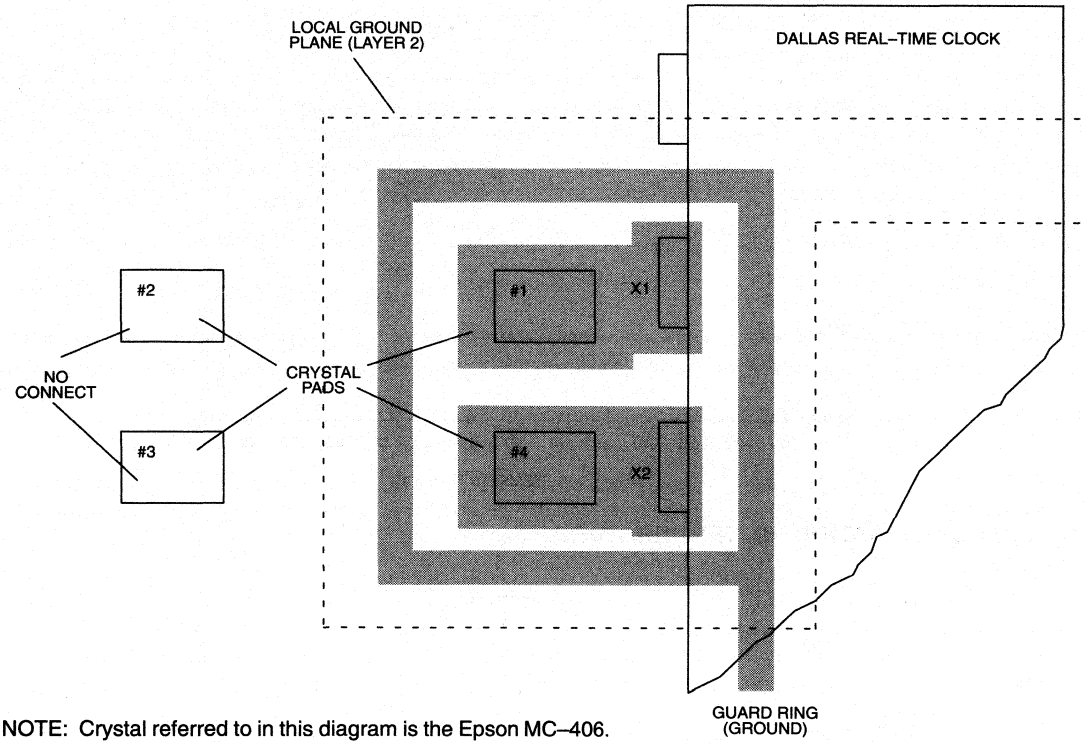
   $$C = \varepsilon A/t$$

   where

   ε = dielectric constant of the PCB
   A = area of the ground plane
   t = thickness of the PCB layer.

Therefore, to determine if a ground plane is appropriate for a given design, the above parameters must be taken into account to insure that the capacitance from the local ground plane is not sufficiently large enough to slow down the clock.

EXAMPLE OF CRYSTAL PLACEMENT ON PCB Figure 2



NOTE: Crystal referred to in this diagram is the Epson MC–406.

CLOCK ACCURACY OVER TEMPERATURE

The accuracy of a real time clock is directly dependent upon the frequency of the crystal. Therefore, since the resonant frequency of a crystal is dependent upon temperature, a real time clock will also be dependent upon temperature. The resonant frequency of a crystal is expressed in the following basic formula:

$$f = f0 + k * (T - T0)^2$$

where

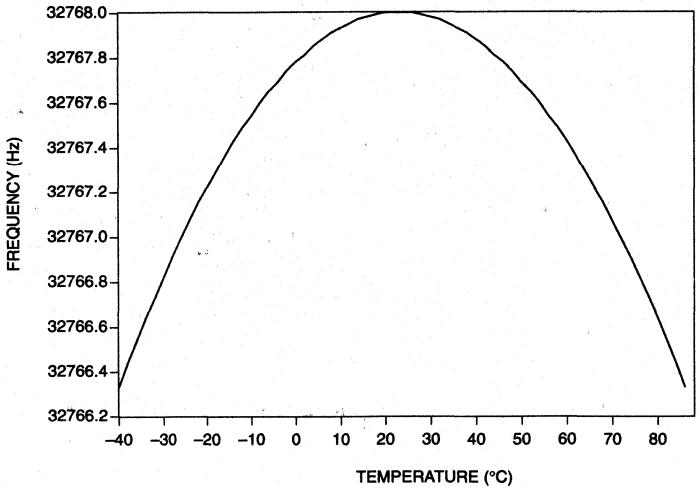
f_0 = nominal frequency
k = parabolic curvature constant
T_0 = turnover temperature
T = temperature

The values of the above parameters can be found in the data sheet of the crystal being used. The temperature characteristic of a nominal Daiwa crystal is illustrated in Figure 3 where $f_0 = 32.768$ KHz, $k = -0.042$ ppm/°C, and $T_0 = 23$°C. As can be seen in this figure, frequency has a parabolic relationship to temperature – as temperature deviates from the ideal 23°C, the crystal frequency becomes increasingly slower.

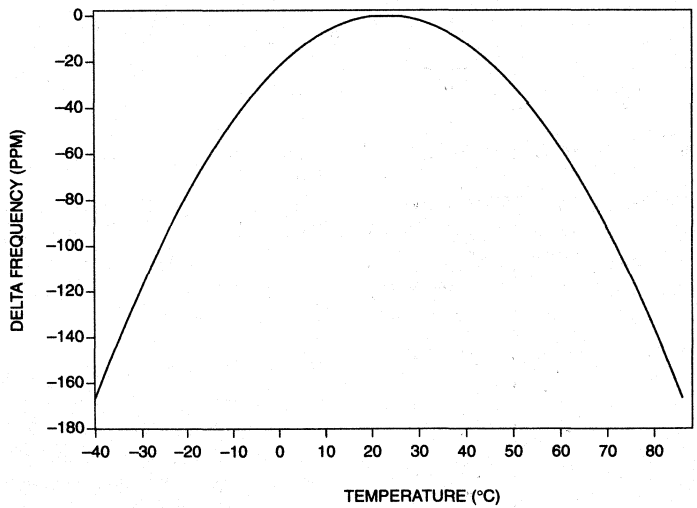
Figure 4 shows the same basic curve, however, the Y axis has been changed to show the frequency deviation (in ppm) from the crystal's nominal frequency at 23°C. This curve illustrates more clearly how the frequency of the crystal will affect the accuracy of the clock. A frequency deviation of 23 ppm translates into an accuracy of approximately ±1 minute per month. With this in mind, a quick glance at Figure 4 will give an approximate expected accuracy at a given temperature.

The above information should help to provide a basic understanding of how temperature will affect a Dallas Semiconductor real time clocks.

CRYSTAL FREQUENCY VS. TEMPERATURE Figure 3



FREQUENCY DEVIATION VS. TEMPERATURE Figure 4



TROUBLESHOOTING

This section is provided as a summary of the most frequent causes of real time clock inaccuracies. Most of these problems have been mentioned earlier, but are repeated here as a quick reference. This section has been divided into two parts. The first part will consider the factors that cause a real time clock to run too fast and the second part will consider the factors that cause a real time clock to run too slow.

FAST CLOCKS

The following are the most common scenarios that cause a crystal– based real time clock to run fast.

1. Noise coupling into the crystal from adjacent signals: This problem has been extensively covered above. Noise coupling will usually cause a real time clock to be grossly inaccurate.
2. Wrong crystal: A real time clock will typically run fast if a crystal with a specified load capacitance (C_L) greater than 6 pF is used. The severity of the inaccuracy is dependent on the value of the C_L. For example using a crystal with a C_L of 12 pF will cause the real time clock to be about 3–4 minutes per month fast.

SLOW CLOCKS

The following are the most common scenarios that cause a crystal–based real time clock to run slow.

1. Overshoot on real time clock input pins: It is possible to cause a real time clock to run slow by periodically stopping the oscillator. This can be inadvertently accomplished by noisy input signals to the real time clock. If an input signal rises to a voltage that is greater than a diode drop (~0.3V) above V_{DD}, the ESD protection diode for the input pin will forward bias, allowing the substrate to be flooded with current. This, in turn, will stop the oscillator until the input signal voltage decreases to below a diode drop above V_{DD}.

   This mechanism can cause the oscillator to stop frequently if input signals are noisy. Therefore, care should be taken to insure that there is no overshoot on input signals.

   Another situation that is common to overshoot problem is having an input to the real time clock at 5V when the real time clock is in battery back–up mode. This can be a problem in systems that systematically shut down certain circuits, but keep others powered up. It is very important to insure that there are no input signals to the real time clock that are greater than the battery voltage when the device is in battery back–up mode.
2. Wrong crystal: A real time clock will typically run slow if a crystal with a specified load capacitance (C_L) less than 6 pF is used. The severity of the inaccuracy is dependent on the value of the C_L.
3. Stray capacitance: Stray capacitance between the crystal pins can slow a real time clock down. Therefore care must be taken when designing the PCB layout to insure that the stray capacitance is kept to a minimum.
4. Temperature: The further the operating temperature is from the crystal turnover temperature, the slower the crystal will oscillate. See Figures 3 and 4.

REFERENCES

1. Eaton, S. S. *Timekeeping Advances Through COS/MOS Technology*, RCA Application Note ICAN–6086.
2. Eaton, S. S. *Micropower Crystal–Controlled Oscillator Design Using RCA COS/MOS Inverters*, RCA Application Note ICAN–6539.
3. Meyer, R. G. "MOS Crystal Oscillator Design," *IEEE Journal of Solid–State Circuits*, Vol. SC–15, No. 2, pp. 222–227, April 1980.
4. Williamson, T. *Oscillators for Microcontrollers*, Intel Application Note AP–155.

DALLAS SEMICONDUCTOR

Application Note 66
Watchdog Timekeeper

GENERAL OVERVIEW

Many applications require a real time clock to keep track of absolute time. Often times these same applications could benefit by being told to perform certain functions at specific times. The Watchdog Timekeeper family from Dallas Semiconductor is a solution to systems that need both an accurate real time clock and interrupt capabilities at specific times. In addition the Dallas Watchdog Timekeeper family also provides an upgradeable nonvolatile RAM path.

Dallas Watchdog Timekeepers provide basic real time clock functions. The devices keep track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The time is accurately maintained by a very low power oscillator. The Watchdog Timekeeper modules which contain the Watchdog integrated circuit as well as a crystal and lithium battery provide an accuracy of ±1 minute per month. Because of the low power oscillator, the internal lithium battery provides 10 years of continuous operation in the absence of system power.

The Dallas Watchdog Timekeeper family is made up of the DS1283 and DS1284 integrated circuits as well as the DS1286, DS1386, and DS1486 modules. Table 1 lists the different devices that belong to this family. As can be seen in the table, this family provides an upgradeable nonvolatile RAM growth path.

THE DALLAS WATCHDOG TIMEKEEPER FAMILY Table 1

DEVICE	NVRAM	
DS1283	50 bytes	IC
DS1284	50 bytes	IC
DS1286	50 bytes	Module
DS1386–08	8K bytes	Module
DS1386–32	32K bytes	Module
DS1486	128K bytes	Module

One benefit of using Dallas Watchdog Timekeepers is that the devices are simple to use since the real time clock registers are mapped directly into the device's onboard RAM. This makes accessing the timekeeping registers analogous to accessing a byte in RAM. See Figure 1 for the memory map of the DS1486, for example. Note that the real time clock registers occupy only the top 14 bytes of the memory.

An additional benefit that simplifies the design effort when using the Watchdog family is that the DS1386 and DS1486 pinouts are very close to the standard JEDEC bytewide pinout for SRAM's. The two interrupt outputs and the square wave output are the only pins that differ from the JEDEC pinout. See Figure 2 for a comparison of standard JEDEC bytewide pinouts compared to the pinouts of the DS1386 and the DS1486.

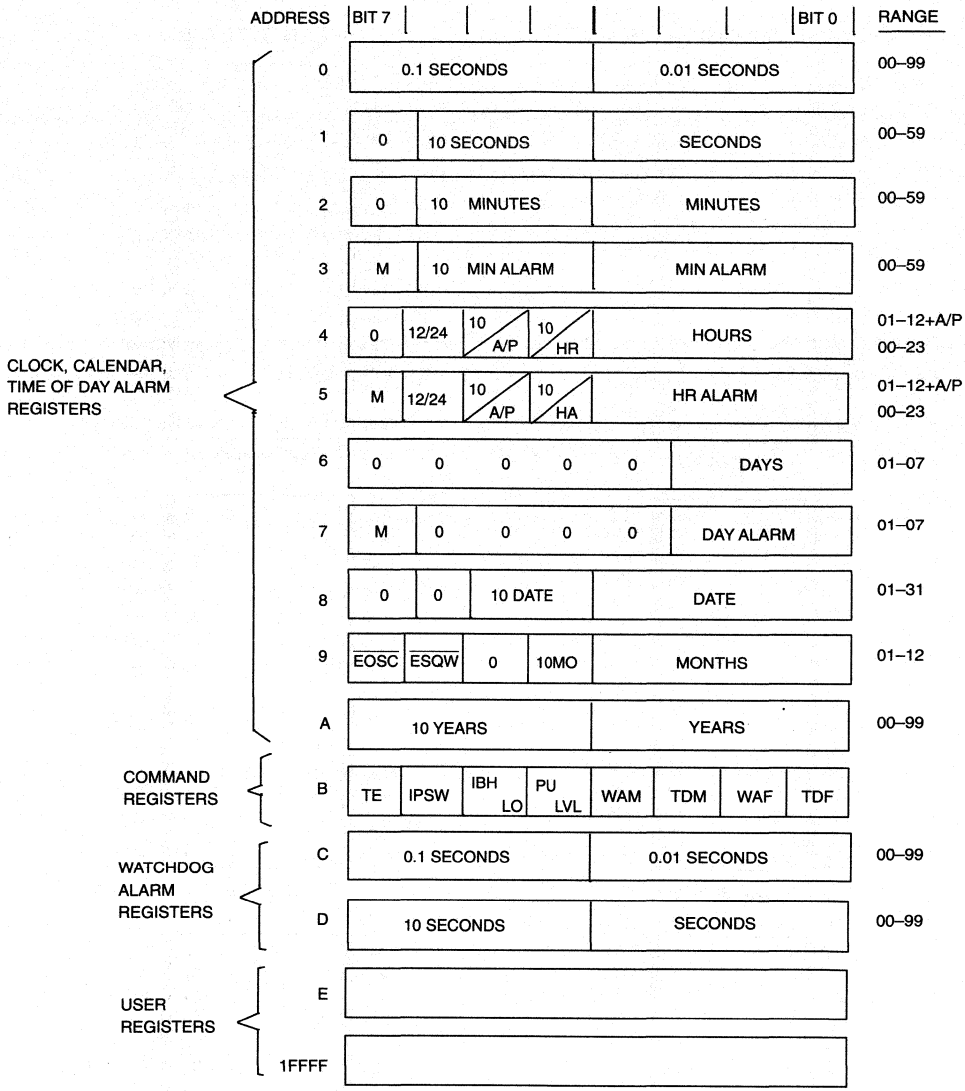
INTERRUPTS

A key feature of the Dallas Watchdog Timekeepers is that two different interrupt outputs are provided – a time of day alarm and a watchdog interrupt. These two interrupts are controlled by the Command Register, time of day alarm registers, and watchdog alarm registers. The Command Register allows flexibility in the operation of the interrupts. See Appendix for a complete description of the Command Register bits.

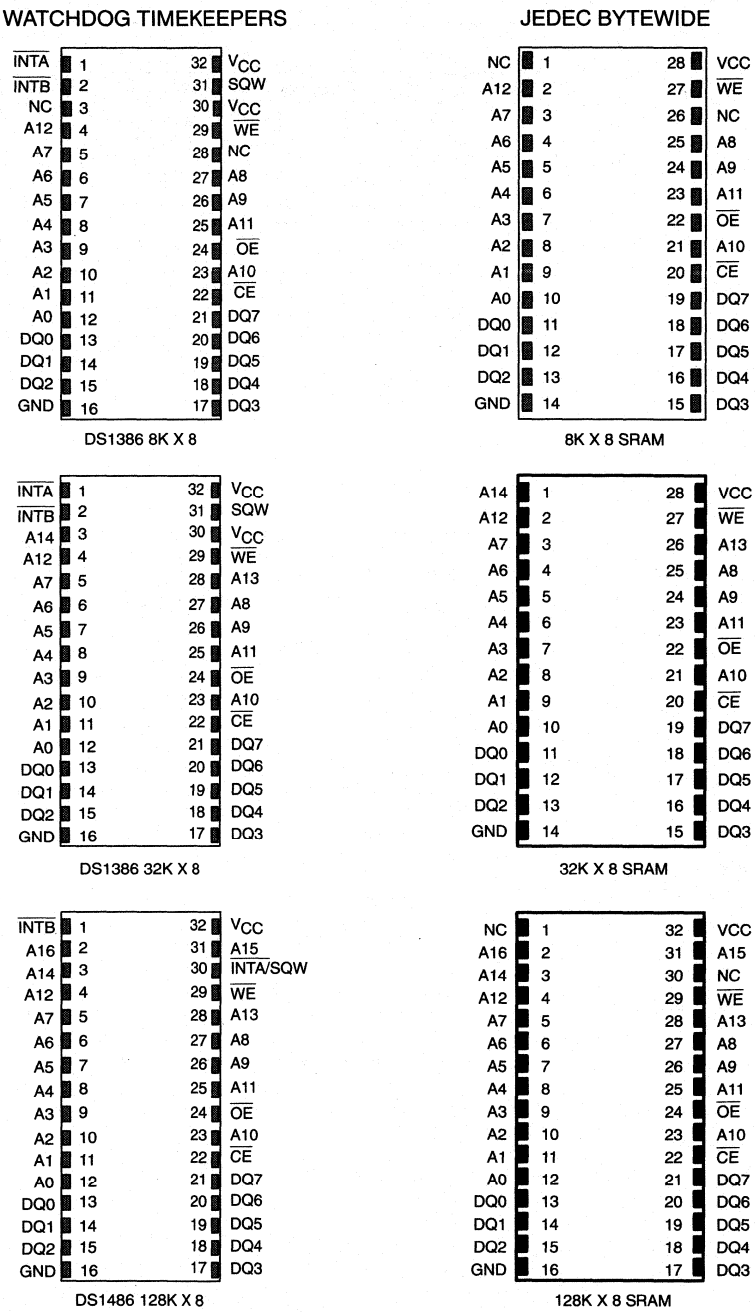
Time of Day Alarm

The first type of interrupt is the Time of Day Alarm. The Time of Day Alarm allows the user to program the device to generate an interrupt at a specific time of day for a specific day of the week. Special mask bits in the alarm registers also make it possible for this alarm to generate an interrupt once per minute, once per hour, or once per day.

DS1486 RAMIFIED TIMEKEEPER REGISTERS Figure 1



COMPARISON OF WATCHDOG TIMEKEEPER AND JEDEC BYTEWIDE PINOUTS Figure 2



Watchdog Alarm

The second type of interrupt is the Watchdog Alarm. The Watchdog Alarm allows the user to program the device to generate a periodic interrupt at a user defined interval. The user can program the device to generate an interrupt every 0.01 seconds to 100 seconds in 0.01 second increments. The watchdog interrupt is typically used in one of two different ways – as a microprocessor monitor or as a periodic interrupt.

Watchdog Alarm as Microprocessor Monitor

The Watchdog Alarm is often used as a microprocessor monitor in critical applications. In this function, the Watchdog Alarm is used to ensure that the microprocessor does not go out of control. For this type of application, the system is designed such that the microprocessor "checks in" with the Watchdog Timekeeper periodically by reading or writing to any of the watchdog alarm registers. Each time the microprocessor "checks in" with the Watchdog Timekeeper the watchdog timer is reset. If the microprocessor does not "check in" within the user specified watchdog interval, the Watchdog Alarm will generate an interrupt. This interrupt is used to reset the microprocessor. Figures 3 and 4 show two different ways that the Watchdog Timekeeper is interfaced with a microcontroller to monitor the system for an out of control condition.

In Figure 3, the interface between the DS1386–08 and the 68HC11 microcontroller is illustrated. In this diagram, $\overline{INTA}$ from the DS1386–08 is connected to the interrupt request (IRQ) pin of the 68HC11. In this example, the 68HC11 can be programmed such that it will reset the system if $\overline{INTA}$ is allowed to go active. Figure 4 illustrates the interface between the DS1386–08 and the 8051 microcontroller. In this example, the $\overline{INTA}$ pin is connected to one input of a 74LS122 one shot circuit. The output of the one shot is connected to the reset (RST) pin of the 8051. In this circuit, if the watchdog timer is allowed to time out, the $\overline{INTA}$ pin will go active, causing the one shot to provide a pulse to the 8051 reset and thus reset the 8051.

It should be noted that in both examples the interrupt output was not connected directly to the microcontroller reset. The reason for this is related to one of the options that is provided in the Command Register. The Command Register allows the interrupts to be programmed to generate either a pulse or a constant level signal in the event that the interrupts are activated. When the pulse option is provided, there is no problem with connecting the $\overline{INTA}$ output directly to the reset pin. However, if the constant level signal mode is selected, the microcontroller would be permanently locked in reset since there would be no way to clear the interrupt (since the interrupt output would permanently hold the microcontroller in reset). With this in mind, connecting the interrupts directly to the reset input is never recommended. Even if the designer programs the interrupts to run in pulse mode, it is still possible that the level mode could be accidentally activated by a software error which would cause the microcontroller to be permanently locked in reset.

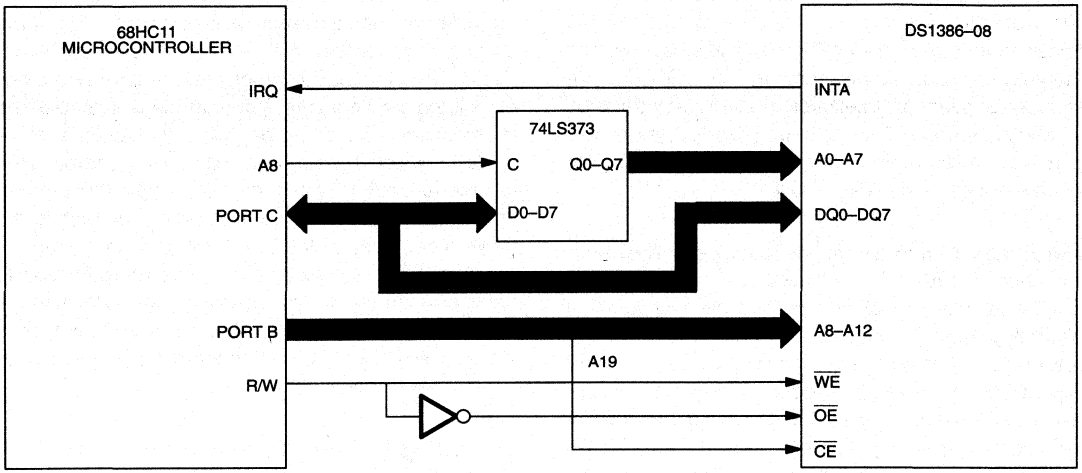
Watchdog As Periodic Interrupt

A second popular way that the Watchdog Alarm is used is as a periodic interrupt. In this case the Watchdog Timekeeper is programmed to generate an interrupt and, in contrast to the above example, the intention is to allow the interrupt to occur. In this example the device will generate an interrupt periodically at a user defined interval. Using the interrupt in this manner is useful, for example, in data acquisition equipment. The interrupt is used to tell the system to collect data each time it is activated. The circuit illustrated in Figure 3 could be used for this type of application. In this example the microcontroller could be programmed to gather data whenever an interrupt is activated.

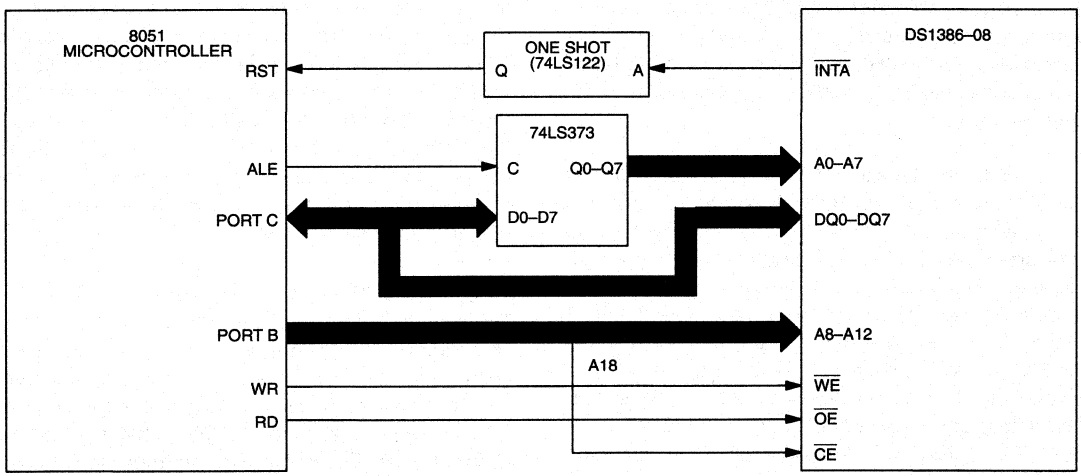
Interrupt as "Wake Up" Signal

One important feature of the interrupt outputs of the Watchdog Timekeeper is that they can be enabled even when system power is off and the device is in battery backed operation. This is particularly useful in applications where the system is shut off to conserve power when not in use. Either of the two interrupts can be used to "wake up" a system or specific circuitry within a system. The specified task can be completed and then the system can be shut off again. The system will remain powered down until the Watchdog Timekeeper tells the system to power up again. It should be mentioned that the interrupt outputs must be selected for active low operation to function when in battery backed mode.

WATCHDOG TIMEKEEPER INTERFACED WITH 68HC11 MICROCONTROLLER Figure 3



WATCHDOG TIMEKEEPER INTERFACED WITH 8051 MICROCONTROLLER Figure 4



One important consideration when using an interrupt to "wake up" a system is to insure that no pins on the Watchdog Timekeeper are interfacing with any logic that is at a greater potential than the battery voltage when system power is turned off. If a pin is at a potential that is greater than the battery voltage when the system power is turned off, this will cause the positive ESD (electro–static discharge) protection diode to forward bias. This allows current to flood the substrate of the Watchdog Timekeeper which in turn can cause the oscillator to stop.

IDEAL APPLICATIONS

Dallas Watchdog Timekeepers are ideally suited for many different types of applications. In general, this product family is a perfect fit for any system that requires a real time clock, nonvolatile RAM, and interrupt capabilities. Furthermore, the upgrade path in RAM densities make this product even more attractive for designers who see the potential need for greater RAM densities. The near–JEDEC bytewide footprint and the easy software interface with the Watchdog Timekeeper further its appeal as a simple product to use.

The interrupt outputs provided by the Watchdog Timekeepers offer much flexibility to a designer. These interrupts can be used to signal a system to perform an event at a specific time and/or can be used in critical applications to monitor the microprocessor to insure that it does not run "out of control." Additionally, the interrupts can be operated even when the device is in battery backed operation. This allows the designer to use the Watchdog Timekeeper to "wake up" a system.

TROUBLESHOOTING

The Dallas Watchdog Timekeepers have proven to be highly reliable and meet the published specifications. However, during the course of development, some common difficulties could be experienced. This section is provided as a summary of the most common problems that could be encountered and gives the solution to those problems.

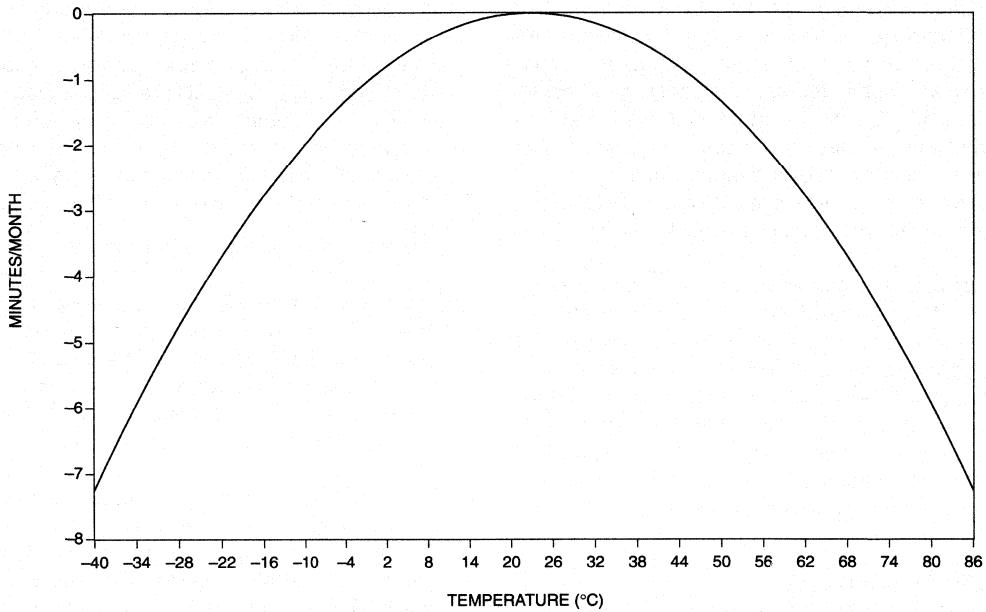
1. Clock is Inaccurate (i.e. greater than ±1 minute/ month at 25°C)

It is possible to cause the Watchdog Timekeeper to run slow by periodically stopping the oscillator. This can be caused inadvertently by noisy input signals to the Watchdog Timekeeper. If an input signal rises to a voltage that is greater than a diode drop (~0.3 volts) above V_{CC}, the ESD protection diode for the input pin will forward bias allowing the substrate of the device to be flooded with current. This, in turn, can stop the oscillator until the input signal voltage decreases to below a diode drop above V_{DD}.

There is a second scenario that can also cause the clock to appear to run slow. This scenario is similar to that above. If the Watchdog Timekeeper is in battery back–up mode, it is important to insure that none of the input signals are at a potential that is greater than the battery voltage. This needs to be considered especially for applications that use the interrupt signals when the Watchdog Timekeeper is in battery back–up operation. Since the interrupt outputs are open drain, they need to have external pull up resistors. When the Watchdog Timekeeper is in battery back–up operation, it is necessary to insure that the interrupts are not pulled up to a potential that is greater than the battery voltage, otherwise the ESD protection diode will be forward biased which can cause the oscillator to stop running.

Also, it should be mentioned that the Watchdog Timekeepers will be the most accurate when run at room temperature (25°C). Figure 5 illustrates the accuracy of a typical real time clock over temperature. As can be seen from the graph, timekeeping accuracy is temperature dependent and becomes less accurate the further the ambient temperature deviates from +25°C.

REAL TIME CLOCK ACCURACY OVER TEMPERATURE Figure 5



2. Interrupts Do Not Work

   A couple situations can cause this problem.

   l. The interrupt outputs are open drain. Therefore, $\overline{\text{INTA}}$ needs an external pull–up resistor and $\overline{\text{INTB}}$(INTB) needs an external pull–up resistor when set for active low operation and needs an external pull–down resistor when set for active high operation. If the pull–up or pull–down resistors are not used, the interrupts will not function properly.

   m. When in battery back–up operation, only active low mode can be used for $\overline{\text{INTB}}$(INTB). Active high mode for the $\overline{\text{INTB}}$(INTB) pin will not function when the Watchdog Timekeeper is in battery back–up mode.

3. Cannot Write to Real Time Clock

   Insure that the TE (Transfer Enable) bit has been set to a logic 1. This allows data written in the outer buffers to be transferred into the real time clock registers.

4. Clock will not run.

   Insure that the oscillator enable bit ($\overline{\text{EOSC}}$, bit 7 of register 9) is set to a logic 0.

5. Alarm Flags do not work .

   Alarm flags are set only as long as the corresponding interrupt output is active. Therefore when the interrupts are set to operate in pulse mode, the alarm flag will be set only during the active pulse of the interrupt. If level mode operation is selected, the interrupt will remain until the alarm condition is cleared.

APPENDIX: COMMAND REGISTER

Address location 0Bh is the Command Register where mask bits, control bits and flag bits reside. The operation of each bit is as follows:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TE	IPSW	IBH/LO	PU/LVL	WAM	TDM	WAF	TDF

TE (Bit 7 Transfer enable) - This bit when set to a logic 0 will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and reads or writes will not be affected with updates. This bit must be set to a logic 1 to allow updates.

IPSW (Bit 6 Interrupt switch) - When set to a logic 1, $\overline{\text{INTA}}$ is the Time of Day Alarm and INTB/($\overline{\text{INTB}}$) is the Watchdog Alarm. When set to logic 0, this bit reverses the output pins. $\overline{\text{INTA}}$ is now the Watchdog Alarm output and INTB/($\overline{\text{INTB}}$) is the Time of Day Alarm output.

IBH/LO (Bit 5 Interrupt B Sink or Source Current) - When this bit is set to a logic 1 and V_{CC} is applied, INTB/($\overline{\text{INTB}}$) will source current (see DC characteristics IOH). When this bit is set to a logic 0, INTB will sink current (see DC characteristics IOL).

PU/LVL (Bit 4 Interrupt pulse mode or level mode) - This bit determines whether both interrupts will output a pulse or level signal. When set to a logic 0, $\overline{\text{INTA}}$ and INTB/($\overline{\text{INTB}}$) will be in the level mode. When this bit is set to a logic 1, the pulse mode is selected and $\overline{\text{INTA}}$ will sink current for a minimum of 3 ms and then release. INTB/($\overline{\text{INTB}}$) will either sink or source current, depending on the condition of Bit 5, for a minimum of 3 ms and then release.

WAM (Bit 3 Watchdog Alarm Mask) - When this bit is set to a logic 0, the Watchdog Interrupt output will be activated. The activated state is determined by bits 1,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Watchdog interrupt output is deactivated.

TDM (Bit 2 Time of Day Alarm Mask) - When this bit is set to a logic 0, the Time of Day Alarm Interrupt output will be activated. The activated state is determined by bits 0,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1 , the Time of Day Alarm interrupt output is deactivated.

WAF (Bit 1 Watchdog Alarm Flag) - This bit is set to a logic 1 when a watchdog alarm interrupt occurs. This bit is read only.

The bit is reset when any of the Watchdog Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

TDF (Bit 0 Time of Day Flag) - This is a read only bit. This bit is set to a logic 1 when a Time of Day alarm has occurred. The time the alarm occurred can be determined by reading the Time of Day Alarm registers. This bit is reset to a logic 0 state when any of the Time of Day Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

DALLAS SEMICONDUCTOR

Application Note 77
DS1585/87, DS1685/87 and DS17X85/87 Accessing Extended User RAM via Software

GENERAL OVERVIEW

The DS1585/87, DS1685/87 and DS17X85/87 include an additional block of extended user RAM. The memory capacity of each device varies as follows; the DS1585/87 provides 65,536 bits organized in an 8K x 8 block, the DS1685/87 provides 1,024 bits organized in a 128 x 8 block, and the DS17X85/87 provides 16,384, 32,768 or 65,536, bits organized in 2K x 8, 4K x 8, or 8K x 8, blocks respectively.

REGISTER PARTITIONING

Figure 1 illustrates how the register blocks have been partitioned into two separate banks, bank 0 and bank 1. A bank select bit, DV0 located in control register 0Ah (bit 4), is used to select which register bank to make accessible. When DV0 is written to a logic 0, bank 0 is selected and an additional 64 bytes of user RAM can be accessed. However, when DV0 is written to a logic 1, bank 1 is selected and the additional features, including the extended user RAM, can be accessed. The real time clock (RTC), control registers, and 50 bytes of user RAM are accessible from either bank, independent of the DV0 bit.

SOFTWARE COMMUNICATION PORTS

The extended user RAM communication ports reside in the bank 1 register block. The extended user RAM address ports are located in registers 50h and 51h, while the extended user RAM data port is located in register 53h. Register 50h contains the LSB address and register 51h contains the MSB address. The DS1685/87 requires only seven bits to address the extended RAM and therefore does not require the MSB address register, 51h. These three bank 1 registers provide the software interface necessary to access the extended user RAM. The steps involved to read from and write to the extended RAM are listed below:

- Write the DV0 bit to a logic 1
- Write the LSB address to register 50h
- Write the MSB address (if required) to register 51h
- Read from or write to the data register, 53h

An automatic address increment feature, available with the DS17X85/87, simplifies the software required to access the extended user RAM. This feature can be enabled or disabled with a single bit, located in extended control register 4Ah, bit 5. This feature simplifies the software required to access consecutive RAM address locations.

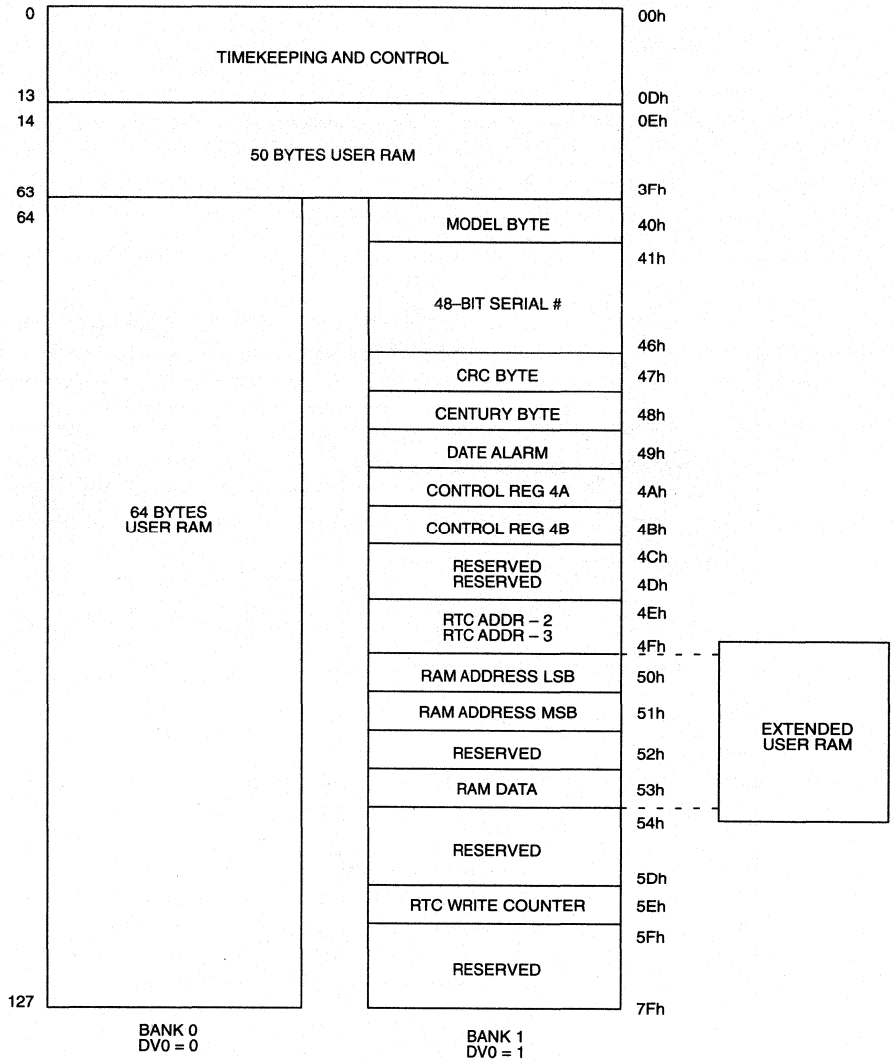
PROTOCOL FOR PC APPLICATIONS

The processor I/O ports used to access CMOS RAM are 70h and 71h. Port 70h is the CMOS RAM address register and port 71h is the CMOS RAM data register. The flow chart shown in Figure 2 illustrates the software protocol for PC applications.

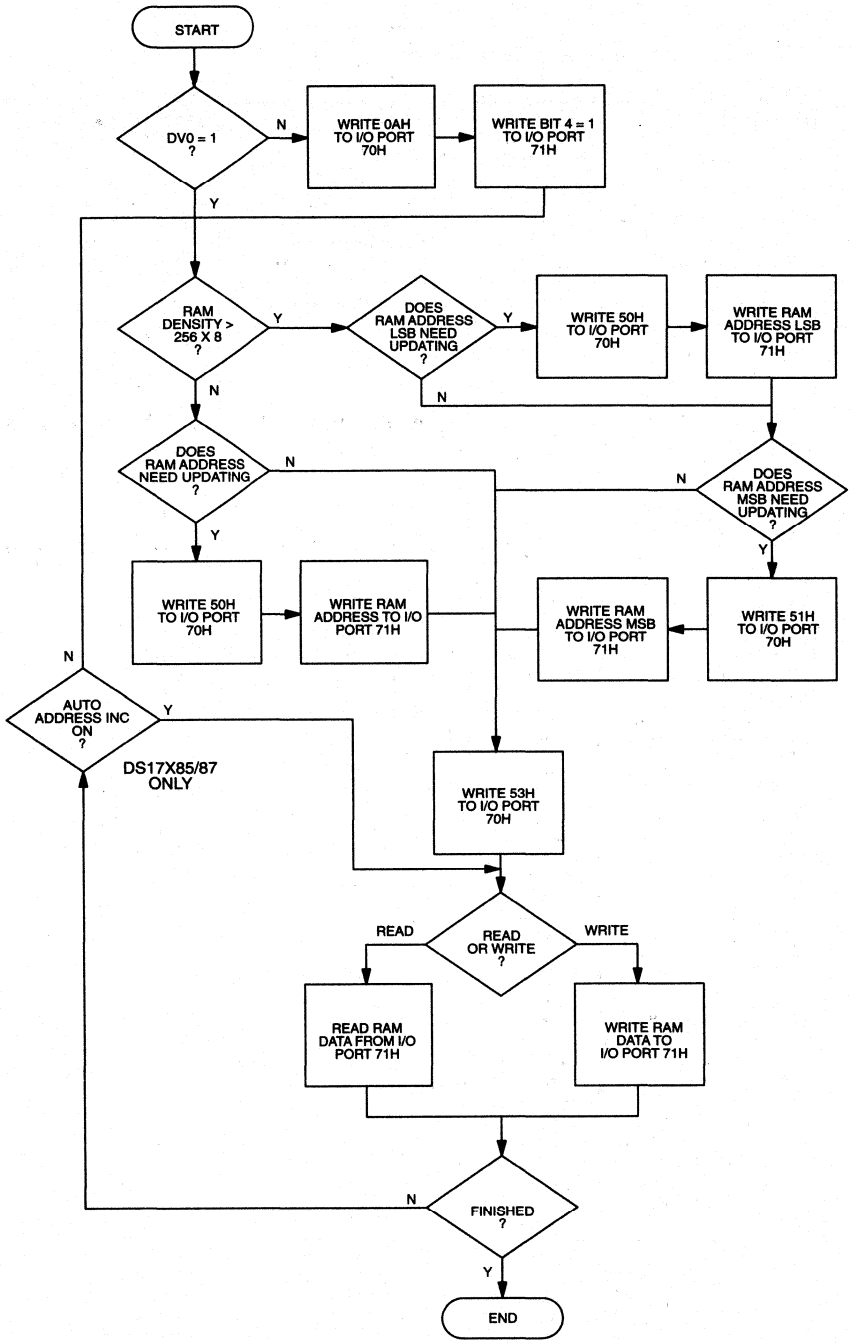
SUMMARY

The DS1585/87 also provides a hardware interface to access the extended user RAM, however, this requires additional hardware to implement. The extended user RAM software access method provides the user with the greatest flexibility when determining which RAM density is needed, without any hardware modifications, for the DS1685/87 and DS17X85/87 (2K, 4K, and 8K) devices.

REGISTER BLOCK PARTITIONING Figure 1



PC SOFTWARE PROTOCOL FLOW CHART Figure 2



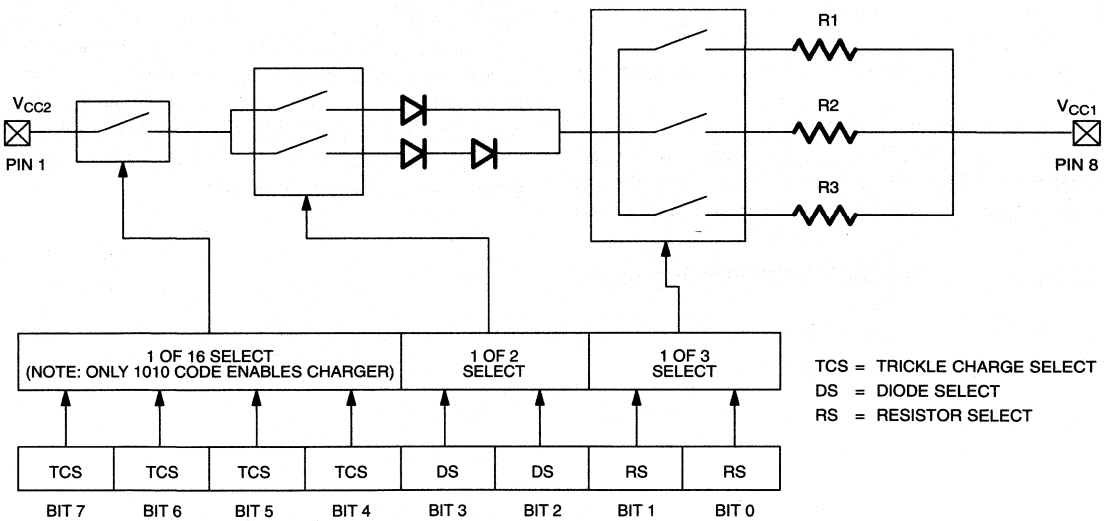
DALLAS SEMICONDUCTOR

Application Note 82
Using the Dallas Tricklecharge Timekeeper

DESCRIPTION

The Dallas Semiconductor DS1302 Trickle Charge Time Keeping Chip is a programmable 3–wire serial interface clock with a trickle charge circuit for using both rechargeable and non–rechargeable backup supplies. The real time clock/calendar provides seconds, minutes, hours, day, date, month, year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24–hour or 12–hour format with an AM/PM indicator. The DS1302 also provides 31 bytes of nonvolatile SRAM for data storage. Interfacing the DS1302 with a microprocessor is simplified by using a synchronous serial communication. Only three wires are required to communicate with the clock/RAM: (1) $\overline{RST}$ (Reset), (2) I/O (Data Line), and (3) SCLK (Serial Clock). Data can be transferred to and from the clock/RAM one byte at a time or in a burst of up to 31 bytes. The DS1302 is designed to operate on very low power and retain data and clock information on less than 1 microwatt. The DS1302 is designed to be completely compatible with designs that are currently using the DS1202. This compatibility allows the DS1302 to be dropped directly into a DS1202 socket. Then the optional trickle charge circuit on the DS1302 can be used to backup the system time and data with a super cap or a rechargeable battery.

DS1302 PROGRAMMABLE TRICKLE CHARGER Figure 1



TRICKLE CHARGER

The trickle charge circuit is shown in Figure 1 along with the trickle charge register. To enable the trickle charger the desired path through the circuit must be selected and the appropriate pattern written to the trickle charge register. The trickle charge select (TCS) bits (bits 4 – 7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 will enable the trickle charger. All other patterns will disable the trickle charger. The DS1302 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2 – 3) select whether one diode or two diodes are connected between V_{CC2} and V_{CC1}. If DS is 01, one diode is selected or if DS is 10, two diodes are selected. If DS is 00 or 11 the trickle charger is disabled independent of TCS. The RS bits (bits 0 – 1) select the resistor that is connected between V_{CC2} and V_{CC1}. The resistor selected by the resistor select (RS) bits is as follows:

RS BITS	RESISTOR	TYPICAL VALUE
00	None	None
01	R1	2KΩ
10	R2	4KΩ
11	R3	8KΩ

If RS is 00 the trickle charger is disabled independent of TCS.

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to V_{CC2} and a super cap is connected to V_{CC1}. Also, assume that the trickle charger has been enabled with 1 diode and resistor R1 between V_{CC2} and V_{CC1}. The maximum current I_{MAX} would therefore be calculated as follows:

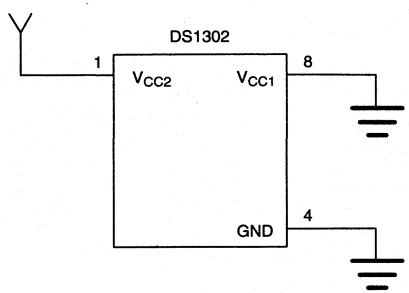
$$I_{MAX} = (5.0V - \text{diode drop})/R1$$
$$\sim(5.0V - 0.7V)/ 2K\Omega$$
$$\sim 2.2\ mA$$

Obviously, as the super cap charges, the voltage drop between V_{CC2} and V_{CC1} will decrease and therefore the charge current will decrease (please see curves in Trickle Charger Characteristics section).

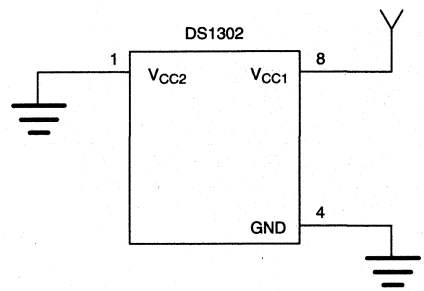
POWER CONTROL

The DS1302 can be powered in several different ways. The first method, shown in Figure 2, illustrates the DS1302 being supplied by only one power supply. In Figure 2a the power supply is connected to V_{CC2} (pin 1) and in Figure 2b the power supply is connected to V_{CC1} (pin 8). In each case the unused power pin, V_{CC1} or V_{CC2}, is grounded. The second method, Figure 3, illustrates the DS1302 being backed up using a non–rechargeable battery connected to V_{CC1}. In these two cases the trickle charge circuit has been disabled. In the final case, Figure 4, the DS1302 is being backed up by connecting a super cap, Figure 4a, or a rechargeable battery, Figure 4b, to V_{CC1}. In this case the trickle charge circuit has been enabled.

SINGLE POWER SUPPLY OPTION Figure 2

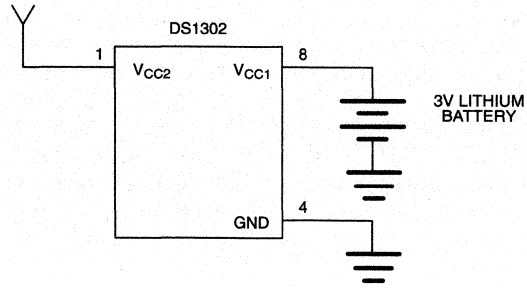


2a

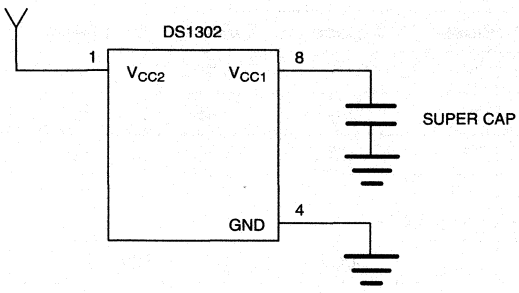


2b

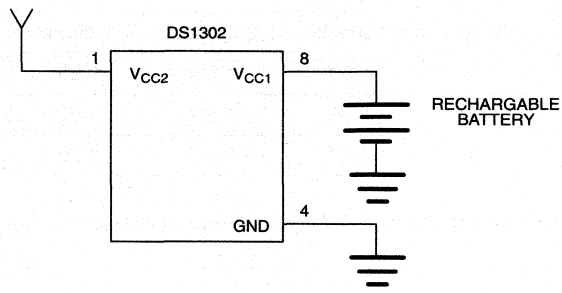
NON–RECHARGEABLE BATTERY BACKUP Figure 3



SUPER CAP OR RECHARGEABLE BATTERY BACKUP Figure 4



4a



4b

TRICKLE CHARGE CHARACTERISTICS

Charging the Super Cap – As was discussed earlier the maximum current, I_{MAX}, required by the trickle charge circuit can be calculated by inserting the correct values selected in the trickle charge register into the following equation:

$$I_{MAX} = (V_{CC2} - \text{diode drop})/R$$

Table 1 contains the values of I_{MAX} for V_{CC2} values of 4.5V, 5.0V and 5.5V; 1 diode drop and 2 diode drops; resistor values of 2000Ω, 4000Ω and 8000Ω.

Also, the charging current can be modeled as a function of charge time. Both the super cap voltage and charging current as a function of time are represented in Figure 5. The equation to model the super cap voltage as a function of time is

$$V(t) = V_{MAX}\,[1-e^{(-t/RC)}]$$

where:

V(t) – Super Cap Voltage
V_{MAX} – (V_{CC2} – n Diode Drops), n=1,2
R – Internal Trickle Charge Resistor
C – Super Cap Capacitance

The time needed to charge the super cap to 95% of V_{MAX} is given in Table 2. Note that the time required to charge the super cap to 95% of the value of V_{MAX} is independent of the value of V_{MAX}. The equation which models the charging current as a function of time is given as

$$I(t) = V_{MAX}/R * e^{(-t/RC)}$$

where:

I(t) – Charging Current
V_{MAX} – (V_{CC2} – n Diode Drops), n=1,2
R – Internal Trickle Charge Resistor
C – Super Cap Capacitance

Discharging the Super Cap – When modeling the DS1302 for the time to discharge the super cap the DS1302 characterization data was used to observe that the I_{CC1T}, Time Keeping Current through V_{CC1}, was linear. This implies that it is proper to represent the DS1302 as a resistive load, R_L, through which the super cap will be discharged. Using the data sheet spec of I_{CC1T} max of 0.3 µA at 2.5 V_{CC1} gives a value for R_L of 8.3MΩ. Then the equation modeling the discharging of the super cap is given by

$$V(t) = V_{MAX} * e^{(-t/R_L C)}$$

where:

V(t) – Super Cap Voltage
V_{MAX} – (V_{CC2} – n Diode Drops), n=1,2
R_L – DS1302 Load Resistance
C – Super Cap Capacitance

The calculated values for the time required to discharge the super cap to 2V are given in Table 3 and a sample of the super cap voltage as a function of discharge time is given in Figure 6.

CALCULATED VALUES OF I_{MAX} Table 1

	2000Ω		4000Ω		8000Ω		
V_{CC2}	1 diode	2 diodes	1 diode	2 diodes	1 diode	2 diodes	UNITS
4.5V	1.90	1.55	0.95	0.78	0.48	0.39	mA
5.0V	2.15	1.80	1.08	0.90	0.54	0.45	mA
5.5V	2.40	2.05	1.20	1.03	0.60	0.51	mA

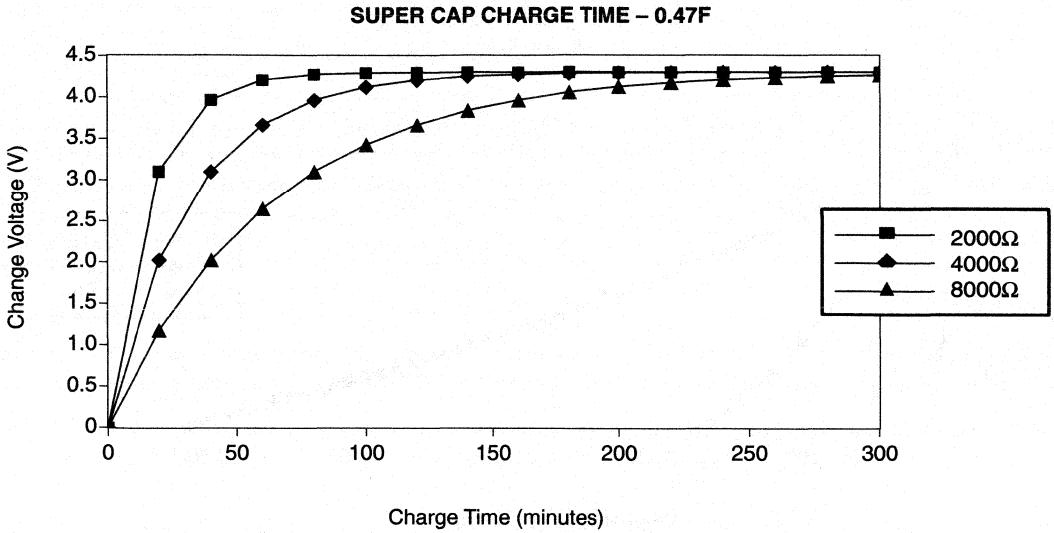
CHARGING TIME FOR SUPER CAP TO 95% OF V_{MAX} Table 2

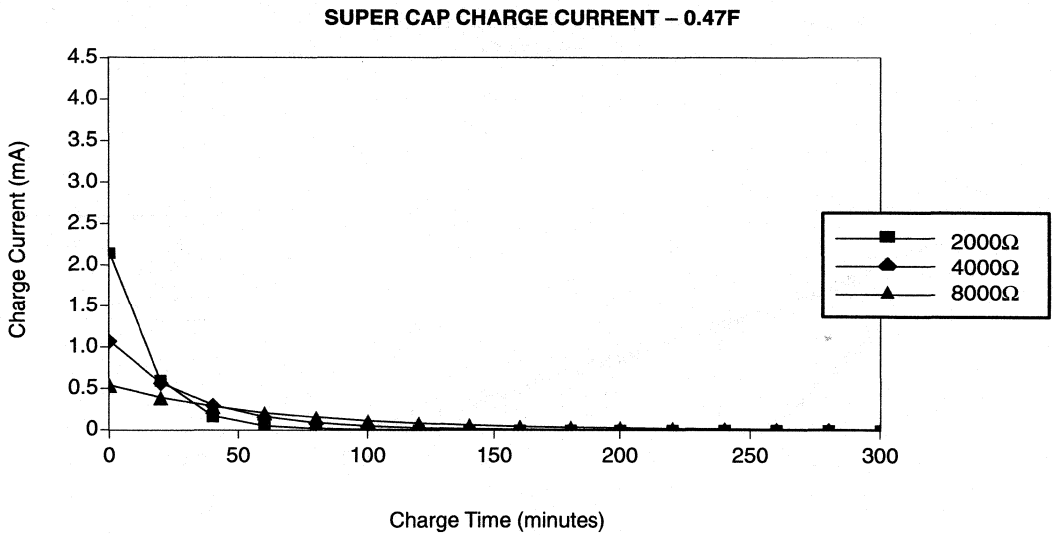
	2000Ω	4000Ω	8000Ω	UNITS
Super Cap=0.047 F	4.7	9.4	18.8	minutes
Super Cap=0.47 F	46.9	93.9	187.7	minutes
Super Cap=1.5 F	149.8	299.6	599.2	minutes

SUPER CAP DISCHARGE TIME TO 2V Table 3

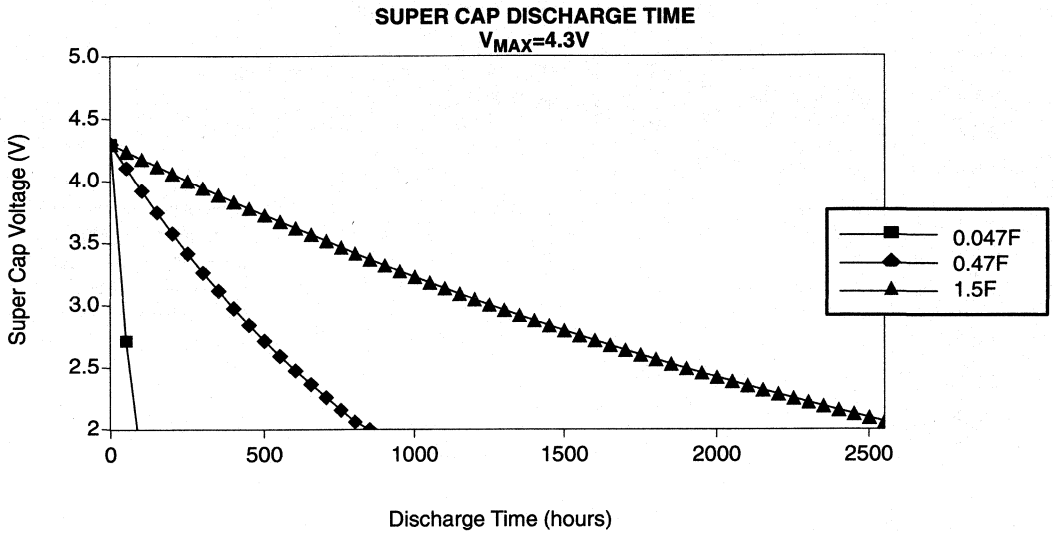
	0.047F		0.47F		1.5F		
V_{CC2}	1 diode	2 diodes	1 diode	2 diodes	1 diode	2 diodes	UNITS
4.5V	69.8	47.7	698.3	476.8	2228.7	1521.7	hours
5.0V	83.3	63.9	832.8	639.5	2657.9	2040.9	hours
5.5V	95.2	78.1	952.5	780.9	3039.8	2492.5	hours

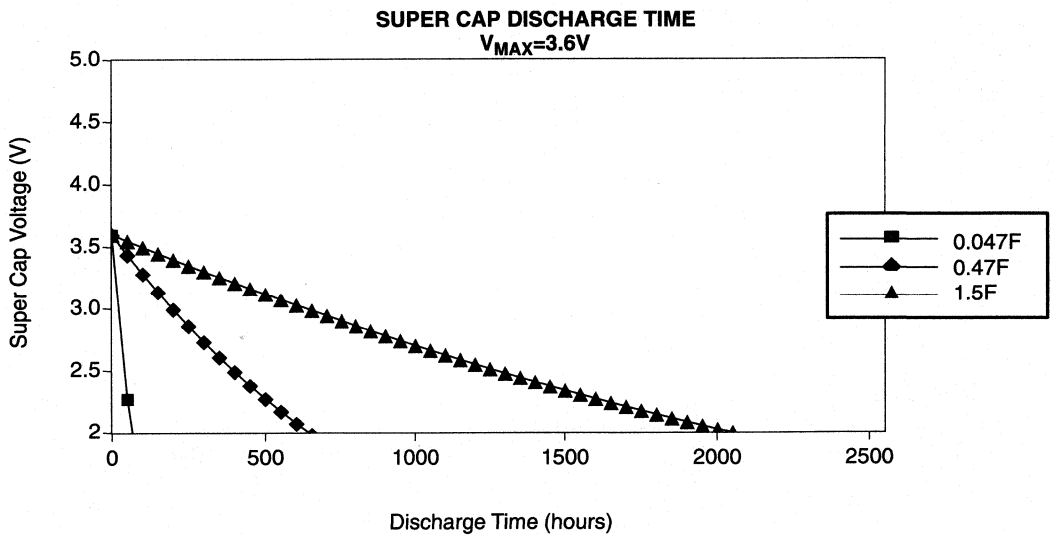
SUPER CAP CHARGING CHARACTERISTICS Figure 5





SUPER CAP DISCHARGING CHARACTERISTICS Figure 6





DALLAS SEMICONDUCTOR

Application Note 90
Using the PC Clock Extended Features

DESCRIPTION

This application note discusses the extended features for the following PC Real Time Clocks (RTCs): DS1585/7, DS1685/7, DS1688/91, DS17285/7, DS17485/7,DS17A84/6, and DS17885/7. Also included is an initialization flow chart for the PC RTCs. All of these devices incorporate these extended features unless otherwise noted.

EXTENDED FEATURES

Auxiliary Battery Input (V_{BAUX}):

The auxiliary battery input, V_{BAUX}, provides the power required to use the kickstart, wake up, power–on output, and the 32 KHz square wave in the absence of system power. The timekeeping and RAM data can also be maintained by this power source. If this input is going to be used, bit 7 in control register 4Bh (ABE) must be set to a logic 1. If this input is not going to be used then ABE must be set to a logic 0 and the V_{BAUX} input tied to ground.

Kickstart Input ($\overline{KS}$):

The kickstart pin is intended to be used in the battery backed mode in conjunction with the $\overline{PWR}$ signal providing systems with power management control. A signal providing a ground closure will force the $\overline{PWR}$ signal to transition low. The $\overline{KS}$ pin can also be used as an interrupt input while V_{CC} is applied.

Power–On Output ($\overline{PWR}$):

This output is open drain and requires an external pull–up resistor for proper operation. This signal is intended to be used in conjunction with $\overline{KS}$ and the wakeup alarm for power management features.

32 KHz Square Wave Output (SQW):

The SQW output pin can provide a 32 KHz square wave for power management purposes. The DS1685/7, DS1688/91, DS17285/7, DS17485/7, and DS17885/7 will provide the 32 KHz each time the system power, V_{CC}, is applied. The DS1585/7, DS1689/93, and DS17A84/6 must be programmed, to output the 32 KHz, after the system power is applied.

Silicon Serial Number:

A unique 64–bit silicon serial number is located in bank 1 registers 40h – 47h. The serial number is divided into three separate parts. The first byte, location 40h, contains a model number to identify the device type and revision. The following is a list of the model numbers currently assigned for the devices mentioned above:

Model #	Part #
70h	DS1585/7
71h	DS1685/7
72h	DS17285/7
73h	DS1688/91
73h	DS1689/93
74h	DS17485/7
78h	DS17885/7

The second part of the serial number is a unique 48–bit binary number located in registers 41h – 46h. The third part of the serial number is located in register 47h and contains a CRC number used to validate the data in registers 40h – 46h. This eight byte serial number is read only.

Century Byte:

The century byte, located in bank 1 register 48h, will update every 100 years keeping track of the century.

Date Alarm Byte:

The date alarm byte, located in bank 1 register 49h, can be used in conjunction with the time of day alarm providing a system with a wakeup alarm programmable up to 31 days.

Control Registers 4Ah and 4Bh:

See the REGISTER DESCRIPTION section.

Extended RAM Software Port:

The extended user RAM can be accessed through software via three internal registers located in bank 1 locations 50h, 51h, and 53h. Locations 50h and 51h are used for the RAM address and location 53h is used for the data transfer. This unique feature eliminates the need for external hardware and at the same time provides the ability to switch RAM densities without any hardware modification required. This feature is not available on the DS1688/91 or DS1689/93.

V_{CC} Elapsed Time Counter:

A 32–bit V_{CC} powered elapsed time counter, located in bank 1 registers 54h (LSB) through 57h (MSB), will keep track of how long system power has been applied. This counter will update once per second as long as V_{CC} is within nominal limits and the oscillator and countdown chain are enabled. When V_{CC} falls outside of the nominal limits the counter is halted and the elapsed time is retained. This counter can be read or written at the users discretion. This feature is available only on the DS1688/91 and DS1689/93.

VBAT Elapsed Time Counter:

A 32–bit VBAT powered elapsed time counter, located in bank 1 registers 58h (LSB) through 5Bh (MSB), will keep track of how long the system has been in service. This counter will run continuously and update once per second as long as VBAT or V_{BAUX} is within nominal limits and the oscillator and countdown chain are enabled. This counter can be read or written at the users discretion. This feature is available only on the DS1688/91 and DS1689/93.

Power Cycle Counter:

A 16–bit power cycle counter, located in bank 1 registers 5Ch (LSB) and 5Dh (MSB), will keep track of the number of times a system is powered on and off. Each time system power, V_{CC}, is applied within nominal limits, the counter will be incremented by one. This counter can be read and written at the users discretion. This feature is available only on the DS1688/91 and DS1689/93.

Additional Serial Number:

An additional 64–bit customer specific serial number or ROM is located in bank 1 registers 60h through 67h. This feature is available only on the DS1688/91 and DS1689/93.

Burst Mode:

The DS17285/7, DS17485/7, and DS17885/7 are the only devices which provide the burst mode option. The model byte uniquely identifies these devices as having burst mode.

REGISTER DESCRIPTION

LOCATION	DESCRIPTION	
0Ah	Control Register A	
	Bit 7	Update In Progress (UIP) – (read only) 0=time/date can be read 1=update in progress
	Bits 6 – 4	Oscillator Control (DV2–DV0) DV2=countdown chain 0=countdown chain enabled 1=resets countdown chain only if DV1=1 DV1=oscillator enable 0=oscillator off 1=oscillator on DV0=bank select 0=original bank 1=extended registers
	Bits 3 – 0	Rate Selection (RS3–RS0) These bits define the square wave output frequency and the periodic interrupt rate.

LOCATION	DESCRIPTION	
0Bh	Control Register B	
	Bit 7	Halt Clock Updates (SET) 0=updates time/date once per second 1=time/date updates are inhibitied
	Bit 6	Periodic Interrupt Enable (PIE) 0=disabled 1=enabled
	Bit 5	Alarm Interrupt Enable (AIE) 0=disabled 1=enabled
	Bit 4	Update–Ended Interrupt Enable (UIE) 0=disabled 1=enabled
	Bit 3	Square Wave Enable (SQWE) 0=disabled 1=enabled
	Bit 2	Time and Date Data Mode (DM) 0=binary coded decimal (BDC) format 1=binary format
	Bit 1	Hour Format (24/12) 0=12 hour mode 1=24 hour mode
	Bit 0	Daylight Savings Time Enable (DSE) 0=disabled 1=enabled

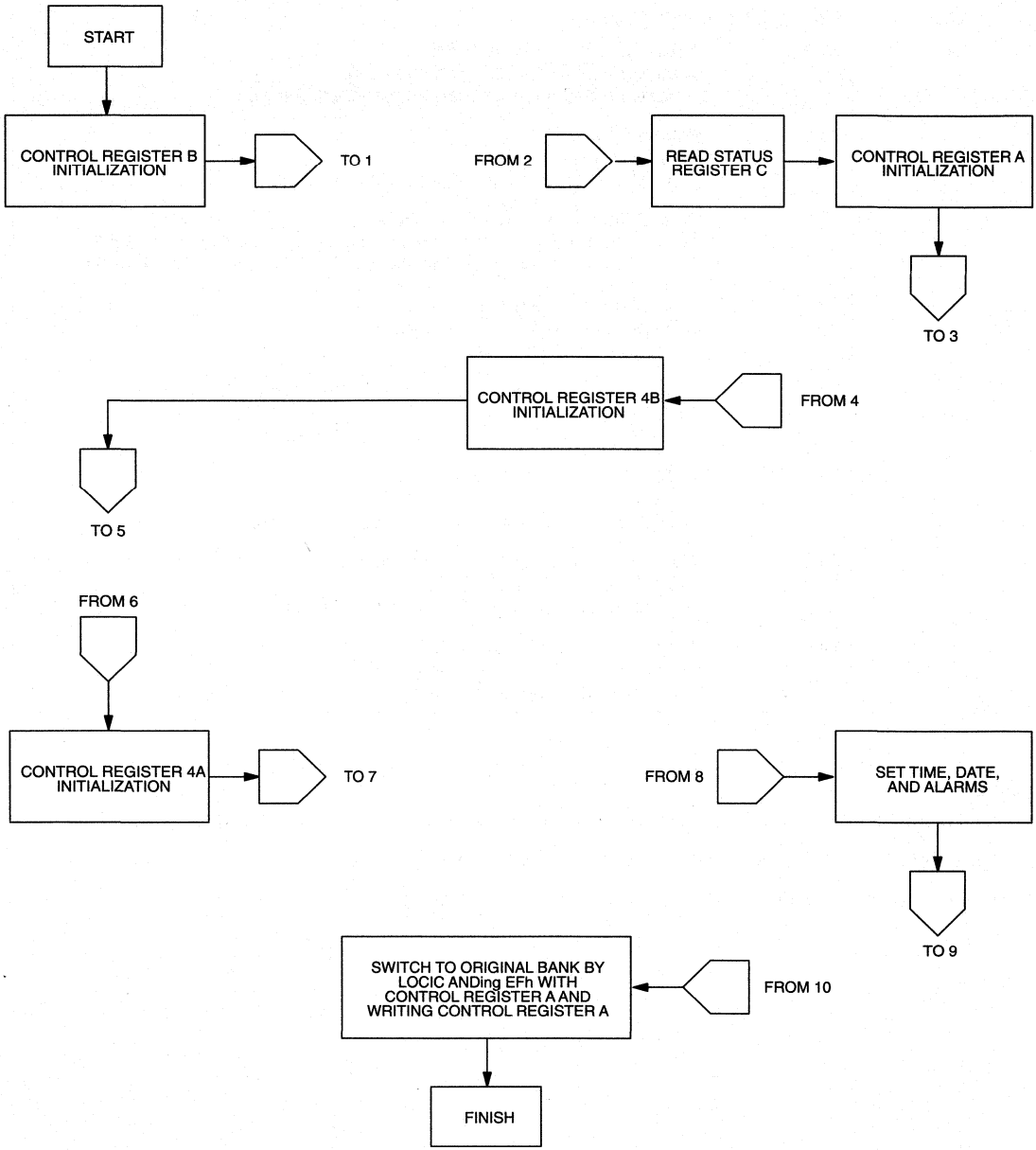
LOCATION	DESCRIPTION
0Ch	Status Register C (read only) Bit 7 Interrupt Request Flag (IRQF) – (read only) Bit 6 Periodic Interrupt (PF) – (read only) Bit 5 Alarm Interrupt Flag (AF) – (read only) Bit 4 Update–Ended Interrupt Flag (UF) – (read only) Bits 3 – 0 Reserved (read only logic 0)
0Dh	Status Register D (read only) Bit 7 Valid RAM and Time (VRT) – (read only) 0=battery low; CMOS RAM invalid 1=battery good; CMOS RAM valid Bits 6 – 0 Reserved (read only logic 0)
04Ah	Extended Control Register 4A Bit 7 Valid RAM and Time 2 (VRT2) – (read only) 0=auxiliary battery is low 1=auxiliary battery is good Bit 6 Increment in Progress (INCR) – (read only) 0=time/date has been updated 1=time/date is incrementing and checking alarms Bit 5 Burst Mode Enable (BME) – See Note 1 0=single byte extended RAM reads and writes 1=auto increments address for extended RAM reads and writes Bit 4 Reserved Bit 3 Power Active Bar (PAB) 0=$\overline{\text{PWR}}$ pin is in the active low state 1=$\overline{\text{PWR}}$ pin is in the inactive high state Bit 2 RAM Clear Flag (RF) 0=cleared state (must be written) 1=high to low transition detected on $\overline{\text{RCLR}}$ if RCE=1 Bit 1 Wakeup Alarm Flag (WF) 0=cleared state (must be written) 1=wakeup alarm condition has occured Bit 0 Kickstart Flag (KF) 0=cleared state (must be written) 1=high to low transition detected on $\overline{\text{KS}}$ input

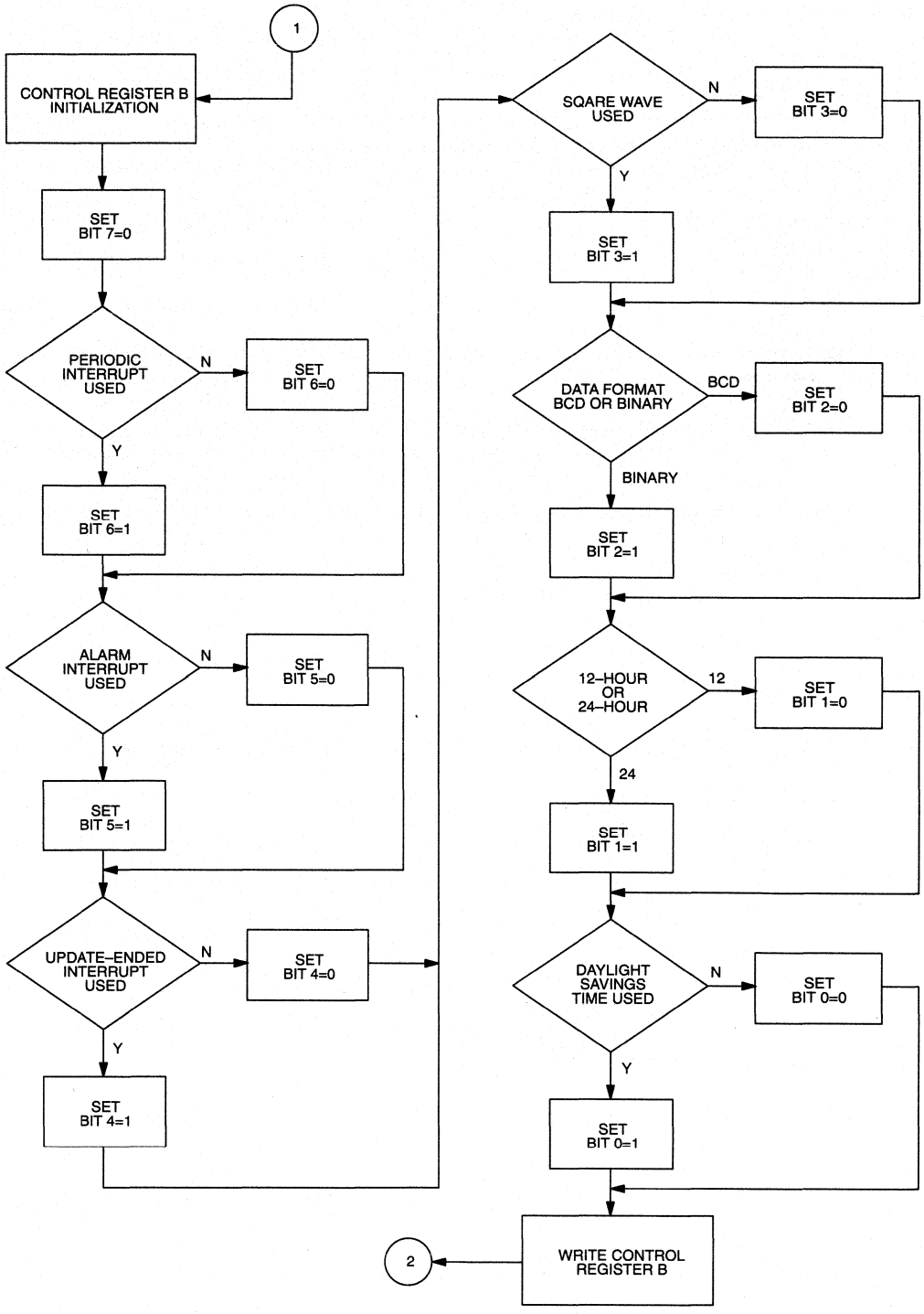
LOCATION	DESCRIPTION
04Bh	Extended Control Register 4B
	Bit 7 Auxiliary Battery Enable (ABE) 0=auxiliary battery input not being used 1=auxiliary battery input used for extended features
	Bit 6 Enable 32 KHz (E32K) 0=32 KHz disabled 1=32 KHz enabled to be output on the SQW pin
	Bit 5 Crystal Selection (CS) – See Note 2 0=oscillator configured for a crystal with a load capacitance of 6 pF 1=oscillator configured for a crystal with a load capacitance of 12.5 pF
	Bit 4 RAM Clear Enable (RCE) 0=RAM clear function is disabled 1=allows $\overline{\text{RCLR}}$ pin to clear user RAM
	Bit 3 Power Active Bar Reset Select (PRS) – See Note 3 0=$\overline{\text{PWR}}$ pin will go High–Z when entering power fail 1=$\overline{\text{PWR}}$ pin remains active when entering power fail
	Bit 2 RAM Clear Interrupt Enable (RIE) 0=disabled 1=enables RAM clear function to generate interrupts
	Bit 1 Wakeup Alarm Interrupt Enable (WIE) 0=disabled 1=enables wakeup alarm to generate interrupts
	Bit 0 Kickstart Interrupt Enable (KSE) 0=disabled 1=enables $\overline{\text{KS}}$ to generate interrupts

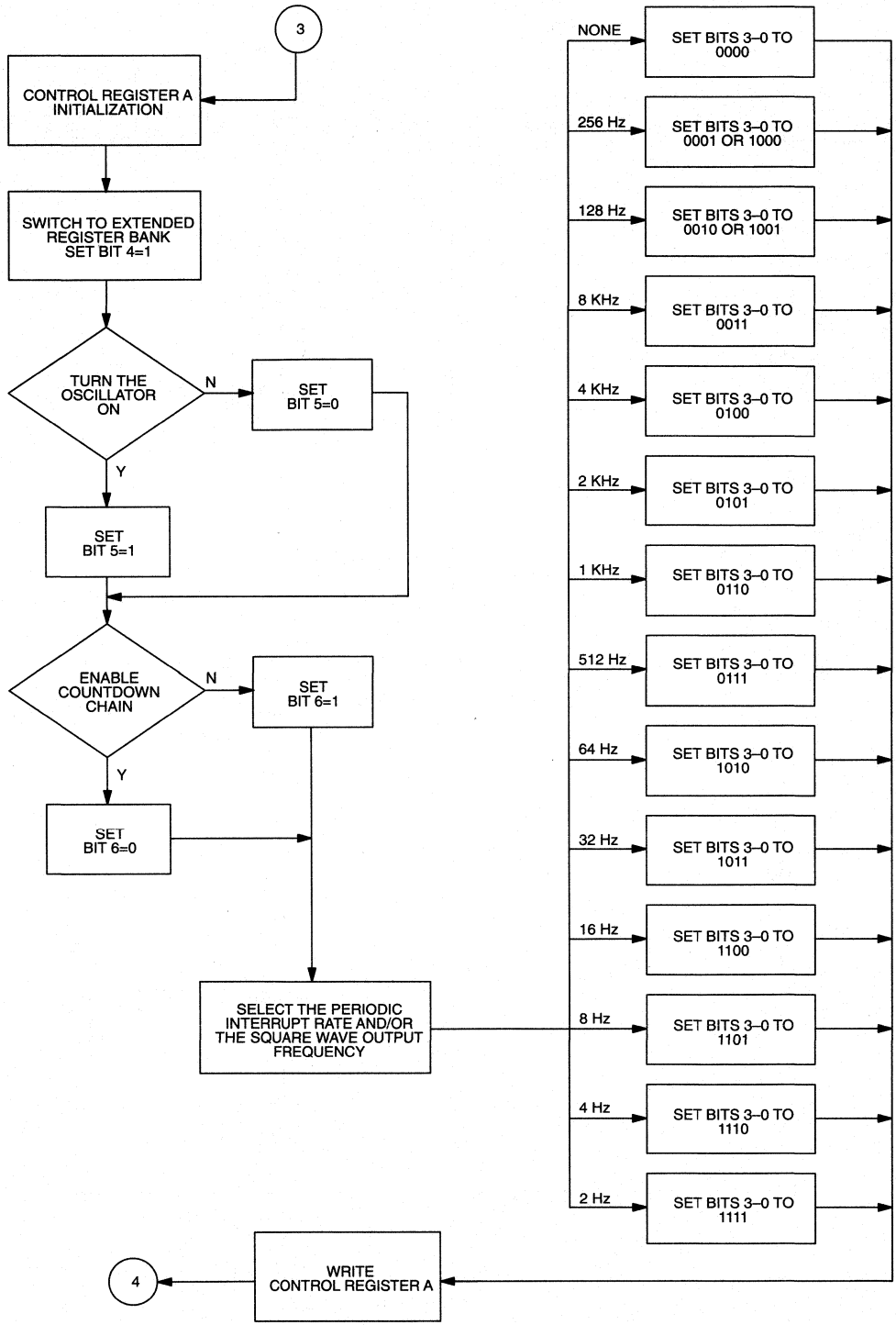
NOTES:

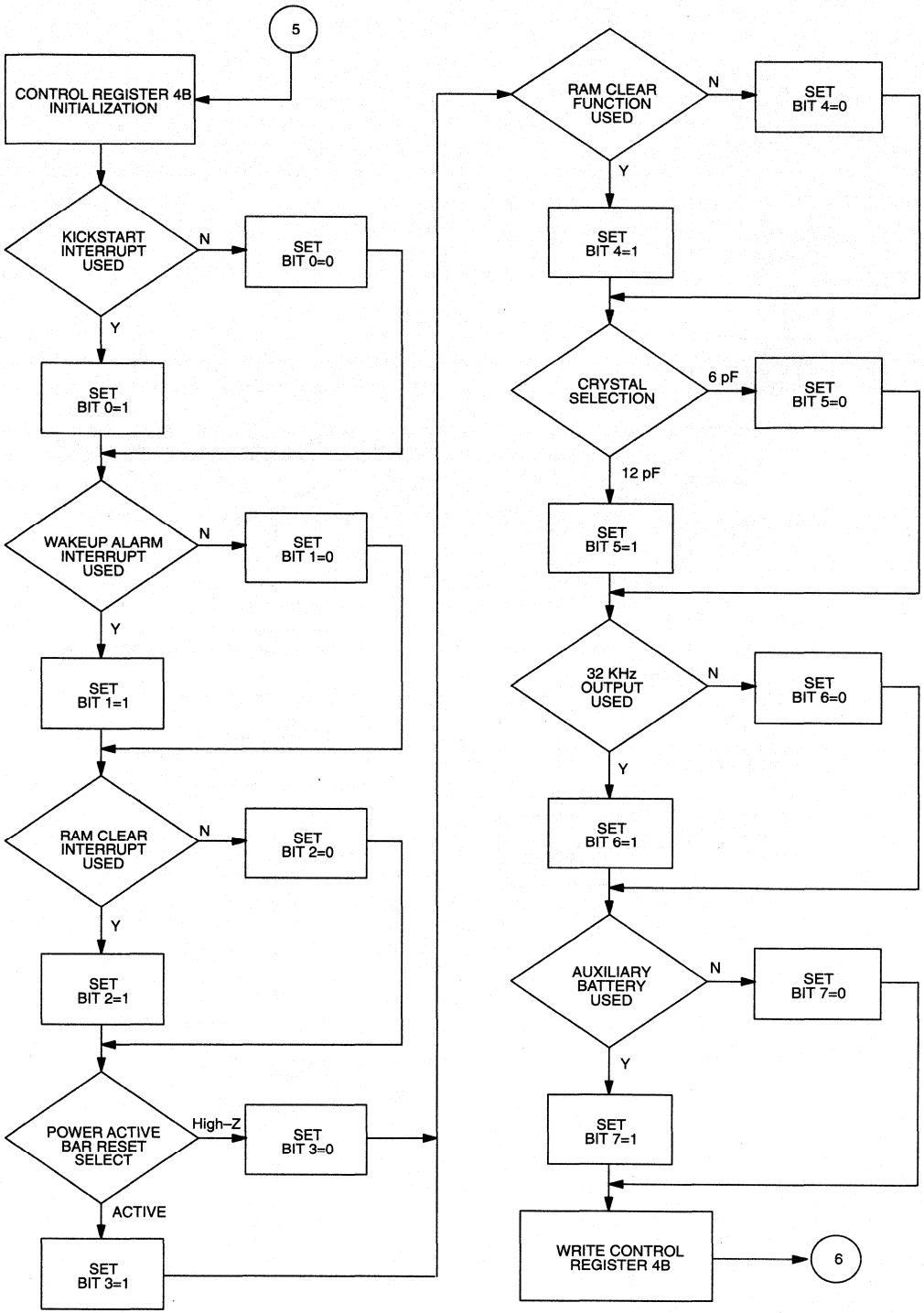
1. Burst Mode Enable (BME) is available only on the DS17285/7, DS17485/7, and DS17885/7 devices.
2. Cystal Selection (CS) is not available on the DS1585/7 or DS17A84/6 devices.
3. Power Active Bar Reset Select (PRS) is not available on the DS1585/7 or DS17A84/6 devices.

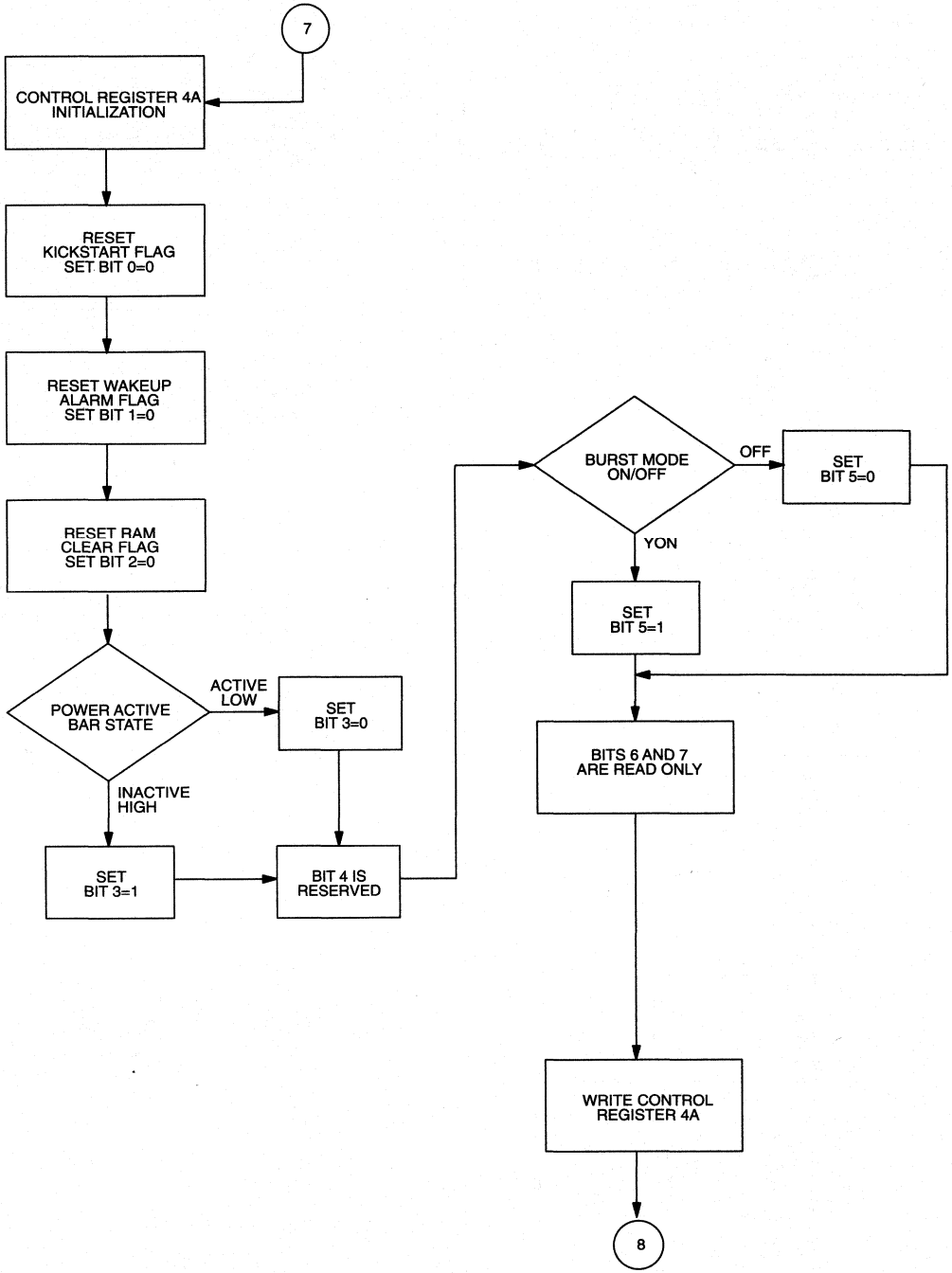
PC RTC INITIALIZATION PROCEDURE

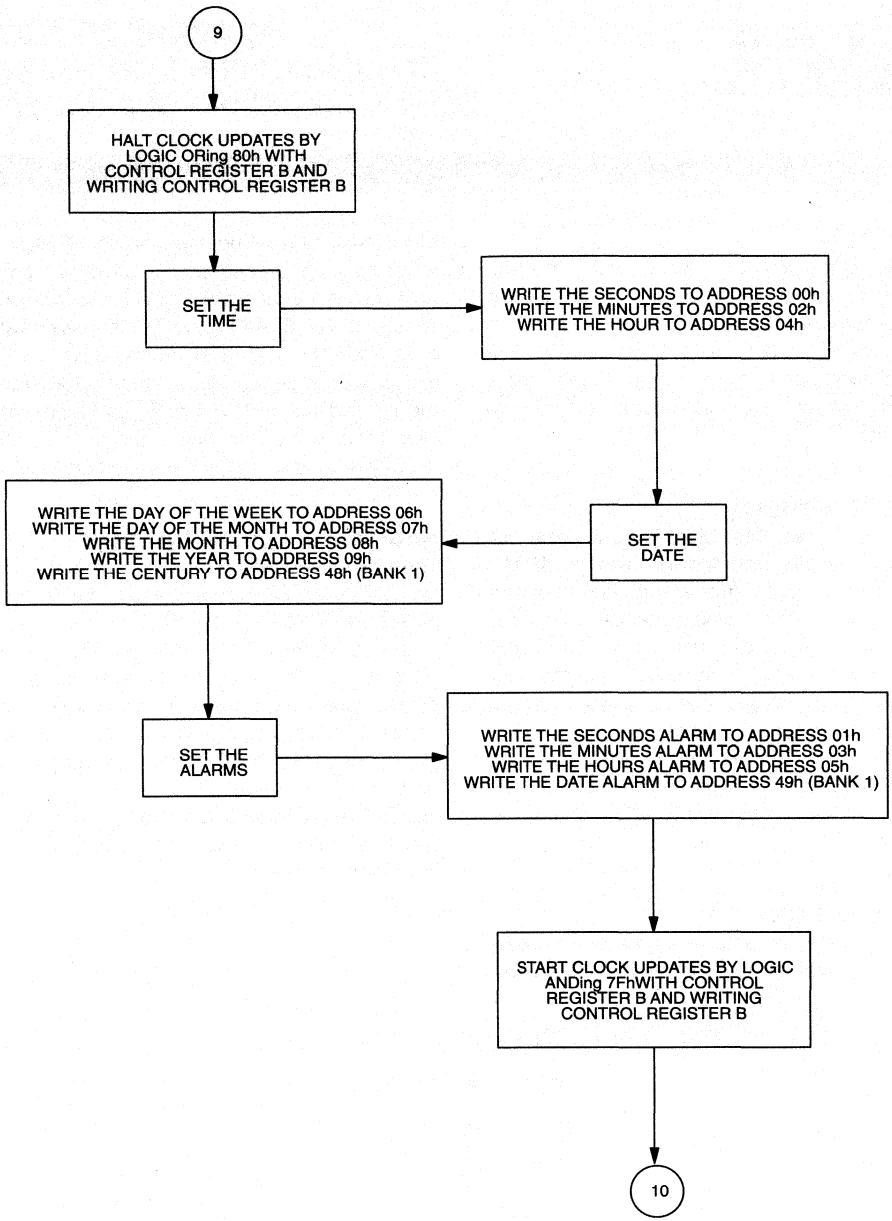



1
CONTROL REGISTER B INITIALIZATION
SET BIT 7=0
PERIODIC INTERRUPT USED
N
SET BIT 6=0
Y
SET BIT 6=1
ALARM INTERRUPT USED
N
SET BIT 5=0
Y
SET BIT 5=1
UPDATE-ENDED INTERRUPT USED
N
SET BIT 4=0
Y
SET BIT 4=1
SQARE WAVE USED
N
SET BIT 3=0
Y
SET BIT 3=1
DATA FORMAT BCD OR BINARY
BCD
SET BIT 2=0
BINARY
SET BIT 2=1
12-HOUR OR 24-HOUR
12
SET BIT 1=0
24
SET BIT 1=1
DAYLIGHT SAVINGS TIME USED
N
SET BIT 0=0
Y
SET BIT 0=1
WRITE CONTROL REGISTER B
2


3
CONTROL REGISTER A INITIALIZATION
SWITCH TO EXTENDED REGISTER BANK SET BIT 4=1
TURN THE OSCILLATOR ON
N
SET BIT 5=0
Y
SET BIT 5=1
ENABLE COUNTDOWN CHAIN
N
SET BIT 6=1
Y
SET BIT 6=0
SELECT THE PERIODIC INTERRUPT RATE AND/OR THE SQUARE WAVE OUTPUT FREQUENCY
NONE
SET BITS 3–0 TO 0000
256 Hz
SET BITS 3–0 TO 0001 OR 1000
128 Hz
SET BITS 3–0 TO 0010 OR 1001
8 KHz
SET BITS 3–0 TO 0011
4 KHz
SET BITS 3–0 TO 0100
2 KHz
SET BITS 3–0 TO 0101
1 KHz
SET BITS 3–0 TO 0110
512 Hz
SET BITS 3–0 TO 0111
64 Hz
SET BITS 3–0 TO 1010
32 Hz
SET BITS 3–0 TO 1011
16 Hz
SET BITS 3–0 TO 1100
8 Hz
SET BITS 3–0 TO 1101
4 Hz
SET BITS 3–0 TO 1110
2 Hz
SET BITS 3–0 TO 1111
WRITE CONTROL REGISTER A
4


5
CONTROL REGISTER 4B INITIALIZATION
KICKSTART INTERRUPT USED
N
SET BIT 0=0
Y
SET BIT 0=1
WAKEUP ALARM INTERRUPT USED
N
SET BIT 1=0
Y
SET BIT 1=1
RAM CLEAR INTERRUPT USED
N
SET BIT 2=0
Y
SET BIT 2=1
POWER ACTIVE BAR RESET SELECT
High–Z
SET BIT 3=0
ACTIVE
SET BIT 3=1
RAM CLEAR FUNCTION USED
N
SET BIT 4=0
Y
SET BIT 4=1
CRYSTAL SELECTION
6 pF
SET BIT 5=0
12 pF
SET BIT 5=1
32 KHz OUTPUT USED
N
SET BIT 6=0
Y
SET BIT 6=1
AUXILIARY BATTERY USED
N
SET BIT 7=0
Y
SET BIT 7=1
WRITE CONTROL REGISTER 4B
6


7
CONTROL REGISTER 4A INITIALIZATION
RESET KICKSTART FLAG SET BIT 0=0
RESET WAKEUP ALARM FLAG SET BIT 1=0
RESET RAM CLEAR FLAG SET BIT 2=0
POWER ACTIVE BAR STATE
ACTIVE LOW
SET BIT 3=0
INACTIVE HIGH
SET BIT 3=1
BIT 4 IS RESERVED
BURST MODE ON/OFF
OFF
SET BIT 5=0
YON
SET BIT 5=1
BITS 6 AND 7 ARE READ ONLY
WRITE CONTROL REGISTER 4A
8


9
HALT CLOCK UPDATES BY LOGIC ORing 80h WITH CONTROL REGISTER B AND WRITING CONTROL REGISTER B
SET THE TIME
WRITE THE SECONDS TO ADDRESS 00h
WRITE THE MINUTES TO ADDRESS 02h
WRITE THE HOUR TO ADDRESS 04h
SET THE DATE
WRITE THE DAY OF THE WEEK TO ADDRESS 06h
WRITE THE DAY OF THE MONTH TO ADDRESS 07h
WRITE THE MONTH TO ADDRESS 08h
WRITE THE YEAR TO ADDRESS 09h
WRITE THE CENTURY TO ADDRESS 48h (BANK 1)
SET THE ALARMS
WRITE THE SECONDS ALARM TO ADDRESS 01h
WRITE THE MINUTES ALARM TO ADDRESS 03h
WRITE THE HOURS ALARM TO ADDRESS 05h
WRITE THE DATE ALARM TO ADDRESS 49h (BANK 1)
START CLOCK UPDATES BY LOGIC ANDing 7FhWITH CONTROL REGISTER B AND WRITING CONTROL REGISTER B
10

DALLAS SEMICONDUCTOR

Application Note 95
Interfacing the DS1307 with a 8051-Compatible Microcontroller

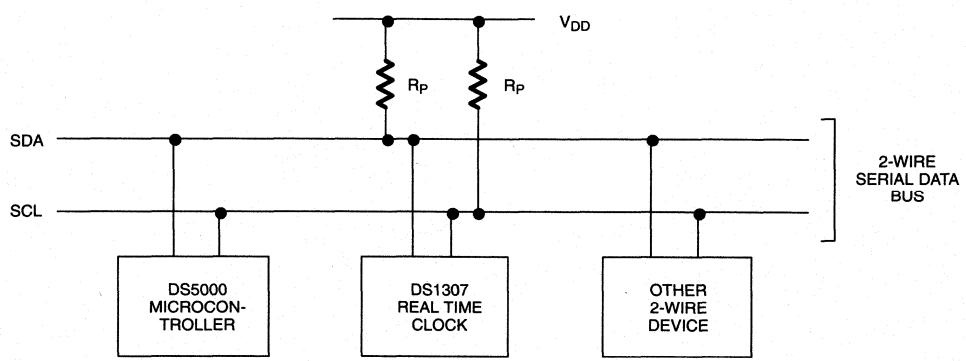
INTRODUCTION
The DS1307 Serial Real Time Clock, which incorporates a 2–wire serial interface, can be controlled using an 8051 compatible DS5000 microcontroller. The DS1307 is connected directly to two of the I/O ports on a DS5000 microcontroller and the 2–wire handshaking is handled by low level drivers, which are discussed in this application note.

DS1307 DESCRIPTION
The DS1307 Serial Real Time Clock is a low-power, full BCD clock/calendar plus 56 bytes of nonvolatile SRAM. Address and data are transferred serially via the 2–wire bi-directional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24–hour or 12–hour format with AM/PM indicator. The DS1307 has a built–in power sense circuit which detects power failures and automatically switches to the battery supply.

DS1307 OPERATION
The DS1307 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by a register address. Subsequent registers can be accessed sequentially until a STOP condition is executed. The START and STOP conditions are generated using the low level drives, SEND_START and SEND_STOP found in the attached DS5000 code. Also the subroutines SEND_BYTE and READ_BYTE provide the 2–wire handshaking required for writing and reading 8–bit words to and from the DS1307.

HARDWARE CONFIGURATION
The system is configured as shown in Figure 1. The DS1307 has the 2–wire bus connected to two I/O port pins of the DS5000: SCL – P1.0, SDA – P1.1. The V_{DD} voltage is 5V, R_P = 5 KΩ and the DS5000 is using a 12 MHz crystal. The other peripheral device could be any other device that recognizes the 2–wire protocol, such as the DS1621 Digital Thermometer and Thermostat. The interface with the D5000 was accomplished using the DS5000T Kit hardware and software. This development kit allows the PC to be used as a dumb terminal using the DS5000's serial ports to communicate with the keyboard and monitor.

TYPICAL 2–WIRE BUS CONFIGURATION Figure 1



The following bus protocol has been defined (see Figure 2).

- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Start data transfer: A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

Stop data transfer: A change in the state of the data line from low to high, while the clock line is high defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte–wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

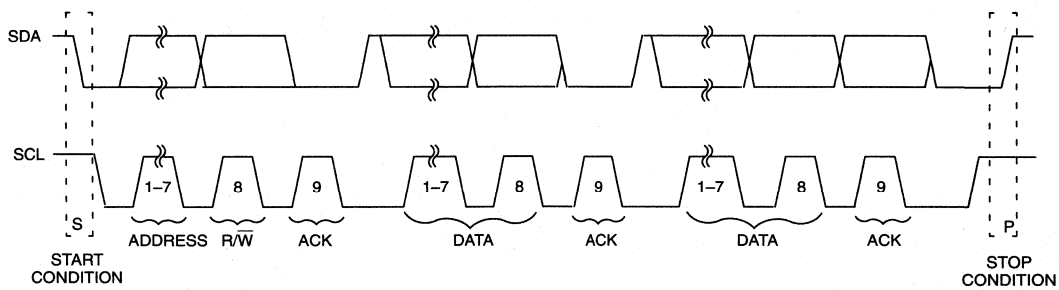
A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

Figure 2 details how data transfer is accomplished on the 2–wire bus. Depending on the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

6. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

7. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge is returned.

DATA TRANSFER ON 2–WIRE SERIAL BUS Figure 2



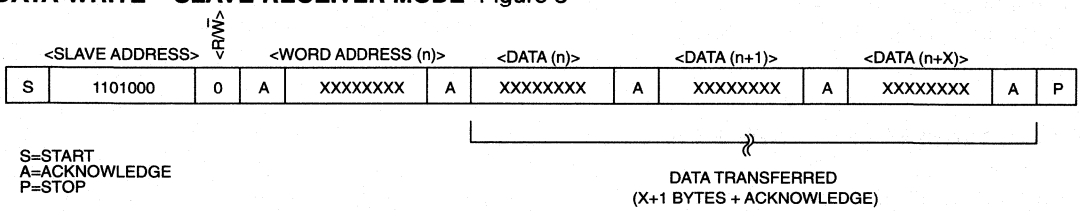
The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transferred with the most significant bit (MSB) first.

The DS1307 may operate in the following two modes:

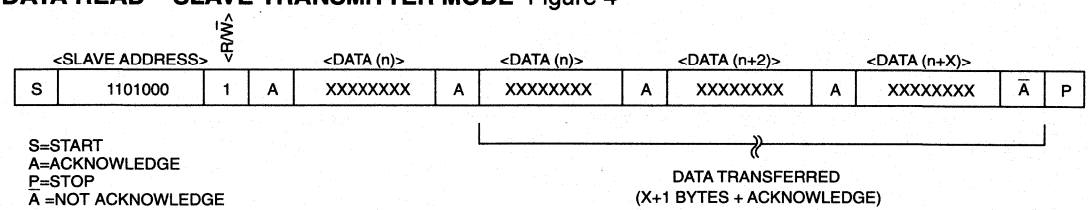
1. **Slave receiver mode (DS1307 write mode):** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 3). The address byte is the first byte received after the start condition is generated by the master. The address byte contains the 7-bit DS1307 address, which is 1101000, followed by the direction bit ($R/\overline{W}$) which for a write is a 0. After receiving and decoding the address byte, the DS1307 outputs an acknowledge on the SDA line. After the DS1307 acknowledges the slave address + write bit, the master transmits a register address to the DS1307. This will set the register pointer on the DS1307. The master will then begin transmitting each byte of data with the DS1307 acknowledging each byte received. The master will generate a stop condition to terminate the data write.

2. **Slave transmitter mode (DS1307 read mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1307 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (See Figure 4). The address byte is the first byte received after the start condition is generated by the master. The address byte contains the 7 bit DS1307 address, which is 1101000, followed by the direction bit ($R/\overline{W}$) which for a read is a 1. After receiving and decoding the address byte, the DS1307 inputs an acknowledge on the SDA line. The DS1307 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The DS1307 must be sent a Not–Acknowledge bit by the master to terminate a read.

DATA WRITE – SLAVE RECEIVER MODE Figure 3



DATA READ – SLAVE TRANSMITTER MODE Figure 4



SOFTWARE OPERATION

DS5000 INTERFACE

The software presented in Appendix 1 is written to interface the DS5000 with the DS1307 over the 2–wire interface. The DS5000 was programmed using Dallas Semiconductor's DS5000T Evaluation Kit, which allows a PC to be used as a dumb terminal. The KIT5K software environment supplied with the DS5000T Evaluation Kit provides a high–level interface for loading application software to the DS5000 or for setting its configuration parameters via the Program command. The KIT5K software includes a dumb terminal emulator to allow users to run application software in the DS5000 which communicates with the user via a PC COM port.

DS1307 SOURCE CODE

The first section of the code found in the Appendix is used to configure the DS5000 for serial communication with the PC. Also at the beginning of the code is the MASTER_CONTROLLER subroutine which is used to control the demonstration software.

The subroutines that immediately follow the MASTER_CONTROLLER subroutine are the low level drivers for controlling the 2–wire interface. They are not specific to the DS1307 but can be used with any 2–wire compatible Slave–only device. These subroutines are:

SEND_START
: This subroutine is used to generate the Start condition on the 2–wire bus.

SEND_STOP
: This subroutine is used to generate the Stop condition on the 2–wire bus.

SEND_BYTE
: This subroutine sends an 8–bit word, MSB first, over the 2–wire bus with a 9th clock pulse for the Acknowledge pulse.

READ_BYTE
: This subroutine reads an 8–bit word over the 2–wire bus. It checks for the LASTREAD flag to be cleared indicating when the last read from the slave device is to occur. If it is not the last read, the DS5000 sends an Acknowledge pulse on the 9th clock and if it is the last read from the slave device, the DS5000 sends a Not–Acknowledge.

SCL_HIGH
: This subroutine transitions the SCL line low–to–high and ensures the SCL line is high before continuing.

DELAY and DELAY_4
: These two subroutines have been included to ensure that the 2–wire bus timing is maintained.

The rest of the code included in the appendix is specifically designed to demonstrate the functions of the DS1307. The functions that are demonstrated are:

Setting Time
: The time is read in from the keyboard and stored in the DS5000 scratchpad memory. It is then transferred, over the 2–wire interface, to the DS1307.

Set RAM
: A single hex byte is read in from the keyboard and written to the entire user RAM of the DS1307.

Read Date/Time
: The date and time are read, over the 2–wire bus, and stored in the DS5000 scratchpad memory. It is then written to the screen. This continues until a key is pressed on the keyboard.

Read RAM
: The entire user RAM of the DS1307 is read into the DS5000 scratchpad memory and then written to the PC monitor.

OSC On/ OSC Off
: The DS1307 clock oscillator can be turned on or off.

SQW/OUT On/ SQW/OUT Off
: The SQW/OUT can be turned on or off. It will toggle at 1 Hz.

AC ELECTRICAL CHARACTERISTICS Table 1

PARAMETER	SYMBOL	ACTUAL	UNITS
SCL Clock Frequency	f_{SCL}	59	KHz
Bus Free Time Between a STOP and START Condition	t_{BUF}	5.7	µs
Hold Time (repeated) START Condition	$t_{HD:STA}$	6.2	µs
LOW Period of SCL Clock	t_{LOW}	10.5	µs
HIGH Period of SCL Clock	t_{HIGH}	6.5	µs
Set-up Time for a Repeated START Condition	$t_{SU:STA}$	5.3	µs
Data Hold Time	$t_{HD:DAT}$	5.5	µs
Data Set-up Time	$t_{SU:DAT}$	3.1	µs
Rise Time of Both SDA and SCL Signals	t_R		ns
Fall Time of Both SDA and SCL Signals	t_F		ns
Set-up Time for STOP Condition	$t_{SU:STO}$	5.4	µs

CONCLUSION

It has been shown that it is very straight forward to interface the DS1307 or any other 2-wire slave device to an 8051-compatible microcontroller. The only concern must be that the 2-wire timing specification is not violated by the low level drivers on the microcontroller. The delay subroutines have been inserted into the code for this purpose. The values in Table 1 are the actual timing parameters observed in the hardware setup used to develop this application note.

APPENDIX

DS1307.ASM

```
;       Program DS1307.ASM
;
;       This program responds to commands received over the serial
;       port to set the date/time as well as RAM data on the DS1307
;       using a DS5000 as a controller
;
$MOD51
CR              EQU             0DH
LF              EQU             0AH
MCON            EQU             0C6H
TA              EQU             0C7H
SCL             BIT             P1.0
SDA             BIT             P1.1
TRIG            BIT             P1.2
DS1307W         EQU             0D0H
DS1307R         EQU             0D1H
FLAGS           DATA            20H
LASTREAD        BIT             FLAGS.0
_12_24          BIT             FLAGS.1
PM_AM           BIT             FLAGS.2
OSC             BIT             FLAGS.3
SQW             BIT             FLAGS.4
ACK             BIT             FLAGS.5
BUS_FAULT       BIT             FLAGS.6
_2W_BUSY        BIT             FLAGS.7
BITCOUNT        DATA            21H
BYTECOUNT       DATA            22H
BYTE            DATA            23H
                CSEG            AT              0
                AJMP            START
;
                CSEG            AT              30H
;*************************************************************
;***             RESET GOES HERE TO START PROGRAM          ****
;*************************************************************
START:
                MOV             TA,             #0AAH   ;  Timed
                MOV             TA,             #55H    ;  access.
                MOV             PCON,           #0      ;  Reset watchdog timer.
                MOV             MCON,           #0F8H   ;  Turn off CE2 for memory
                                                        ;  access.
                MOV             SP,             #70H    ;  Position stack above
                                                        ;  buffer.
                MOV             IE,             #0
                MOV             TMOD,           #20H    ;  Initialize the
                MOV             TH1,            #0FAH   ;  serial port
                MOV             TL1,            #0FAH   ;  for 9600
                ORL             PCON,           #80H    ;  baud.
```

```
                MOV             SCON,           #52H
                MOV             TCON,           #40H

                MOV             R0,             #0
                MOV             R1,             #0
                DJNZ            R0,             $
                DJNZ            R1,             $-2
                SETB            SDA                     ;  ENSURE SDA HIGH
                LCALL           SCL_HIGH                ;  ENSURE SCL HIGH
                CLR                             ACK     ;  CLEAR STATUS FLAGS
                CLR                             BUS_FAULT
                CLR                             _2W_BUSY
;-------------------------------------------------------------------------
;       THIS IS THE MASTER CONTROLLER LOOP
;-------------------------------------------------------------------------
MASTER_CONTROLLER:
        MOV     BYTECOUNT,#20H
FORM_FEED:
        MOV     A,#LF                                   ;  CLEAR SCREEN FOR MAIN MENU
        LCALL   WRITE_DATA
        DJNZ    BYTECOUNT,FORM_FEED

        MOV     DPTR,    #TEXT0                         ;  PUT MAIN MENU ON SCREEN
        LCALL   WRITE_TEXT
        MOV     DPTR,    #TEXT3
        LCALL   WRITE_TEXT
        LCALL   READ_DATA
        CLR     ACC.5                                   ;  CONVERT ACC TO UPPER CASE

        CJNE    A,#'A',NOTA                             ;  CALL SET CLOCK FUNCTION
        LCALL   SET_CLOCK
NOTA:
        CJNE    A,#'B',NOTB                             ;  CALL SET RAM FUNCTION AND
        LCALL   SET_RAM                                 ;  CALL READ RAM FUNCTION
        LCALL   READ_RAM
NOTB:
        CJNE    A,#'C',NOTC                             ;  CALL READ CLOCK FUNCTION
        LCALL   READ_CLOCK
NOTC:
        CJNE    A,#'D',NOTD                             ;  CALL READ RAM FUNCTION
        LCALL   READ_RAM
NOTD:
        CJNE    A,#'E',NOTE                             ;  CALL OSC CONTROL FUNCTION
        CLR     OSC                                     ;  CLR OSC FLAG - ON
        LCALL   OSC_CONTROL
NOTE:
        CJNE    A,#'F',NOTF                             ;  CALL OSC CONTROL FUNCTION
        SETB    OSC                                     ;  SET OSC FLAG - OFF
        LCALL   OSC_CONTROL
NOTF:
        CJNE    A,#'G',NOTG                             ;  CALL SWQ CONTROL FUNCTION
```

```
        CLR     SQW                                     ;  CLR SQW FLAG - ON
        LCALL   SQW_CONTROL
NOTG:
        CJNE    A,#'H',NOTH                             ;  CALL SWQ CONTROL FUNCTION
        SETB    SQW                                     ;  SET SQW FLAG - OFF
        LCALL   SQW_CONTROL
NOTH:
        JMP     MASTER_CONTROLLER                       ;  LOOP UNTIL DONE
;-------------------------------------------------------------------------
;       THIS SUB SENDS THE START CONDITION
;-------------------------------------------------------------------------
SEND_START:                                             ;
        SETB    _2W_BUSY                                ;  INDICATE THAT 2WIRE
                                                        :  OPERATION IN PROGRESS
        CLR     ACK                                     ;  CLEAR STATUS FLAGS
        CLR     BUS_FAULT
        JNB     SCL,FAULT                               ;  CHECK FOR BUS CLEAR
        JNB     SDA,FAULT
                                                        ;  BEGIN START CONDITION
        SETB    SDA                                     ;
        LCALL   SCL_HIGH                                ;  SDA
        CLR     SDA                                     ;
        LCALL   DELAY                                   ;  SCL ^START CONDITION
        CLR     SCL                                     ;
                RET
FAULT:
        SETB    BUS_FAULT                               ;  SET FAULT STATUS
        RET                                             ;  AND RETURN
;-------------------------------------------------------------------------
;       THIS SUB SENDS THE STOP CONDITION
;-------------------------------------------------------------------------
SEND_STOP:                                              ;
        CLR     SDA                                     ; SDA
        LCALL   SCL_HIGH                                ;
        SETB    SDA                                     ; SCL ^STOP CONDITION
        CLR     2W_BUSY                                 ;
        RET                                             ;
;-------------------------------------------------------------------------
;       THIS SUB SENDS ONE BYTE OF DATA TO THE DS1307
;-------------------------------------------------------------------------
SEND_BYTE:
        MOV     BITCOUNT,#08H                           ;  SET COUNTER FOR 8 BITS
SB_LOOP:
        JNB     ACC.7,NOTONE                            ;  CHECK TO SEE IF BIT 7 OF
                                                        ;  ACC IS A 1
        SETB    SDA                                     ;  SET SDA HIGH (1)
        JMP     ONE
NOTONE:
        CLR     SDA                                     ;  CLR SDA LOW (0)
ONE:
        LCALL   SCL_HIGH                                ;  TRANSITION SCL LOW-TO-HIGH
```

```
        RL      A                                       ;  ROTATE ACC LEFT ONE BIT
        CLR     SCL                                     ;  TRANSITION SCL HIGH-TO-LOW
        DJNZ    BITCOUNT,SB_LOOP                        ;  LOOP FOR 8 BITS

        SETB    SDA                                     ;  SET SDA HIGH FOR
                                                        ;  ACKNOWLEDGE PULSE
        LCALL   SCL_HIGH                                ;  TRASITION SCL LOW-TO-HIGH
        CLR     ACK                                     ;  CLEAR ACKNOWLEDGE FLAG
        JNB     SDA,SB_EX                               ;  CHECK FOR ACK OR NOT ACK
        SETB    ACK                                     ;  SET ACKNOWLEDGE FLAG FOR
                                                        ;  NOT ACK
SB_EX:
        LCALL   DELAY                                   ;  DELAY FOR AN OPERATION
        CLR     SCL                                     ;  TRANSITION SCL HIGH-TO-LOW
        LCALL   DELAY                                   ;  DELAY FOR AN OPERATION
        RET
;-------------------------------------------------------------------------
;       THIS SUB READS ONE BYTE OF DATA FROM THE DS1307
;-------------------------------------------------------------------------
READ_BYTE:
        MOV     BITCOUNT,#008H                          ;  SET COUNTER FOR 8 BITS OF
                                                        :  DATA
        MOV     A,#00H                                  ;
        SETB    SDA                                     ;  SET SDA HIGH TO ENSURE LINE
                                                        ;  FREE
SB_LOOP2:
        LCALL   SCL_HIGH                                ;  TRANSITION SCL LOW-TO-HIGH
        MOV     C,SDA                                   ;  MOVE DATA BIT INTO CARRY
                                                        ;  BIT
        RLC     A                                       ;  ROTATE CARRY BIT INTO ACC.0
        CLR     SCL                                     ;  TRANSITION SCL HIGH-TO-LOW
        DJNZ    BITCOUNT,SB_LOOP2                       ;  LOOP FOR 8 BITS

        JB      LASTREAD,ACK                            ;  CHECK TO SEE IF THIS IS THE
                                                        :  LAST READ
        CLR     SDA                                     ;  IF NOT LAST READ SEND
                                                        :  ACKNOWLEDGE BIT
ACK:
        LCALL   SCL_HIGH                                ;  PULSE SCL TO TRANSIMIT
                                                        ;  ACKNOWLEDGE
        CLR     SCL                                     ;  OR NOT ACKNOWLEDGE BIT
        RET
;-------------------------------------------------------------------------
;       THIS SUB SETS THE CLOCK LINE HIGH
;-------------------------------------------------------------------------
SCL_HIGH:
        SETB    SCL                                     ;  SET SCL HIGH
        JNB     SCL,$                                   ;  LOOP UNTIL STRONG 1 ON SCL
        RET
```

```
;-------------------------------------------------------------------------
;       THIS SUB DELAY THE BUS
;-------------------------------------------------------------------------
DELAY:
        NOP                                             ;  DELAY FOR BUS TIMING
        RET
;-------------------------------------------------------------------------
;       THIS SUB DELAYS 4 CYCLES
;-------------------------------------------------------------------------
DELAY_4:
        NOP                                             ;  DELAY FOR BUS TIMING
        NOP
        NOP
        NOP
        RET
;-------------------------------------------------------------------------
;       THIS SUB SETS THE CLOCK
;-------------------------------------------------------------------------
SET_CLOCK:
        MOV     R1,#2EH                                 ;  SET R1 TO SCRATCHPAD MEMORY
                                                        ;  FOR DATE/TIME
        MOV     DPTR,   #YEAR                           ;  GET THE DATE/TIME
                                                        ;  INFORMATION FROM THE
        LCALL   WRITE_TEXT                              ;  USER.  WRITE THE DATE/TIME
                                                        ;  TO SCRATCHPAD
        LCALL   READ_BCD                                ;  MEMORY
        MOV     @R1,A
        DEC     R1
        MOV     DPTR,   #MONTH
        LCALL   WRITE_TEXT
        LCALL   READ_BCD
        MOV     @R1,A
        DEC     R1
        MOV     DPTR,   #DAY
        LCALL   WRITE_TEXT
        LCALL   READ_BCD
        MOV     @R1,A
        DEC     R1
        MOV     DPTR,   #DAYW
        LCALL   WRITE_TEXT
        LCALL   READ_BCD
        ANL     A,      #7
        MOV     @R1,A
        DEC     R1
        MOV     DPTR,   #HOUR
        LCALL   WRITE_TEXT
        LCALL   READ_BCD
        MOV     @R1,A
        DEC     R1
        MOV     DPTR,   #MINUTE
        LCALL   WRITE_TEXT
```

```
        LCALL   READ_BCD
        MOV     @R1,A
        DEC     R1
        MOV     DPTR,   #SECOND
        LCALL   WRITE_TEXT
        LCALL   READ_BCD
        MOV     @R1,A
        MOV     R1,#28H                         ;  POINT TO BEGINNING OF CLOCK
                                                ;  DATA IN SCRATCHPAD MEMORY
        LCALL   SEND_START                      ;  SEND 2WIRE START CONDITION
        MOV     A,#DS1307W                      ;  SEND DS1307 WRITE COMMAND
        LCALL   SEND_BYTE
        MOV     A,#00H                          ;  SET DATA POINTER TO
                                                ;  REGISTER 00H ON
        LCALL   SEND_BYTE                       ;  THE DS1307
SEND_LOOP:
        MOV     A,@R1                           ;  MOVE THE FIRST BYTE OF DATA
                                                ;  TO ACC
        LCALL   SEND_BYTE                       ;  SEND DATA ON 2WIRE BUT
        INC     R1
        CJNE    R1,#2FH,SEND_LOOP               ;  LOOP UNTIL CLOCK DATA SENT
                                                ;  TO DS1307
        LCALL   SEND_STOP                       ;  SEND 2WIRE STOP CONDITION
        RET
;-------------------------------------------------------------------------
;       THIS SUB SETS THE DS1307 USER RAM TO THE VALUE IN 'BYTE'
;-------------------------------------------------------------------------
SET_RAM:
        MOV     R1,#08H                         ;  POINTER TO BEGINNING OF
                                                ;  DS1307 USER RAM
        MOV     DPTR,   #TEXT5                  ;  MESSAGE TO ENTER DATA BYTE
        LCALL   WRITE_TEXT                      ;
        LCALL   READ_BCD                        ;  READ BYTE FROM KEYBOARD
        MOV     BYTE,A                          ;  AND STORE IN 'BYTE'
        LCALL   SEND_START                      ;  SEND 2WIRE START CONDITION
        MOV     A,#DS1307W                      ;  LOAD DS1307 WRITE COMMAND
        LCALL   SEND_BYTE                       ;  SEND WRITE COMMAND
        MOV     A,#08H                          ;  SET DS1307 DATA POINTER TO
                                                ;  BEGINNING
        LCALL   SEND_BYTE                       ; OF USER RAM - 08H
SEND_LOOP2:
        MOV     A,BYTE                          ;  WRITE BYTE TO ENTIRE RAM
                                                ;  SPACE
        LCALL   SEND_BYTE                       ;  WHICH IS 08H TO 37H
        INC     R1
        CJNE    R1,#040H,SEND_LOOP2             ;  LOOP UNTIL RAM FILLED
        LCALL   SEND_STOP                       ;  SEND 2WIRE STOP CONTION
        RET
```

```
;-------------------------------------------------------------------------
;       THIS SUB READS THE DS1307 RAM AND WRITES IT TO THE SCRATCH PAD MEMORY
;-------------------------------------------------------------------------
READ_RAM:
        MOV     DPTR,#TEXT4                     ;  SEND KEY PRESS MSG
        LCALL   WRITE_TEXT
        MOV     R1,#30H                         ;  START OF RAM REGS IN
                                                ;  SCRATCH PAD
        MOV     BYTECOUNT,#00H                  ;  COUNTER, UP TO 56 BYTES FOR
                                                ;  CLOCK
        CLR     LASTREAD                        ;  FLAG TO CHECK FOR LAST READ
        LCALL   SEND_START                      ;  SEND 2WIRE START CONDITION
        MOV     A,#DS1307W                      ;  SEND DS1307 WRITE COMMAND
        LCALL   SEND_BYTE
        MOV     A,#08H                          ;  SET POINTER TO REG 08H ON
                                                :  DS1307
        LCALL   SEND_BYTE
        LCALL   SEND_START                      ;  SEND REPEATED START
                                                ;  CONDITION
        MOV     A,#DS1307R                      ;  SEND DS1307 READ COMMAND
        LCALL   SEND_BYTE
READ_LOOP2:
        MOV     A,BYTECOUNT                     ;  CHECK TO SEE OF DOING LAST
                                                ;  READ
        CJNE    A,#3EH,NOT_LAST2
        SETB    LASTREAD                        ;  IF LAST READ SET LASTREAD
                                                ;  FLAG
NOT_LAST2:
        LCALL   READ_BYTE                       ;  READ A BYTE OF DATA
        MOV     @R1,A                           ;  MOVE DATA INTO SCRATCHPAD
                                                ;  MEMORY
        INC     R1                              ;  INC POINTERS
        INC     BYTECOUNT
        MOV     A,BYTECOUNT
        CJNE    A,#3FH,READ_LOOP2               ;  LOOP FOR ENTIRE DS1307 RAM

        LCALL   SEND_STOP                       ;  SEND 2WIRE STOP CONDITION
        LCALL   DISP_RAM                        ;  DISPLAY DATA IN SCRATCHPAD
                                                ;  MEMORY
        JNB     RI,$                            ;  WAIT UNTIL A KEY IS PRESSED
        CLR     RI
RET
;-------------------------------------------------------------------------
;       THIS SUB DISPLAYS THE RAM DATA SAVED IN SCRATCHPAD MEMORY
;-------------------------------------------------------------------------
DISP_RAM:
        MOV     R1,#30H                         ;  START OF RAM IN SCRATCHPAD
                                                ;  MEMORY
        MOV     BITCOUNT,#00H
        MOV     DPTR,#TEXT6                     ;  ASK FOR DATA BYTE TO STORE
                                                ;  IN RAM
```

```
        LCALL   WRITE_TEXT
        LCALL   DISP_LOC                        ;  DISPLAY VALUE OF CURRENT
                                                ;  RAM LOCATION
DIS_LOOP:
        MOV     A,@R1                           ;  DISPLAY RAM DATA SAVED IN
                                                ;  SCRATCHPAD
        LCALL   WRITE_BCD                       ;  CONVERT TO BCD FORMAT AND
                                                ;  DISPLAY
        INC     R1
        INC     BITCOUNT
        MOV     A,#20H                          ;  SPACE BETWEEN DATA BYTES
        LCALL   WRITE_DATA
MOV     A,BITCOUNT
        CJNE    A,#08H,NEXTLINE                 ;  LINE FEED AFTER 8 BYTES OF
                                                ;  DATA
        MOV     BITCOUNT,#00H
        MOV     DPTR,#TEXT3                     ;  'CR,LF'
        LCALL   WRITE_TEXT
        LCALL   DISP_LOC                        ;  DISPLAY VALUE OF CURRENT
                                                ;  RAM LOCATION
NEXTLINE:
        CJNE    R1,#68H,DIS_LOOP                ;  DISPLAY DATA FOR 56 BYTES
                                                ;  OF RAM
RET
;-------------------------------------------------------------------------
;       THIS SUB WRITES THE RAM LOCATION OF THE DATA
;-------------------------------------------------------------------------
DISP_LOC:
        MOV     A,R1                            ;  DISPLAY THE HEX VALUE FOR
                                                ;  THE DATA
        ADD     A,#-30H                         ;  IN THE DS1307 RAM SPACE
        LCALL   WRITE_BCD                       ;  CONVERTS SCRATCHPAD ADDRESS
        MOV     A,#20H                          ;  INTO DS1307 RAM ADDRESS
        LCALL   WRITE_DATA
        MOV     A,#20H
        LCALL   WRITE_DATA
        MOV     A,#20H
        LCALL   WRITE_DATA
        RET
;-------------------------------------------------------------------------
;       THIS SUB READS THE CLOCK AND WRITES IT TO THE SCRATCH PAD MEMORY
;-------------------------------------------------------------------------
READ_CLOCK:
        MOV     DPTR,#TEXT4                     ;  KEY PRESS MSG
        LCALL   WRITE_TEXT
READ_AGAIN:
        MOV     R1,#28H                         ;  START OF CLOCK REG IN
                                                ;  SCRATCHPAD
        MOV     BYTECOUNT,#00H                  ;  COUNTER UP TO 8 BYTES FOR
                                                ;  CLOCK
        CLR     LASTREAD                        ;  FLAG TO CHECK FOR LAST READ
```

```
        LCALL   SEND_START                      ;  SEND START CONDITION
        MOV     A,#DS1307W                      ;  SET POINTER TO REG 00H ON
                                                ;  DS1307
        LCALL   SEND_BYTE
        MOV     A,#00H
        LCALL   SEND_BYTE
        LCALL   SEND_START                      ;  SEND REPEATED START
                                                ;  CONDITION
        MOV     A,#DS1307R                      ;  SEND READ COMMAND TO DS1307
        LCALL   SEND_BYTE
READ_LOOP:
        MOV     A,BYTECOUNT                     ;  CHECK TO SEE OF DOING LAST
                                                ;  READ
        CJNE    A,#07H,NOT_LAST
        SETB    LASTREAD                        ;  SET LASTREAD FLAG
NOT_LAST:
        LCALL   READ_BYTE                       ;  READ A BYTE OF DATA
        MOV     @R1,A                           ;  MOVE DATA IN SCRATCHPAD
                                                ;  MEMORY
        MOV     A,BYTECOUNT                     ;  CHECK TO SEE IF READING
                                                ;  SECONDS REG
        CJNE    A,#00H,NOT_FIRST
        CLR     OSC                             ;  CLR OSC FLAG
        MOV     A,@R1                           ;  MOVE SECONDS REG INTO ACC
        JNB     ACC.7,NO_OSC                    ;  JUMP IF BIT 7 OF IS A 0
        SETB    OSC                             ;  SET OSC FLAG, BIT 7 IS A 1
        CLR     ACC.7                           ;  CLEAR BIT 7 FOR DISPLAY
                                                ;  PURPOSES
        MOV     @R1,A                           ; MOVE DATA BACK TO SCRATCHPAD
NO_OSC:
NOT_FIRST:
        INC     R1                              ;  INC COUNTERS
        INC     BYTECOUNT
        MOV     A,BYTECOUNT
        CJNE    A,#08H,READ_LOOP                ;  LOOP FOR ENTIRE CLOCK
                                                ;  REGISTERS
        LCALL   SEND_STOP                       ;  SEND 2WIRE STOP CONDITION
        LCALL   DISP_CLOCK                      ;  DISPLAY DATE/TIME FROM
                                                ;  SCRATCHPAD
        JNB     RI,READ_AGAIN                   ;  READ AND DISPLAY UNTIL A
                                                ;  KEY IS PRESSED
        CLR     RI
RET
;-------------------------------------------------------------------------
;       THIS SUB DISPLAYS THE DATE AND TIME SAVED IN SCRATCHPAD MEMORY
;-------------------------------------------------------------------------
DISP_CLOCK:
        MOV     DPTR,#TEXT1                     ;  DATE:
        LCALL   WRITE_TEXT
        MOV     R1,#2DH                         ;  MONTH
        MOV     A,@R1
```

```
        LCALL   WRITE_BCD
        MOV     A,#'/'
        LCALL   WRITE_DATA
        MOV     R1,#2CH                         ;  DATE
        MOV     A,@R1
        LCALL   WRITE_BCD
        MOV     A,#'/'
        LCALL   WRITE_DATA
        MOV     R1,#2EH                         ;  YEAR
        MOV     A,@R1
        LCALL   WRITE_BCD
        MOV     A,#09H                          ;  TAB
        LCALL   WRITE_DATA
        MOV     DPTR,#TEXT2                     ;  TIME:
        LCALL   WRITE_TEXT
        MOV     R1,#2AH                         ;  HOURS
        MOV     A,@R1
        LCALL   WRITE_BCD
        MOV     A,#3AH                          ;  COLON
        LCALL   WRITE_DATA
        MOV     R1,#29H                         ;  MINUTES
        MOV     A,@R1
        LCALL   WRITE_BCD
        MOV     A,#3AH                          ;  COLON
        LCALL   WRITE_DATA
        MOV     R1,#28H                         ;  SECONDS
        MOV     A,@R1
        LCALL   WRITE_BCD
        RET
;-------------------------------------------------------------------------
;       THIS SUB SETS THE OSCILLATOR ACCORDING TO THE OSC BIT
;-------------------------------------------------------------------------
OSC_CONTROL:
        LCALL   SEND_START                      ;  SEND START CONDITION
        MOV     A,#DS1307W                      ;  SET POINTER TO REG 00H ON
                                                ;  DS1307
        LCALL   SEND_BYTE
        MOV     A,#00H
        LCALL   SEND_BYTE
        SETB    LASTREAD                        ;  SET LAST READ FOR SINGLE
                                                ;  READ
        LCALL   SEND_START                      ;  SEND REPEATED START
                                                ;  CONDITION
        MOV     A,#DS1307R                      ;  SEND READ COMMAND TO DS1307
        LCALL   SEND_BYTE
        LCALL   READ_BYTE                       ;  READ SECONDS REGISTER
        CLR     ACC.7                           ;  TURN OSC ON
        JNB     OSC,OSC_ON
        SETB     ACC.7                          ;  TURN OSC OFF IF OSC BIT IS
                                                ;  SET IN
OSC_ON:                                         ;  SECONDS REGISTER
```

```
        PUSH    ACC                             ;  SAVE SECONDS DATA ON STACK
        LCALL   SEND_START                      ;  SEND START CONDITION
        MOV     A,#DS1307W                      ;  SET POINTER TO REG 00H ON
                                                ;  DS1307
        LCALL   SEND_BYTE
        MOV     A,#00H
        LCALL   SEND_BYTE
        POP     ACC                             ;  SEND SECONDS REGISTER TO
                                                ;  CONTROL
        LCALL   SEND_BYTE                       ;  OSCILLATOR ON DS1307
        LCALL   SEND_STOP
        RET
;-------------------------------------------------------------------------
;       THIS SUB CONTROLS THE SQW OUTPUT
;-------------------------------------------------------------------------
SQW_CONTROL:
        LCALL   SEND_START                      ;  SEND START CONDITION
        MOV     A,#DS1307W                      ;  SET POINTER TO REG 07H ON
                                                ;  DS1307
        LCALL   SEND_BYTE
        MOV     A,#07H
        LCALL   SEND_BYTE

        MOV     A,#90H                          ;  SQW/OUT ON AT 1HZ
        JNB     SQW,SQW_ON                      ;  JUMP IS SQW BIT IS ACTIVE
        MOV     A,#80H                          ;  TURN SQW/OUT OFF - OFF HIGH
SQW_ON:
        LCALL   SEND_BYTE
        LCALL   SEND_STOP
        LCALL   READ_CLOCK                      ;  DISPLAY DATE/TIME
RET
;-------------------------------------------------------------------------
;       THIS SUB IS A SCOPE TRIGGER BIT
;-------------------------------------------------------------------------
TRIGGER:
        CLR     TRIG
        SETB    TRIG
        LCALL   DELAY_4
        CLR     TRIG
RET
;-------------------------------------------------------------------------
;       THIS SUB READS DATA FROM THE SCREEN AND CONVERTS IT TO BCD FORM
;       DATA SHOULD BE HEX DIGITS: 1,2,3...9,A,B,C,D,E,F
;-------------------------------------------------------------------------
READ_BCD:
        MOV     R0,#0                           ;  CLEAR R0 BCD_LOOP:
        LCALL   READ_DATA                       ;  READ BYTE FROM KEYBOARD
        LCALL   WRITE_DATA                      ;  WRITE BYTE BACK TO SCREEN
        CJNE    A,#0DH,BCD                      ;  CHECK FOR CR
        MOV     A,R0                            ;  MOVE R0 TO ACC AND RETURN
        RET
```

```
BCD:
        ADD     A,#-30H                         ;  BEGIN TO CONVERT TO ACTUAL
                                                ;  VALUE
        JNB     ACC.4,NUMBER                    ;  JUMP IF NOT A-F
        ADD     A,#-07H                         ;  IF A-F SUBTRACT 7
                                                ;  NUMBER:
        ANL     A,#0FH                          ;  ENSURE BITS 4-7 ARE CLEARED
        ANL     0,#0FH                          ;  ENSURE BITS 4-7 ARE CLEARED
        XCH     A,R0                            ;  EXCHANGE R0 AND ACC
        SWAP    A                               ;  NIBBLE SWAP ACC
        ORL     A,R0                            ;  INSERT BITS 0-3 OF R0 INTO
                                                ;  ACC
        MOV     R0,A                            ;  MOVE ACC INTO R0
        SJMP    BCD_LOOP                        ;  LOOP UNTIL CR ENCOUNTERED
;-------------------------------------------------------------------------
;       THIS SUB WRITES THE BYTE TO THE SCREEN
;-------------------------------------------------------------------------
WRITE_BCD:
        PUSH    ACC                             ;  SAVE ACC ON STACK
        SWAP    A                               ;  NIBBLE SWAP ACC
        ANL     A,#0FH                          ;  CLEAR BITS 4-7 OF ACC
        ADD     A,#07H                          ;  ADD 7 TO ACC TO CONVERT TO
                                                ;  ASCII HEX
        JNB     ACC.4,LESSNINE                  ;  CHECK TO SEE IF LESS THAN
                                                ;  NINE 0-8
        CJNE    A,#10H,NOTNINE                  ;  JUMP IS GREATER THAN NINE
                                                ;  A-F
LESSNINE:
        ADD     A,#-07H                         ;  SUBTRACT 7 FOR 0-9
NOTNINE:
        ADD     A,#30H                          ;  ADD 30 TO CONVERT TO ASCII
                                                ;  EQUIVALENT
        LCALL   WRITE_DATA                      ;  WRITE BYTE TO SCREEN
        POP     ACC                             ;  RECALL ACC FROM STACK
        ANL     A,#0FH                          ;  PERFORM CONVERSION ON OTHER
                                                ;  HALF OF BYTE
        ADD     A,#07H
        JNB     ACC.4,NINE2
        CJNE    A,#10H,NOTNINE2
NINE2:
        ADD     A,#-07H
NOTNINE2:
        ADD     A,#30H
        LCALL   WRITE_DATA
        RET
;-------------------------------------------------------------------------
;-------------------------------------------------------------------------
READ_DATA:
        JNB     RI,READ_DATA                    ;  LOOP WHILE RI BIT IS LOW
        CLR     RI                              ;
        MOV     A,SBUF                          ;  GET DATA BYTE FROM SERIAL
```

```
                                                    ;  BUFFER
        RET
;-------------------------------------------------------------------------
;-------------------------------------------------------------------------
WRITE_DATA:
        JNB     TI,WRITE_DATA                       ;  LOOP WHILE TI BIT IS LOW
        CLR     TI                                  ;
        MOV     SBUF,A                              ;  SEND DATA BYTE TO SERIAL
                                                    ;  BUFFER
        RET
;-------------------------------------------------------------------------
;-------------------------------------------------------------------------
WRITE_TEXT:
        PUSH    ACC                                 ;  SAVE ACC BYTE ON STACK WT1:
        CLR      A                                  ;  CLEAR ACC
        MOVC    A,@A+DPTR                           ;  MOVE FIRST BYTE OF STRING
                                                    ;  TO ACC
        INC     DPTR                                ;  INC DATA POINTER
        CJNE    A,#0,WT2                            ;  CHECK FOR STRING
                                                    ;  TERMINATOR - 0
        POP     ACC                                 ;  RESTORE ACC
        RET                                         ;  RETURN WHEN STRING IS SENT
WT2:
        LCALL   WRITE_DATA                          ;  SEND BYTE OF STRING OVER
                                                    ;  SERIAL PORT
        SJMP    WT1
;-------------------------------------------------------------------------
;       TEXT STRINGS USED FOR USER INTERFACE OVER SERIAL PORT
;-------------------------------------------------------------------------
YEAR:
        DB      CR,LF,'YEAR (0 - 99)   :       ',0
MONTH:
        DB       CR,LF,'MONTH (1 - 12) :       ',0
DAY:
        DB      CR,LF,'DAY OF MONTH    :       ',0
DAYW:
        DB      CR,LF,'DAY OF WEEK     :       ',0
HOUR:
        DB      CR,LF,'HOUR (0 - 23)   :       ',0
MINUTE:
        DB      CR,LF,'MINUTE (0 - 59) :       ',0
SECOND:
        DB      CR,LF,'SECOND (0 - 59) :       ',0
TRIER:
        DB      CR,LF,'PRESS ANY KEY TO SET THIS TIME ',CR,LF,0
TEXT0:
        DB      CR,LF,'******* DALLAS SEMICONDUCTOR *******  '
        DB      CR,LF,'   DS1307 DEMONSTRATION PROGRAM       ',CR,LF
        DB      CR,LF,'PLEASE CHOOSE AN OPTION TO CONTINUE   '
        DB      CR,LF,'------------------------------------  '
        DB      CR,LF,'A. SET TIME            B. SET RAM     '
```

```
        DB      CR,LF,'C. READ DATE/TIME      D. READ RAM     '
        DB      CR,LF,'E. OSC ON              F. OSC OFF      '
        DB      CR,LF,'G. SQW/OUT ON-1HZ      H. SQW/OUT OFF  '
        DB      CR,LF,'ESC. TO QUIT                           ',0
TEXT1:
        DB      CR,'DATE:       ',0
TEXT2:
        DB      'TIME:  ',0
TEXT3:
        DB      CR,LF,0
TEXT4:
        DB      CR,LF,'PRESS ANY KEY TO READ TO END READ DATE/TIME'
        DB      CR,LF,0
TEXT5:
        DB      CR,LF,'ENTER THE BYTE VALUE WHICH WILL FILL THE RAM'
        DB      CR,LF,0
TEXT6:
        DB      CR,LF,'RAM             RAM'
        DB      CR,LF,'ADDR            DATA'
        DB      CR,LF,'----------------------------'
        DB      CR,LF,0
;****************************************
;**** END OF PROGRAM ********************
;****************************************
; END
; End of Program.
```

INTELLIGENT SOCKETS

4

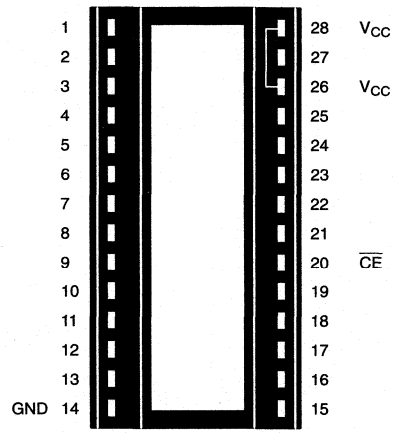
DALLAS SEMICONDUCTOR

DS1213B
SmartSocket 16K/64K

FEATURES

- Accepts standard 2K x 8 or 8K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 2K x 8 to 8K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



28-PIN INTELLIGENT SOCKET

PIN DESCRIPTION

$\overline{CE}$ – Conditioned Chip Enable
V_{CC} – Switched V_{CC}
GND – Ground
All pins pass through except 20, 26 and 28.

DESCRIPTION

The DS1213B SmartSocket is a 28-pin, 600 mil DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either 24-pin 2K x 8 (lower-justified) or 28-pin 8K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility . The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, the internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption.

Using the SmartSocket saves printed circuit board space since the SRAM/SmartSocket combination occupies no more area than the SRAM alone. The SmartSocket modifies only pins 20, 26 and 28, to nonvolatize the RAM. All other pins are passed straight through.

OPERATION

The DS1213B SmartSocket performs five circuit functions required to battery back up a CMOS memory. The first function involves switching between the battery and the V_{CC} supply, depending on which is greater. The switch has a voltage drop of less than 0.2 volts.

The second function is power-fail detection. The DS1213B constantly monitors the V_{CC} supply. When V_{CC} falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable.

The third function, write protection, is accomplished by holding the RAM chip enable signal to within 0.2 volts of V_{CC} or the battery supply whichever is greater. If the incoming chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the current memory cycle is complete to avoid corruption of data. Power fail detection occurs in the range of 4.75 to 4.5 volts. During nominal power supply conditions the chip enable signal will be passed through from the socket pin to the socket contact with a maximum propagation delay of 20 ns.

The fourth function the DS1213B performs is to check battery status to warn of potential data loss. Each time that V_{CC} power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory access to the SmartSocket is inhibited. Battery status can, therefore, be determined by a three–step process. First, a read cycle is performed to any location in the memory, in order to save the contents of that location. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the battery voltage is less than 2.0 V and data is in danger of being corrupted.

The fifth function the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to ensure reliability. The DS1213B SmartSocket provides two batteries and an internal isolation switch to select between them. During battery back up, the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two internal lithium cells has a 45 mAh capacity.

NOTE: As shipped from Dallas Semiconductor, battery voltage cannot be measured on the V_{CC} socket contact. Only after V_{CC} has been applied to the device for the first time and then removed will the battery voltage be present on socket contacts 28, 26 and 20.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	40°C to 70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1,3
Logic 1 PIN 20 L	V_{IH}	2.2		V_{CC}+0.3	V	1,3
Logic 0 PIN 20 L	V_{IL}	-0.3		+ 0.8	V	1,3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Current	I_{CC}			5	mA	3, 4, 5
PIN 26 U, PIN 28 U Supply Voltage	V_{CCO}	V_{CC} -0.2			V	1, 3, 8
PIN 26 U, PIN 28 U Supply Current	I_{CCO}			80	mA	3,8
PIN 20 L $\overline{CE}$ Input Leakage	I_{IL}	-1.0		+1.0	µA	3, 4
PIN 20 U $\overline{CE}$ Output @ 2.4 V	I_{OH}	-1.0			mA	2, 3
PIN 20 U $\overline{CE}$ Output @ .4V	I_{OL}			4.0	mA	2, 3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} < 4.5V)

PIN 20 U Output	V_{OHL}	V_{CC} -0.2 V_{BAT}-0.2			V	1, 3
PIN 26 U, PIN 28U Battery Current	I_{BAT}			1	µA	3, 6
PIN 26 U, PIN 28 U Battery Voltage	V_{BAT}	2	3	3.6	V	1, 3

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance PIN 20 L	C_{IN}			5	pF	3
Output Capacitance PIN 20 U	C_{OUT}			7	pF	3

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2,9
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

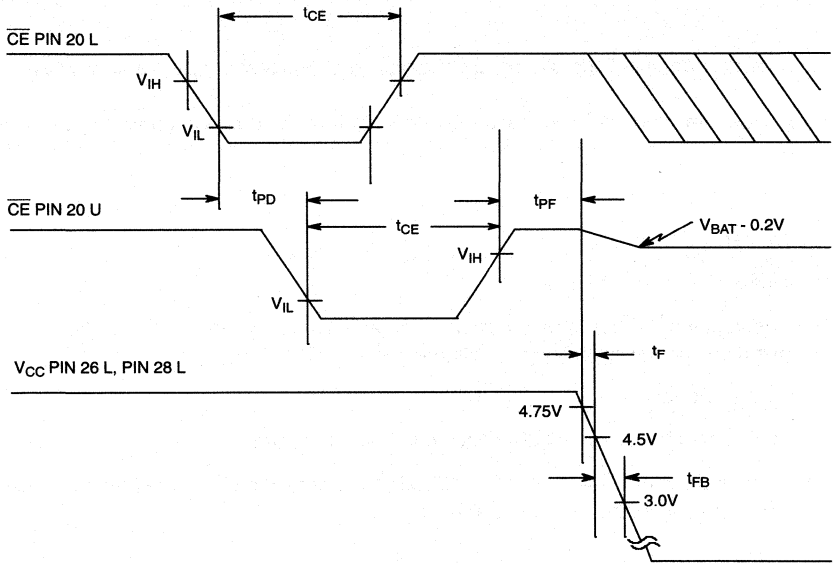
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI} < 4.75 V)

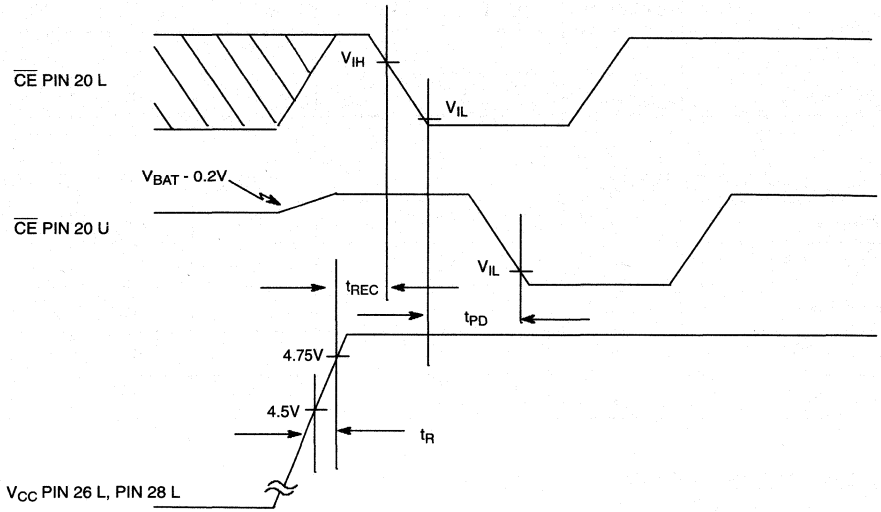
Recovery at Power-Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate 4.75 - 4.5 V	t_F	300			µs	
V_{CC} Slew Rate 4.5 - 3 V	t_{FB}	10			µs	
V_{CC} Slew Rate 4.5-4.75 V	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	7

4

TIMING DIAGRAM: POWER-DOWN



TIMING DIAGRAM: POWER-UP



WARNINGS:

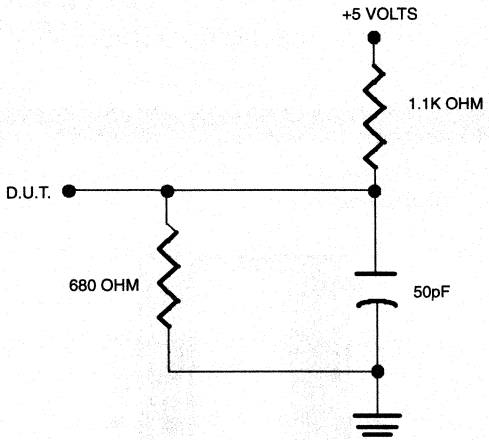
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal will discharge internal lithium source because exposed voltage pins are present.

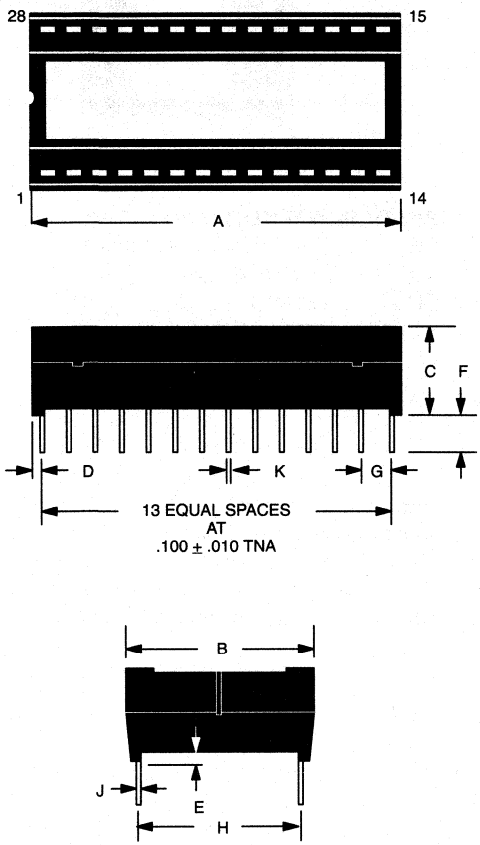
NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Pin locations are designated "U" (for upper) when a parameter definition refers to the socket receptacle and "L" (for lower) when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Pin 26 L may be connected to V_{CC} or left disconnected at the PC board.
6. I_{BAT} is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. t_{CE} max. must be met to ensure data integrity on power loss.
8. V_{CC} is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.

OUTPUT LOAD Figure 1



DS1213B INTELLIGENT SOCKET 28 PIN (FOR 600–MIL DIP)



PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	1.380 35.05	1.420 36.07
B IN. MM	0.690 17.53	0.720 18.29
C IN. MM	0.370 9.39	0.420 10.67
D IN. MM	0.035 0.89	0.065 1.65
E IN. MM	0.015 0.38	0.035 0.89
F IN. MM	0.120 3.04	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

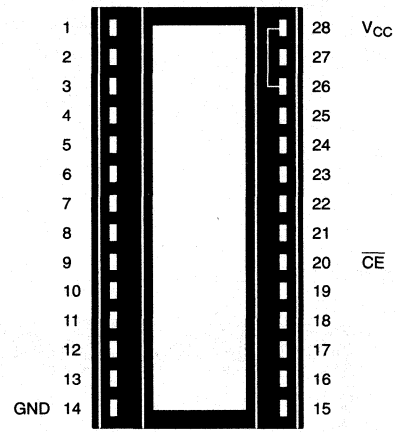
DALLAS SEMICONDUCTOR

DS1213C
SmartSocket 256K

FEATURES

- Accepts standard 32K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



28-PIN INTELLIGENT SOCKET

PIN DESCRIPTION

$\overline{CE}$ – Conditioned Chip Enable
V_{CC} – Switched V_{CC}
GND – Ground
All pins pass through except 20 and 28.

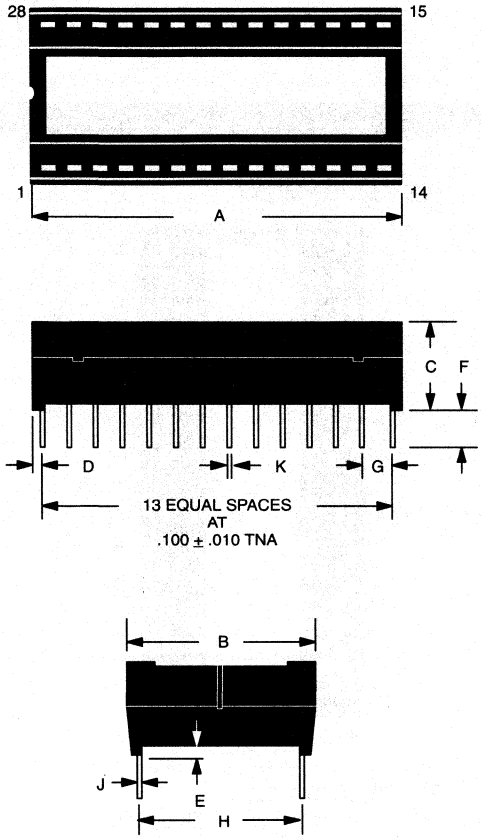
DESCRIPTION

The DS1213C SmartSocket is a 28-pin, 600 mil DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts a 32K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility . The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, the internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption.

Using the SmartSocket saves printed circuit board space since the SRAM/SmartSocket combination occupies no more area than the memory alone. The SmartSocket uses only Pins 20 and 28 for RAM control. All other pins are passed straight through.

See the DS1213B SmartSocket data sheet for technical details.

DS1213C INTELLIGENT SOCKET 28–PIN (FOR 600 MIL DIP)



PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	1.380 35.05	1.420 36.07
B IN. MM	0.690 17.53	0.720 18.29
C IN. MM	0.370 9.39	0.420 10.67
D IN. MM	0.035 0.89	0.065 1.65
E IN. MM	0.015 0.38	0.035 0.89
F IN. MM	0.120 3.04	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

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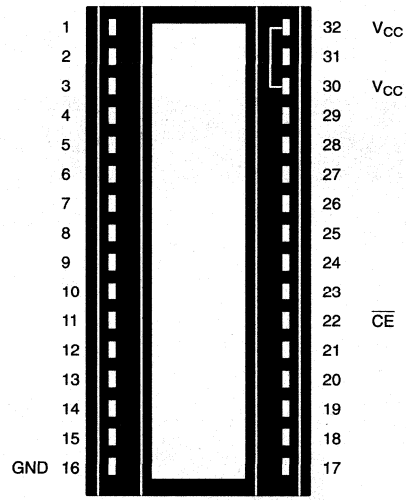
DALLAS SEMICONDUCTOR

DS1213D
SmartSocket 256K/1M

FEATURES

- Accepts standard 32K x 8 or 128K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 32K x 8 to 128K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



32-PIN INTELLIGENT SOCKET
(600 MIL)

PIN DESCRIPTION

$\overline{CE}$ – Conditioned Chip Enable
V_{CC} – Switched V_{CC}
GND – Ground
All pins pass through except 22, 30 and 32.

DESCRIPTION

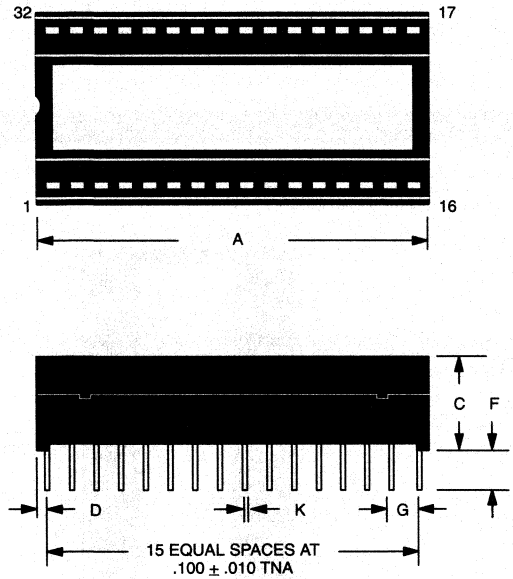
The DS1213D SmartSocket is a 32-pin, 600 mil DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts 32K x 8 or 128K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption.

Using the SmartSocket saves printed circuit board space since the SRAM/SmartSocket combination occupies no more area than the SRAM alone. The SmartSocket uses only Pins 22, 30 and 32 for RAM control. All other pins are passed straight through.

See the DS1213B SmartSocket data sheet for technical details.

See Dallas Semiconductor Application Note 4 for modification instructions to allow use of 512K x 8 RAM with this part.

DS1213D INTELLIGENT SOCKET 32-PIN (600 MIL DIP)



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.580	1.620
MM	40.13	41.15
B IN.	0.690	0.720
MM	17.53	18.29
C IN.	0.350	0.410
MM	8.89	10.4
D IN.	0.035	0.065
MM	0.89	1.65
E IN.	0.015	0.035
MM	0.38	0.89
F IN.	0.120	0.160
MM	3.04	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

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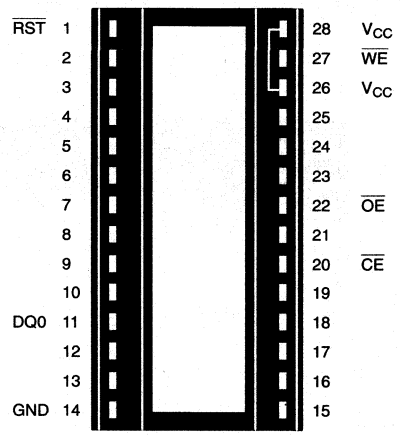
DALLAS SEMICONDUCTOR

DS1216B
SmartWatch/RAM 16K/64K

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 2K x 8 and 8K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min./month @25°C

PIN ASSIGNMENT



28-Pin Intelligent Socket

PIN DESCRIPTION

All Pins Pass Through Except 20, 26, 28

Pin 1	$\overline{RST}$	- Reset
Pin 11	DQ0	- Data Input/Output 0
Pin 14	GND	- Ground
Pin 20	$\overline{CE}$	- Conditioned Chip Enable
Pin 22	$\overline{OE}$	- Output Enable
Pin 26	V_{CC}	- Switched V_{CC} for 24 Pin RAM
Pin 27	$\overline{WE}$	- Write Enable
Pin 28	V_{CC}	- Switched V_{CC} for 28 Pin RAM

DESCRIPTION

The DS1216B SmartWatch/RAM 16/64K is a 28-pin, 600 MIL wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either 24-pin 2K x 8 or 28-pin 8K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS SRAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent loss of watch and RAM data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated RAM take up no more area than the memory alone. The SmartWatch uses pins 28, 27, 26, 22, 20, 11, and 1 for RAM and watch control. All other pins are passed straight through to the socket receptacle.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

OPERATION

Communication with the SmartWatch is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the SmartWatch, and memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the SmartWatch. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

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SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1

	7						0	HEX VALUE
BYTE 0	1	1	0	0	0	1	0	1	C5
BYTE 1	0	0	1	1	1	0	1	0	3A
BYTE 2	1	0	1	0	0	0	1	1	A3
BYTE 3	0	1	0	1	1	1	0	0	5C
BYTE 4	1	1	0	0	0	1	0	1	C5
BYTE 5	0	0	1	1	1	0	1	0	3A
BYTE 6	1	0	1	0	0	0	1	1	A3
BYTE 7	0	1	0	1	1	1	0	0	5C

NOTE:

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the SmartWatch is less than 1 in 10^{19}. This pattern is sent to the SmartWatch LSB to MSB.

NONVOLATILE CONTROLLER OPERATION

The DS1216B SmartWatch performs circuit functions required to make a CMOS RAM nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which voltage is greater. This switch has a voltage drop of less than 0.2 volts. The second function which the SmartWatch provides is power-fail detection. Power-fail detection occurs at approximately 4.0 volts. The DS1216B constantly monitors the V_{CC} supply. When V_{CC} goes out of tolerance, a comparator outputs a power-fail signal to the chip enable logic. The third function accomplishes write protection by holding the chip enable signal to the memory within 0.2 volts of V_{CC} or battery. During nominal power supply conditions the memory chip enable signal will track the chip enable signal sent to the socket with a maximum propagation delay of 20 ns.

SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in eight registers of eight bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each register must be handled in groups of eight bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

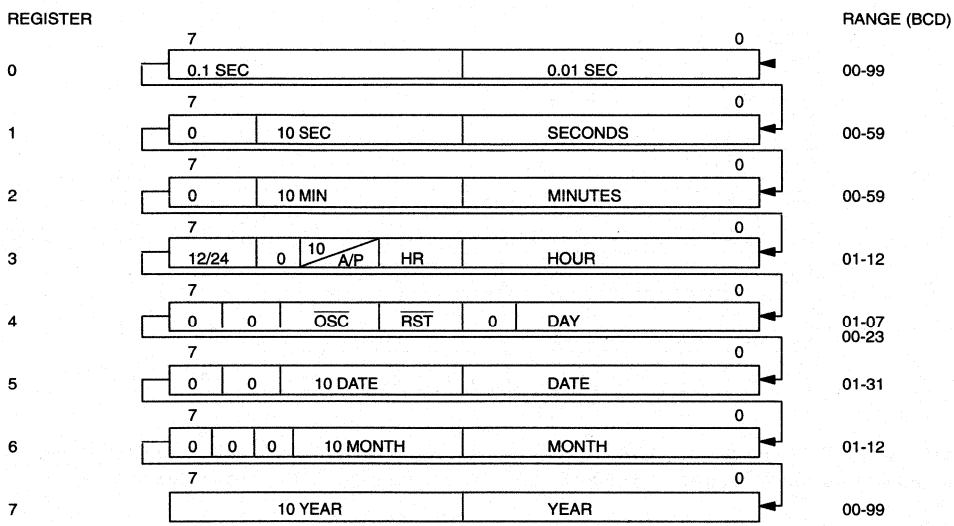
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{RESET}$ and oscillator functions. Bit 4 controls the $\overline{RESET}$ (pin 1). When the $\overline{RESET}$ bit is set to logic 1, the $\overline{RESET}$ input pin is ignored. When the $\overline{RESET}$ bit is set to logic 0, a low input on the $\overline{RESET}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

SMARTWATCH REGISTER DEFINITION Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, PIN 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1, 3
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 10
Logic 0	V_{IL}	-0.3		+0.8	V	1, 10

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, PIN 28L Supply	I_{CCI}			5	mA	3,4,5
PIN 26U, PIN 28U Supply Voltage	V_{CCO}	V_{CC}-0.2			V	3, 8
PIN 26U, PIN 28U Supply Current	I_{CCO}			80	mA	3,8
Input Leakage	I_{IL}	-1.0		+1.0	µA	4,10,13
Output @ 2.4V	I_{OH}	-1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

(0°C to 70°C; V_{CC} < 4.5V)

PIN 20U Output	V_{OHL}	V_{CC}-0.2 V_{BAT}-0.2			V	3
PIN 26U, PIN 28U Battery Current	I_{BAT}			1	µA	3,6
PIN 26U, PIN 28U Battery Voltage	V_{BAT}	2	3	3.6	V	3

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

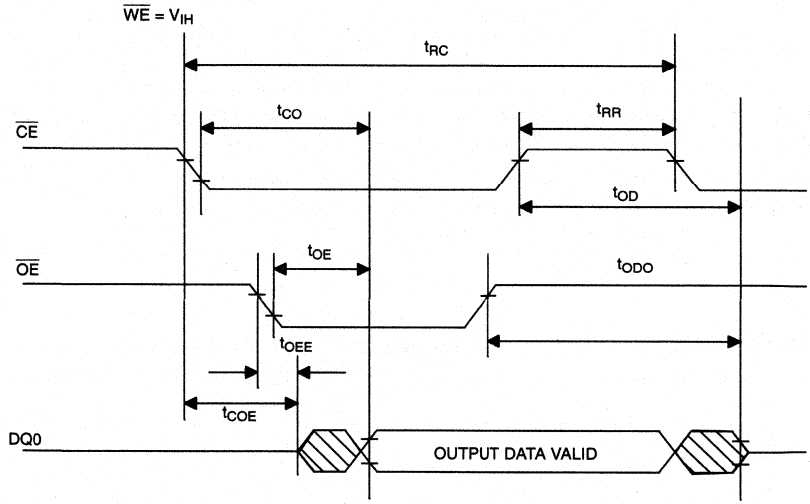
(0°C to 70°C; V_{CC}=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ To Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ To Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ To Output High Z	t_{OD}			100	ns	
$\overline{OE}$ To Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	11
Data Setup Time	t_{DS}	100			ns	12
Data Hold Time	t_{DH}	0			ns	12
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
$\overline{RESET}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 9
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	

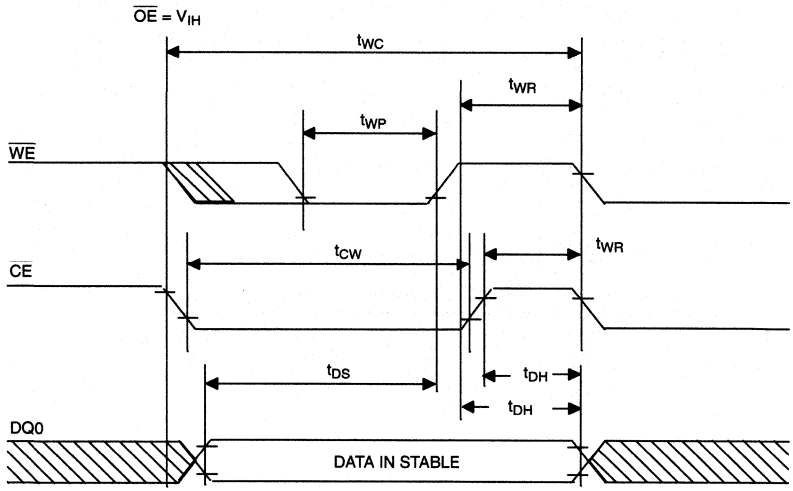
(0°C to 70°C; V_{CC} <4.5V)

Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3V	t_F	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	7

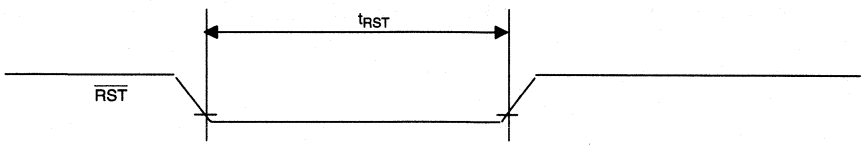
TIMING DIAGRAM: READ CYCLE TO SMARTWATCH



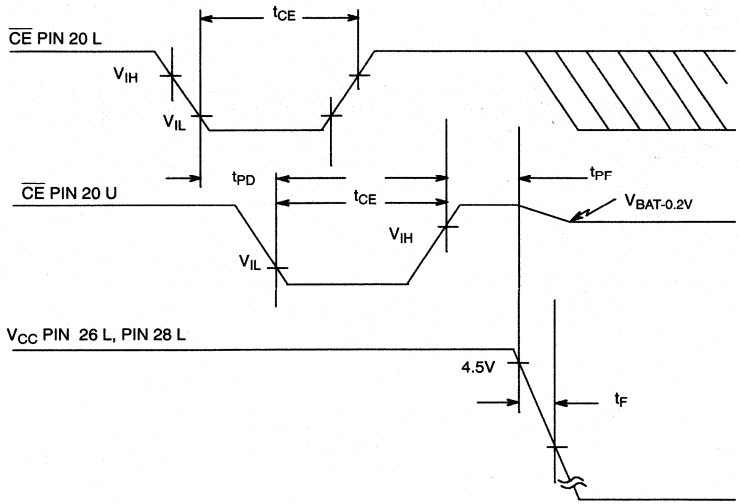
TIMING DIAGRAM: WRITE CYCLE TO SMARTWATCH



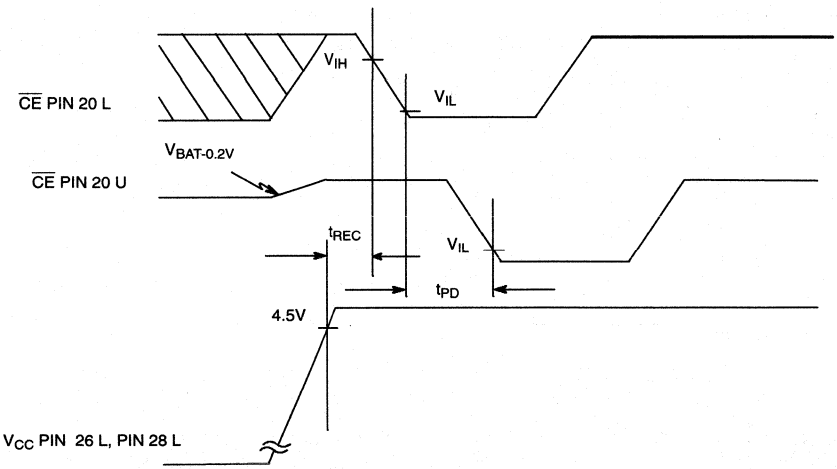
TIMING DIAGRAM: RESET FOR SMARTWATCH



TIMING DIAGRAM: POWER-DOWN



TIMING DIAGRAM: POWER-UP



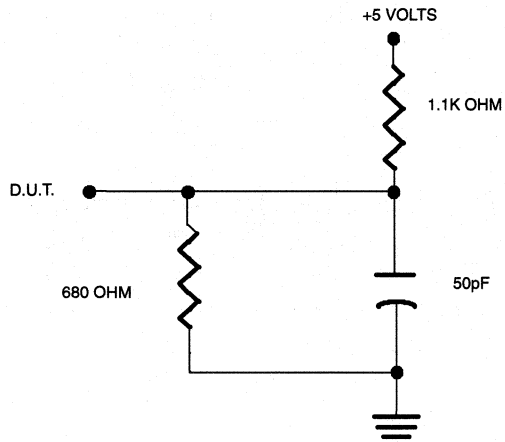
WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode. Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

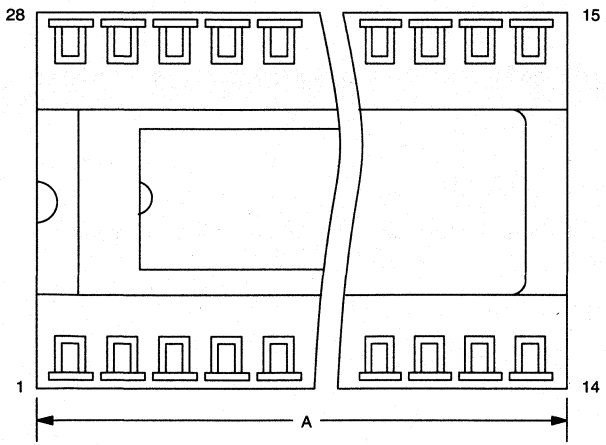
NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 3.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Pin 26L can be connected to V_{CC} or left disconnected at the PC board.
6. I_{BAT} is the maximum current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. t_{CE} max. must be met to ensure data integrity on power loss.
8. V_{CC} is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.
10. Applies to Pins 1 L, 11 L, 20 L, 22 L, and 27 L.
11. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
12. t_{DH} and t_{DS} are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
13. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.

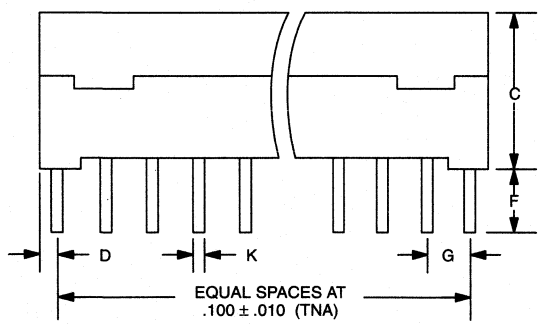
OUTPUT LOAD Figure 3

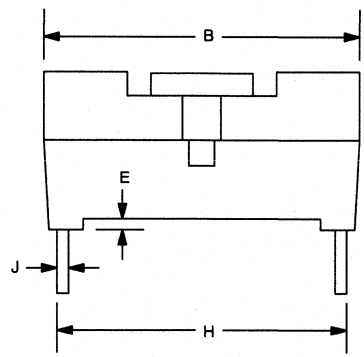


DS1216B SMARTWATCH



PKG	28-PIN		32-PIN	
DIM	MIN	MAX	MIN	MAX
A IN. MM	1.390 35.31	1.420 36.07	1.580 40.13	1.620 41.14
B IN. MM	0.690 17.53	0.720 18.29	0.690 17.53	0.720 18.29
C IN. MM	0.370 9.39	0.420 10.67	0.350 8.89	0.410 10.40
D IN. MM	0.035 0.89	0.065 1.65	0.035 0.89	0.065 1.65
E IN. MM	0.015 0.38	0.035 0.89	0.015 0.38	0.035 0.89
F IN. MM	0.120 3.04	0.160 4.06	0.120 3.04	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53





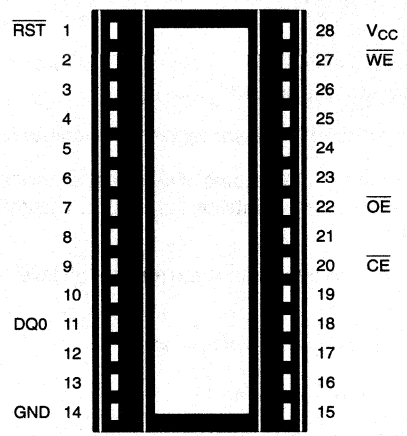
DALLAS SEMICONDUCTOR

DS1216C
SmartWatch/RAM 64K/256K

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 8K x 8 and 32K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min./month @ 25°C

PIN ASSIGNMENT



28-Pin Intelligent Socket

PIN DESCRIPTION

All pins pass through except 20, 28.

Pin 1	$\overline{RST}$	- $\overline{RESET}$
Pin 11	DQ0	- Data Input/Output 0
Pin 14	GND	- Ground
Pin 20	$\overline{CE}$	- Conditioned Chip Enable
Pin 22	$\overline{OE}$	- Output Enable
Pin 27	$\overline{WE}$	- Write Enable
Pin 28	V_{CC}	- Switched V_{CC}

DESCRIPTION

The DS1216C SmartWatch/RAM is a 28-pin, 600 MIL wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K x 8 or a 32K x 8 JEDEC bytewide CMOS stat ic RAM. When the socket is mated with a CMOS SRAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

See the DS1216B SmartWatch/RAM 16/64K data sheet for technical details.

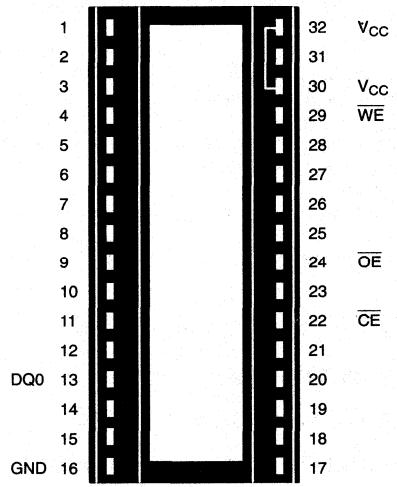
DALLAS SEMICONDUCTOR

DS1216D
SmartWatch/RAM 256K/1M

FEATURES

- Converts standard 8K x 8, 32K x 8, 128K x 8, and 512K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min./month @ 25°C

PIN ASSIGNMENT



32-Pin Intelligent Socket

PIN DESCRIPTION

All pins pass through except 22, 30 and 32.

Pin 1	$\overline{RST}$	- RESET
Pin 13	DQ0	- Data Input/Output 0
Pin 16	GND	- Ground
Pin 22	$\overline{CE}$	- Conditioned Chip Enable
Pin 24	$\overline{OE}$	- Output Enable
Pin 29	$\overline{WE}$	- Write Enable
Pin 30	V_{CC}	- Switched V_{CC} for 28-pin RAM
Pin 32	V_{CC}	- Switched V_{CC} for 32-pin RAM

DESCRIPTION

The DS1216D SmartWatch/RAM 256K/1M is a 32-pin, 600 MIL wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K x 8, 32K x 8, 128K x 8, or 512K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS SRAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

See the DS1216B SmartWatch/RAM 16/64K data sheet for technical details.

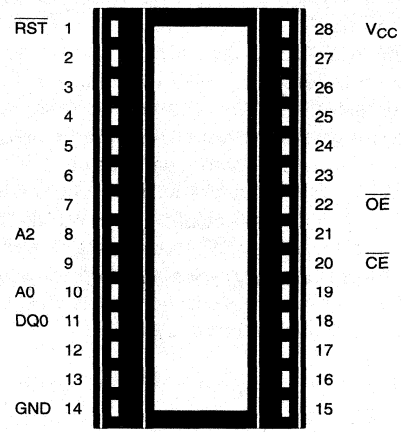
DALLAS SEMICONDUCTOR

DS1216E
SmartWatch/ROM 64K/256K

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of month, months, and years
- Adds timekeeping to any 28-pin JEDEC bytewide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% V_{CC} operating range
- Operating temperature range 0°C to 70°C
- Accurate to within ±1 minute/month @25°C

PIN ASSIGNMENT



28-Pin Intelligent Socket

PIN DESCRIPTION

Pin 1	$\overline{RST}$	- Reset
Pin 8	A2	- Address Bit 2 ($\overline{READ/WRITE}$)
Pin 10	A0	- Address Bit 0 (Data Input)
Pin 11	DQ0	- I/O_0 (Data Output)
Pin 14	GND	- Ground
Pin 20	$\overline{CE}$	- Conditioned Chip Enable
Pin 22	$\overline{OE}$	- Output Enable
Pin 28	V_{CC}	- +5 VDC to the Socket

All pins pass through to the socket except 20.

DESCRIPTION

The DS1216E SmartWatch/ROM 64/256K is a 28-pin, 600 mil-wide DIP socket with a built-in CMOS timekeeper function and an embedded lithium energy source to maintain time and date. It accepts any 28-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeper function remains transparent to the memory device placed above. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on to prevent loss of watch data.

Using the SmartWatch saves PC board space since the combination of the SmartWatch and the mated memory device takes up no more area than the memory alone. The SmartWatch uses pins 1, 8, 10, 11, 20, and 22 for timekeeper control. All pins pass through to the socket receptacle except for pin 20 ($\overline{CE}$), which is inhibited during the transfer of time information.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, days, date, month, and year information. The

date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

OPERATION

A highly structured sequence of 64 cycles is used to gain access to time information and temporarily disconnects the mated memory from the system bus. Information transfer into and out of the SmartWatch is achieved by using address bits A0 and A2, control signals $\overline{OE}$ and $\overline{CE}$, and data I/O line DQ0. All SmartWatch data transfers are accomplished by executing read cycles to the mated memory address space. Write and read functions are determined by the level of address bit A2. When address bit A2 is low, a write cycle is enabled and data must be input on address bit A0. When address bit A2 is high, a read cycle is enabled and data is output on data I/O line DQ0. Either control signal ($\overline{OE}$ or $\overline{CE}$) must transition low to begin and high to end memory cycles that are directed to the SmartWatch. However, both control signals must be in an active state during a memory cycle.

Communication with the SmartWatch is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles, placing address bit A2 low with the proper data on address bit A0. The 64 write cycles are used only to gain access to the SmartWatch. Prior to executing the first of 64 write cycles, a read cycle should be executed by holding A2 high. The read cycle will reset the comparison register pointer within the SmartWatch, ensuring the pattern recognition starts with the first bit of the sequence. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison reg ister and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above, until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive data on Data In (A0) or transmit data on Data Out (DQ0), depending on the level of $\overline{READ}$/$\overline{WRITE}$ (A2). Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ and $\overline{OE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

An unconditional reset to the SmartWatch occurs by either bringing A14 ($\overline{RESET}$) low if enabled, or on power-up. The $\overline{RESET}$ can occur during pattern recognition or while accessing the SmartWatch registers. $\overline{RESET}$ causes access to abort and forces the comparison register pointer back to Bit 0 without changing registers.

NONVOLATILE CONTROLLER OPERATION

The DS1216E SmartWatch performs circuit functions required to make the timekeeping function nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which voltage is greater. The second function provides power-fail detection. Power-fail detection typically occurs at approximately 4.0 volts. Finally, the nonvolatile controller protects the SmartWatch register contents by ignoring any inputs after power-fail detection has occurred. Power-fail detection also has the same effect on data transfer as the $\overline{RESET}$ input.

SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in eight registers of eight bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of eight bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logic 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logic 0, a low input on the $\overline{\text{RESET}}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is turned off. When set to logic 0, the oscillator turns on and the watch becomes operational. Both bits are set to a logic 1 when shipped from the factory

ZERO BITS

Registers 1,2,3,4,5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1

	7	6	5	4	3	2	1	0	HEX VALUE
BYTE 0	1	1	0	0	0	1	0	1	C5
BYTE 1	0	0	1	1	1	0	1	0	3A
BYTE 2	1	0	1	0	0	0	1	1	A3
BYTE 3	0	1	0	1	1	1	0	0	5C
BYTE 4	1	1	0	0	0	1	0	1	C5
BYTE 5	0	0	1	1	1	0	1	0	3A
BYTE 6	1	0	1	0	0	0	1	1	A3
BYTE 7	0	1	0	1	1	1	0	0	5C

NOTE:

The pattern recognition sequence in Hex is C5, 3A, 5C, C5, 3A, A3, 5C. The odds of this pattern accidentally occurring and causing inadvertent entry to the SmartWatch are less than 1 in 10^{19}. This pattern is sent to the SmartWatch LSB to MSB.

SMARTWATCH REGISTER DEFINITION Figure 2

REGISTER	7							0	RANGE (BCD)
0	0.1 SEC							0.01 SEC	00–99
1	0	10 SEC						SECONDS	00–59
2	0	10 MIN						MINUTES	00–59
3	12/24	0	10 A/P		HR			HOUR	01–12
4	0	0	$\overline{\text{OSC}}$	$\overline{\text{RST}}$	0			DAY	01–07 00–23
5	0	0	10 DATE					DATE	01–31
6	0	0	0	10 MONTH				MONTH	01–12
7	10 YEAR							YEAR	00–99

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1, 3
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 6
Logic 0	V_{IL}	-0.3		+0.8	V	1, 6

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 28L, Supply Current	I_{CCI}			5	mA	3,4
Input Leakage	I_{IL}	-1.0		+1.0	µA	4,6,10
Output @ 2.4V	I_{OH}	-1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

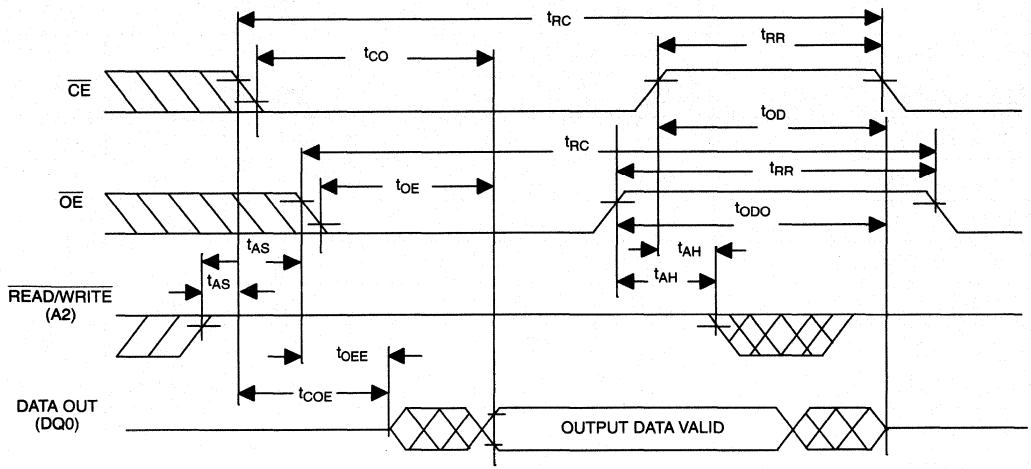
(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ To Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ To Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ To Output High Z	t_{OD}			100	ns	
$\overline{OE}$ To Output High Z	t_{ODO}			100	ns	
Address Setup Time	t_{AS}	20			ns	9
Address Hold Time	t_{AH}			10	ns	8
Read Recovery	t_{RR}	50			ns	7
Write Cycle Time	t_{WC}	250			ns	
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
$\overline{OE}$ Pulse Width	t_{OW}	170			ns	
Write Recovery	t_{WR}	50			ns	7
Data Setup Time	t_{DS}	100			ns	8
Data Hold Time	t_{DH}	0			ns	8
$\overline{RST}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2,5
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	

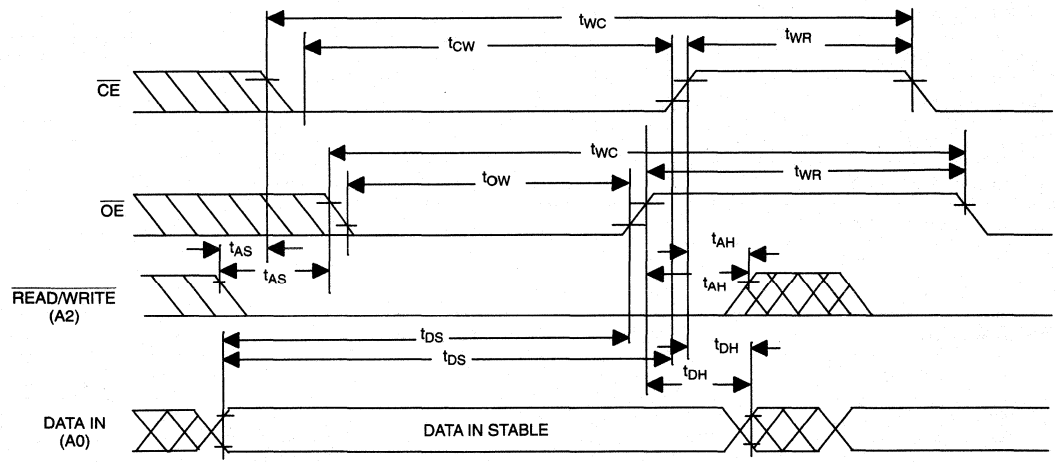
(0°C to 70°C; V_{CC} < 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3V	t_F	0			µs	

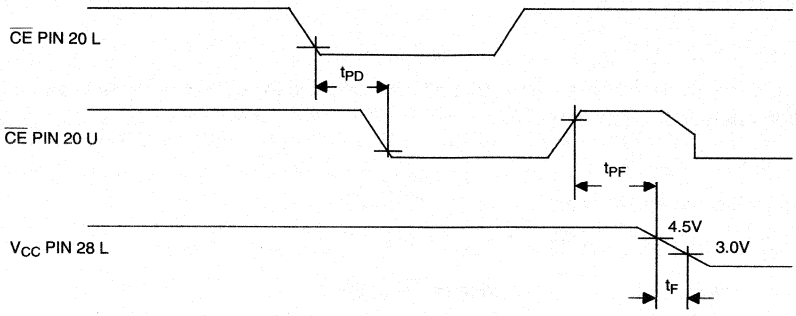
TIMING DIAGRAM: READ CYCLE



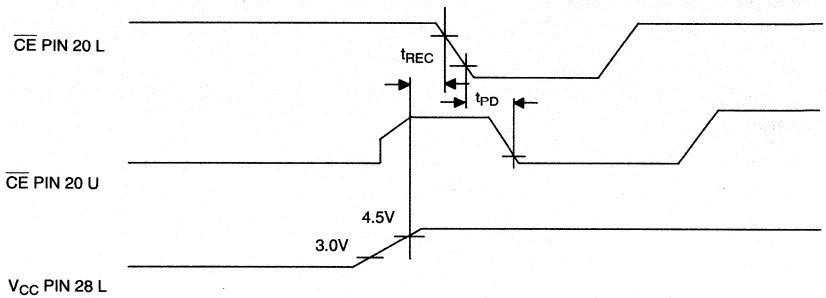
TIMING DIAGRAM: WRITE CYCLE



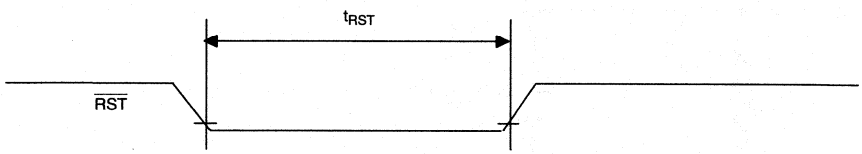
TIMING DIAGRAM: POWER-DOWN



TIMING DIAGRAM: POWER-UP



TIMING DIAGRAM: RESET FOR SMARTWATCH

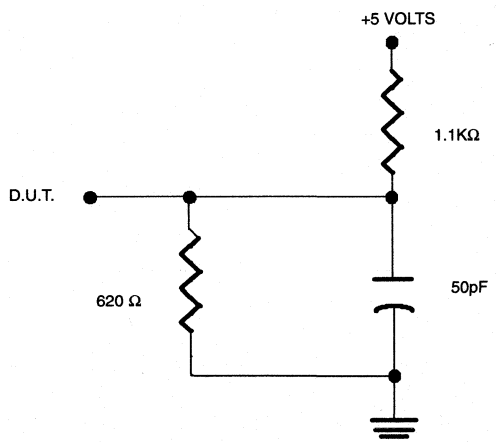


WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.
Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

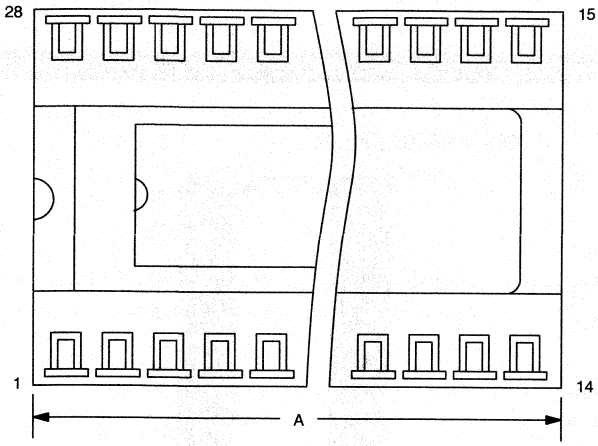
NOTES:

1. All voltages are referenced to ground.
2. Measured with a load shown in Figure 3.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Input pulse rise and fall times equal 10 ns.
6. Applies to pins 1 L, 8 L, 10 L, 20 L, and 22 L.
7. t_{WR} and t_{RR} are functions of the first occurring edge of $\overline{OE}$ or $\overline{CE}$.
8. t_{AH}, t_{DS}, and t_{DH} are functions of the first occurring edge of $\overline{OE}$ or $\overline{CE}$.
9. t_{AS} is a function of the latter occurring edge of $\overline{OE}$ or $\overline{CE}$.
10. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.

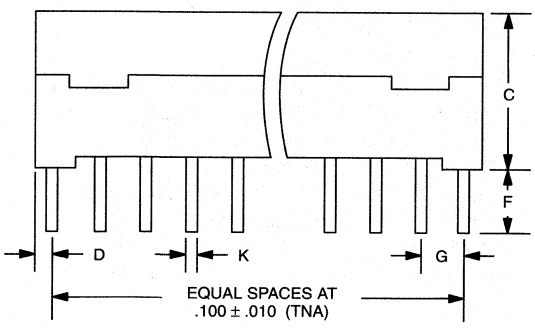
OUTPUT LOAD Figure 3

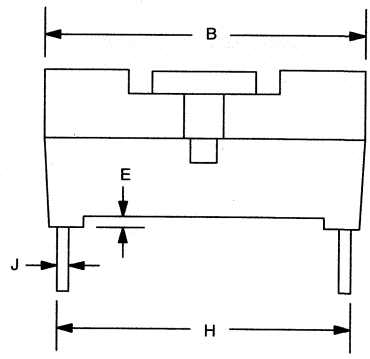


DS1216E SMARTWATCH



PKG	28-PIN		32-PIN	
DIM	MIN	MAX	MIN	MAX
A IN. MM	1.390 35.31	1.420 36.07	1.580 40.13	1.620 41.14
B IN. MM	0.690 17.53	0.720 18.29	0.690 17.53	0.720 18.29
C IN. MM	0.370 9.39	0.420 10.67	0.350 8.89	0.410 10.40
D IN. MM	0.035 0.89	0.065 1.65	0.035 0.89	0.065 1.65
E IN. MM	0.015 0.38	0.035 0.89	0.015 0.38	0.035 0.89
F IN. MM	0.120 3.04	0.160 4.06	0.120 3.04	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53





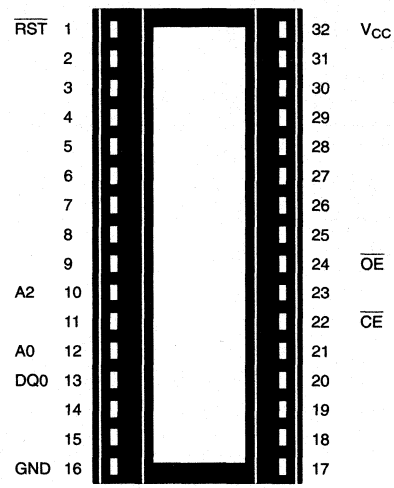
DALLAS SEMICONDUCTOR

DS1216F
SmartWatch/ROM 64K/256K/1M

FEATURES

- Adds timekeeping to any 32-pin JEDEC bytewide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% V_{CC} operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C

PIN ASSIGNMENT



32-PIN INTELLIGENT SOCKET

PIN DESCRIPTION

Pin 1	$\overline{RST}$	- RESET
Pin 10	A2	- Address Bit 2 (READ/ $\overline{WRITE}$)
Pin 12	A0	- Address Bit 0 (Data Input)
Pin 13	DQ0	- I/O_0 (Data Output)
Pin 16	GND	- Ground
Pin 22	$\overline{CE}$	- Conditioned Chip Enable
Pin 24	$\overline{OE}$	- Output Enable
Pin 32	V_{CC}	- +5 VDC to the Socket

All pins pass through to the socket except 22.

DESCRIPTION

The DS1216F SmartWatch/ROM is a 32-pin, 600 mil-wide DIP socket with a built-in CMOS timekeeper and an embedded lithium energy source to maintain time and date. It accepts any 32-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeping function remains transparent to the memory device placed above. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source automatically switches on to prevent loss of time and calendar data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated memory device takes up no more area than the memory alone. The SmartWatch uses pins 1, 10, 12, 13, 22, and 24 for timekeeper control. All pins pass through to the socket receptacle except for pin 22 ($\overline{CE}$), which is inhibited during the transfer of time information.

See the DS1216E SmartWatch/ROM/64/256K data sheet for technical details.

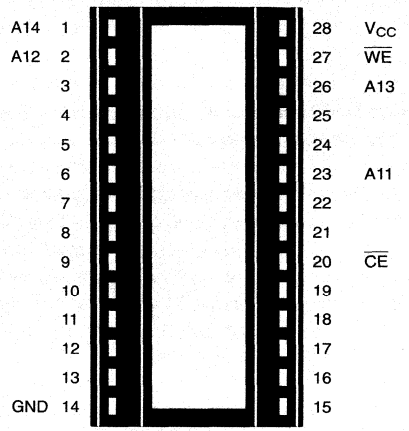
DALLAS SEMICONDUCTOR

DS1613C
Partitionable 256K SmartSocket

FEATURES

- Accepts standard 32K x 8, CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Unconditionally write protects all of memory when V_{CC} is out of tolerance
- Write protects selected blocks of memory when programmed
- Automatically switches to battery backup supply when power fail occurs
- Data retention time is greater than 10 years with the proper RAM selection
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



28-PIN INTELLIGENT SOCKET

PIN DESCRIPTION

A11–A14	–	Address Lines
$\overline{CE}$	–	Conditioned Chip Enable
$\overline{WE}$	–	Conditioned Write Enable
V_{CC}	–	Switched V_{CC}
GND	–	Ground

All pins pass through except 20, 28, and 27.

DESCRIPTION

The DS1613C SmartSocket is a 28-pin, 600 mil DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts a 32K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, on internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt programs important data.

Using the SmartSocket saves printed circuit board space since the SRAM/SmartSocket combination occupies no more area than the SRAM alone. The SmartSocket modifies only pins 20, 27 and 28 to nonvolatize the RAM. All other pins are passed straight through. Pins 1, 2, 23, and 26 are address inputs used to program memory partitions.

OPERATION

The DS1613C SmartSocket performs five circuit functions required to battery back up a CMOS memory. The first function involves switching between the battery and the V_{CC} supply, depending on which is greater. The switch has a voltage drop of less than 0.2 volts.

The second function is power-fail detection. The DS161C constantly monitors the V_{CC} supply. When V_{CC} falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable.

The third function, write protection, is accomplished by holding the RAM chip enable signal to within 0.2 volts of V_{CC} or the battery supply whichever is greater. If the incoming chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the current memory cycle is complete to avoid corruption of data. Power fail detection occurs in the range of 4.75 to 4.5 volts. During nominal power supply conditions the chip enable signal will be passed through from the socket pin to the socket contact with a maximum propagation delay of 20 ns.

The fourth function the DS1613C performs is to check battery status to warn of potential data loss. Each time that V_{CC} power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory access to the SmartSocket is inhibited. Battery status can, therefore, be determined by a three–step process. First, a read cycle is performed to any location in the memory, in order to save the contents of that location. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the battery voltage is less than 2.0 V and data is in danger of being corrupted.

The fifth function the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to ensure reliability. The DS1613C SmartSocket provides two batteries and an internal isolation switch to select between them. During battery back up, the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two internal lithium cells has a 45 mAh capacity.

NOTE: As shipped from Dallas Semiconductor, battery voltage cannot be measured on the V_{CC} socket contact. Only after V_{CC} has been applied to the device for the first time and then removed will the battery voltage be present on socket contacts 28, 26 and 20.

PARTITION PROGRAMMING MODE

The register controlling the partitioning logic switch is selected by recognition of a specific binary pattern which is sent on address lines A11-A14. These address lines are normally the four upper–order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycles will load the partition register. Since there are 16 protectable partitions, the size of each partition is 32K/16 or 2K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A11 through A14 and shown in Table 2. A logical 1 in a bit location write protects the corresponding partition. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A12 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1613C to internally inhibit $\overline{WE}$ whenever A14 A13 A12 A11=0101. Note that while programming the partition register, data which is being accessed from the RAM should be ignored, since the purpose of the 16 read cycles is to program the partition switch, not to access data from RAM.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A11	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A12	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A13	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A14	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST BITS ENTERED

4

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{14} A_{13} A_{12} A_{11})
A11	BIT 21	PARTITION 0	0000
A12	BIT 21	PARTITION 1	0001
A13	BIT 21	PARTITION 2	0010
A14	BIT 21	PARTITION 3	0011
A11	BIT 22	PARTITION 4	0100
A12	BIT 22	PARTITION 5	0101
A13	BIT 22	PARTITION 6	0110
A14	BIT 22	PARTITION 7	0111
A11	BIT 23	PARTITION 8	1000
A12	BIT 23	PARTITION 9	1001
A13	BIT 23	PARTITION 10	1010
A14	BIT 23	PARTITION 11	1011
A11	BIT 24	PARTITION 12	1100
A12	BIT 24	PARTITION 13	1101
A13	BIT 24	PARTITION 14	1110
A14	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28 L Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1, 3
Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	1, 3
Logic 0	V_{IL}	-0.3		+0.8	V	1, 3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28 L Supply Current	I_{CC}			5	mA	3, 4, 5
Pin 28 U Supply Voltage	V_{CCO}	V_{CC}-0.2			V	1, 3, 7
Pin 28 U Supply Current	I_{CCO}			150	mA	3, 7
Pin 20 L $\overline{CE}$, Pin 27 L $\overline{WE}$ Input Leakage Address A11-A14	I_{IL}	-1.0		+1.0	µA	3, 4
Pin 20 U $\overline{CE}$, Pin 27 U $\overline{WE}$ Output @ 2.4V	I_{OH}	-1.0			mA	2, 3
Pin 20 U $\overline{CE}$, Pin 27 U $\overline{WE}$ Output @ 0.4V	I_{OL}			4.0	mA	2, 3

DC ELECTRICAL CHARACTERISTICS

0° to 70°C; V_{CC} < 4.5V

Pin 20 U Output Pin 27 U Output	V_{OLH}	V_{CC}-0.2 V_{BAT}-0.2			V	1, 3
Pin 28 U Battery Current	I_{BAT}			1		3
Pin 28 U Battery Voltage	V_{BAT}	2	3	3.6	V	1, 3

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3
Output Capacitance Pin 27 U, Pin 20 U	C_{OUT}			7	pF	3

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{WE}$, $\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 8
$\overline{WE}$, $\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	10			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

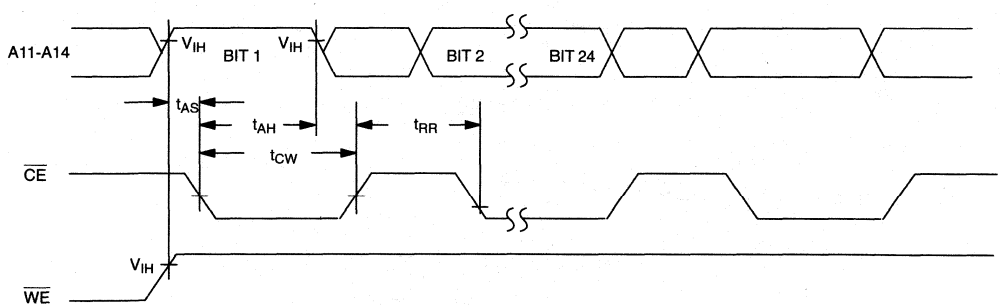
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI} < 4.75V)

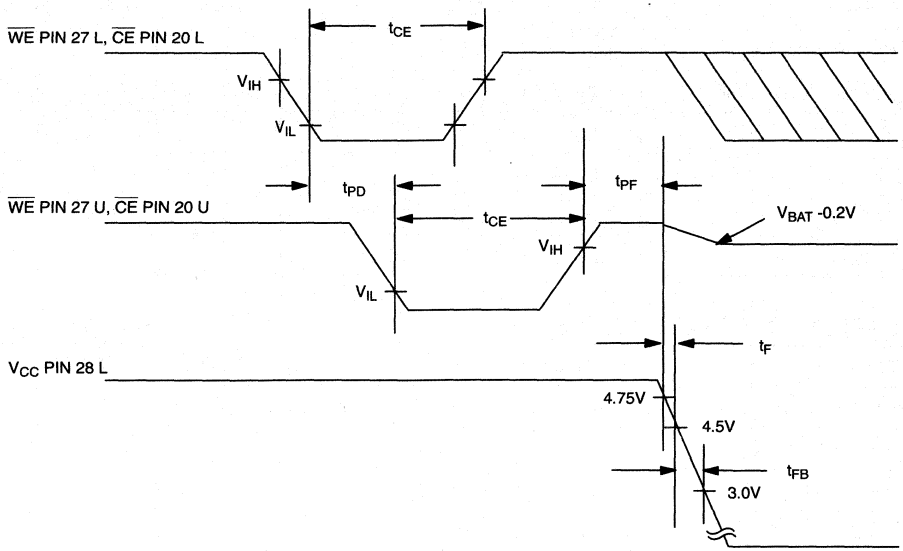
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-up	t_{REC}	25	80	125	ms	
V_{CC} Slew Rate 4.75 - 4.5V	t_F	300			µs	
V_{CC} Slew Rate 4.5 - 3V	t_{FB}	10			µs	
V_{CC} Slew Rate 4.5 - 4.75V	t_R	0			µs	
$\overline{WE}$, $\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	6

4

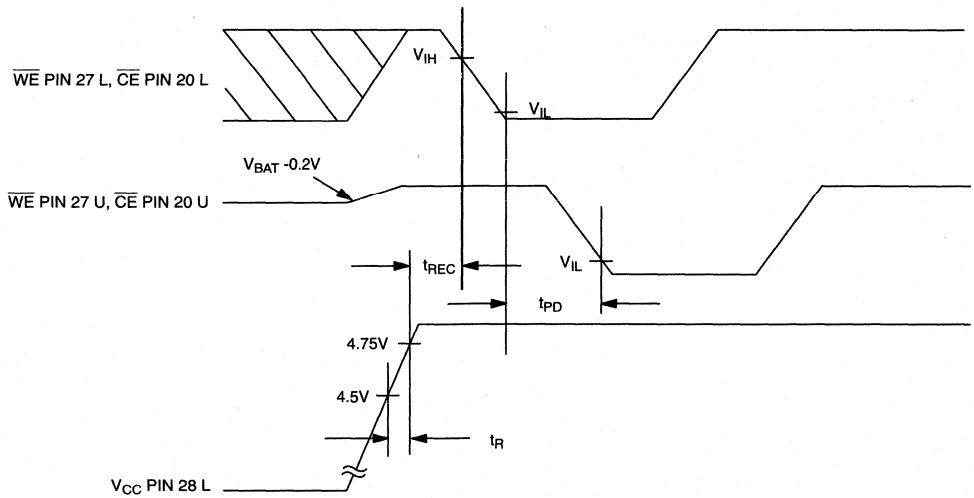
TIMING DIAGRAM: LOADING PARTITION REGISTER



TIMING DIAGRAM: POWER DOWN



TIMING DIAGRAM: POWER UP



WARNINGS:

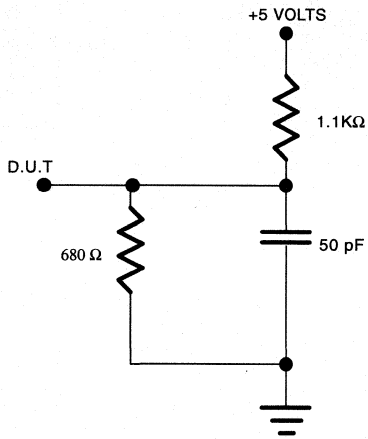
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal will discharge internal lithium source because exposed voltage pins are present.

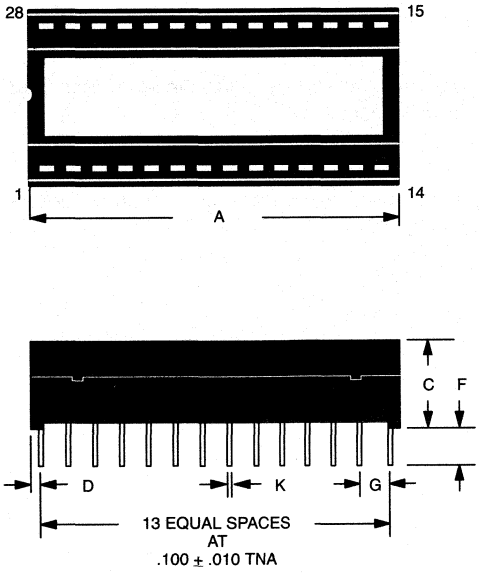
NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Pin locations are designated "U" (for upper) when a parameter definition refers to the socket receptacle and "L" (for lower) when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. I_{BAT} is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
6. t_{CE} maximum must be met to ensure data integrity on power loss.
7. V_{CC} is within nominal limits and a memory is installed in the socket.
8. Input pulse rise and fall times equal 10 ns.

OUTPUT LOAD Figure 1



DS1613C INTELLIGENT SOCKET 28 PIN (600 MIL DIP)



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.380	1.420
MM	35.05	36.07
B IN.	0.690	0.720
MM	17.53	18.29
C IN.	0.370	0.420
MM	9.39	10.67
D IN.	0.035	0.065
MM	0.89	1.65
E IN.	0.015	0.035
MM	0.39	0.89
F IN.	0.120	0.160
MM	3.04	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

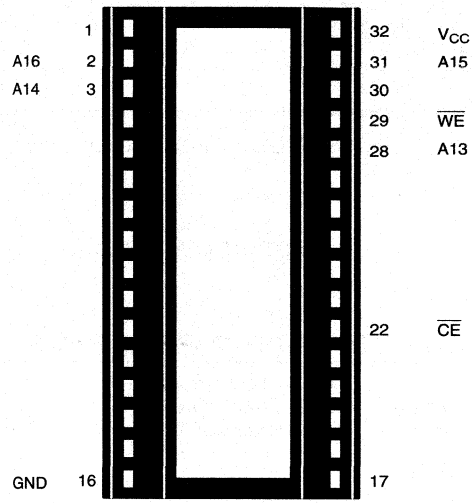
DALLAS SEMICONDUCTOR

DS1613D
Partitionable 1024K SmartSocket

FEATURES

- Accepts standard 128K x 8, CMOS static RAM
- Embedded lithium energy cell retains RAM data
- Unconditionally write protects all of memory when V_{CC} is out of tolerance
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Automatically switches to battery backup supply when power fail occurs
- Data retention time is greater than 10 years with the proper RAM selection
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



32-PIN SOCKET (600 MIL)

PIN DESCRIPTION

A13–A16	–	Address Lines
$\overline{CE}$	–	Conditioned Chip Enable
$\overline{WE}$	–	Conditioned Write Enable
V_{CC}	–	Switched V_{CC}
GND	–	Ground

All pins pass through except 22, 29, 30 and 32.

DESCRIPTION

The DS1613D SmartSocket is a 32-pin, 600 mil DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts 128K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt programs and important data.

Using the SmartSocket saves printed circuit board pacing since the SRAM/SmartSocket combination occupies no more area than the SRAM alone. The SmartSocket modifies only pins 22, 29, 30, and 32 to nonvolatize the RAM. All other pins are passed straight through. Pins 2, 3, 28, and 31 are address inputs used to program memory partitions.

The DS1613D is exactly the same as the DS1613C except that the DS1613D has 32 pins instead of 28 and the address and control signals are on different pin numbers and locations. The upper order address lines used to program the memory partitions also differ because a different RAM size is used. Tables 1 and 2 illustrate the pattern match required for partitioning of the DS1613D. See the DS1613C data sheet for all additional technical details and specifications.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A13	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A14	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A15	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A16	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

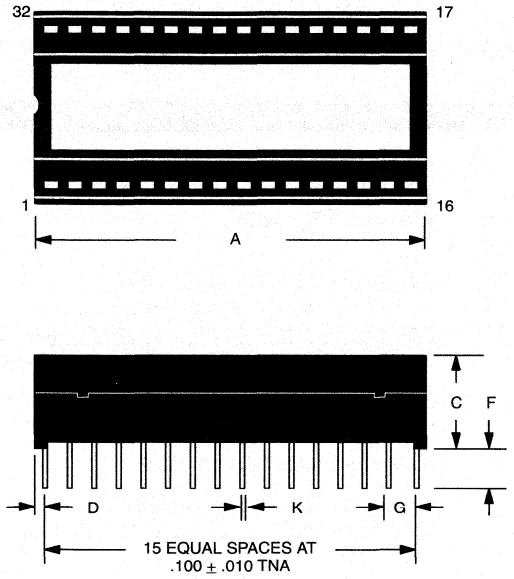
FIRST BITS ENTERED

LAST BITS ENTERED

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{16} A_{15} A_{14} A_{13})
A13	BIT 21	PARTITION 0	0000
A14	BIT 21	PARTITION 1	0001
A15	BIT 21	PARTITION 2	0010
A16	BIT 21	PARTITION 3	0011
A13	BIT 22	PARTITION 4	0100
A14	BIT 22	PARTITION 5	0101
A15	BIT 22	PARTITION 6	0110
A16	BIT 22	PARTITION 7	0111
A13	BIT 23	PARTITION 8	1000
A14	BIT 23	PARTITION 9	1001
A15	BIT 23	PARTITION 10	1010
A16	BIT 23	PARTITION 11	1011
A13	BIT 24	PARTITION 12	1100
A14	BIT 24	PARTITION 13	1101
A15	BIT 24	PARTITION 14	1110
A16	BIT 24	PARTITION 15	1111

DS1613D INTELLIGENT SOCKET 32 PIN (FOR 600 MIL DIP)



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.580 40.13	1.620 41.15
B IN. MM	0.690 17.53	0.720 18.29
C IN. MM	0.350 8.89	0.410 10.40
D IN. MM	0.035 0.89	0.065 1.65
E IN. MM	0.015 0.39	0.035 0.89
F IN. MM	0.120 3.04	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

DALLAS SEMICONDUCTOR

Application Note 4
DS1213, DS1216, DS1613 Smart Socket/Smart Watch Options

SMART SOCKET/SMART WATCH OPTIONS

The DS1213 Smart Socket, DS1613 Partitionable Smart Socket, and DS1216 Smart Watch product families are designed to accept several user modifications. Please review the DS1213, DS1613, and DS1216 data sheets for normal operation before modification.

DS1213 AND DS1613 SMART SOCKET OPTIONS

(Reference Figure 1)

Option 1: Power Supply Tolerance

The standard DS1213 and DS1613 socket products are manufactured such that power–fail detection occurs between 4.75 volts and 4.50 volts, giving a 5% supply operating range. This range can be changed to a 10% supply with power–fail detection occurring between 4.50 volts and 4.25 volts. Follow the procedure below:

- cut metal trace labeled "TOL"
- short together metal tabs labeled "T"

Option 2: Density Upgrade

This option applies to the DS1213B and DS1213D smart sockets only. The DS1213B can be upgraded from 8K x 8 to 32K x 8 memory and the DS1213D can be upgraded from 128K x 8 to 512K x 8 memory be performing the following:

- cut metal traces identified by a hash mark labeled "U"
- short together square metal pads labeled "G"

DS1216 SMART WATCH OPTIONS

(Reference Figure 2)

Option 1: RESET Disconnect

All DS1216 Smart Watch sockets are manufactured such that the RST signal to the real–time clock is located at pin 1 of the socket. If for a given application the RESET signal is not required, or not desired, this signal can be permanently disconnected as follows:

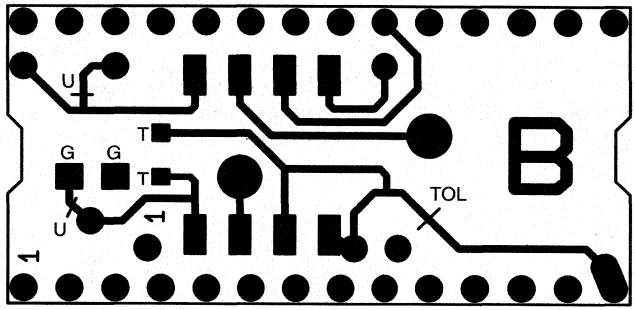
- cut metal trace labeled "RES"

Option 2: Density Upgrade

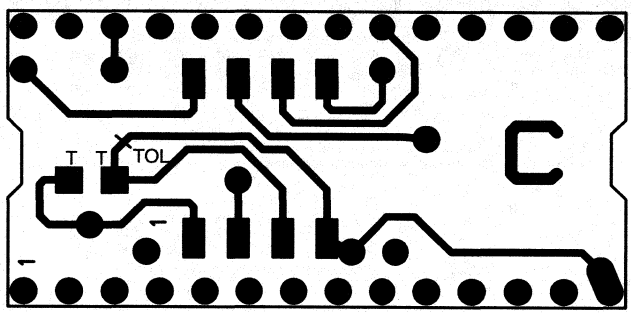
This option applies to the DS1216B and DS1216D smart watch sockets only. As with the DS1213B and DS1213D, the DS1216B and DS1216D can be upgraded from 8K x 8 to 32K x 8 memory and 128K x 8 to 512K x 8 respectively as follows:

- cut metal traces identified by a hash mark labeled "U"
- short together square metal pads labeled "G"

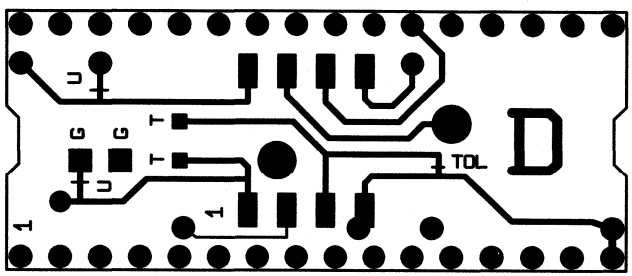
DS1213 AND DS1613 SMART SOCKET FAMILY Figure 1



DS1213B

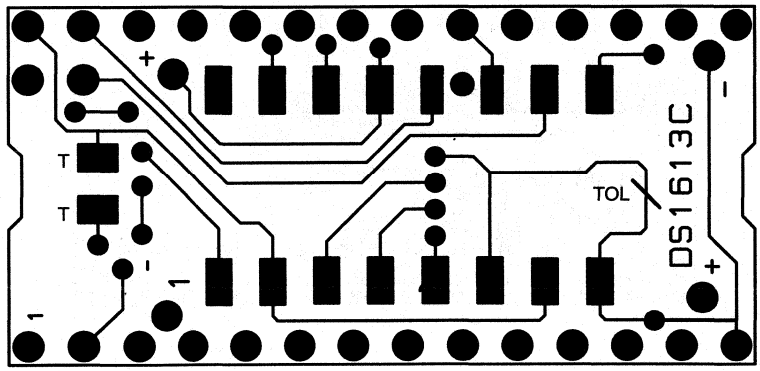


DS1213C

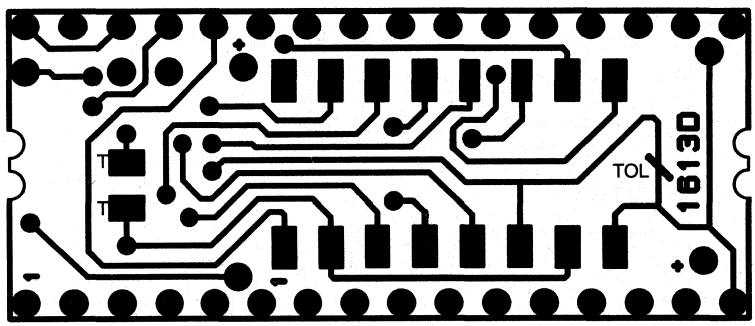


DS1213D

DS1213 AND DS1613 SMART SOCKET FAMILY Figure 1 (continued)

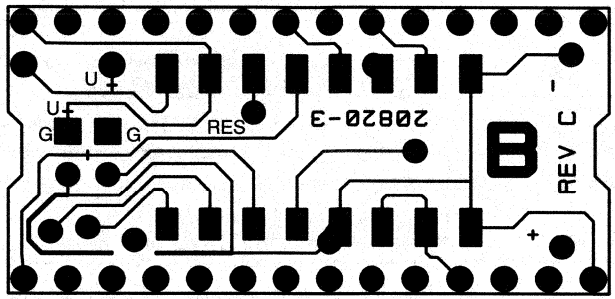


DS1613C

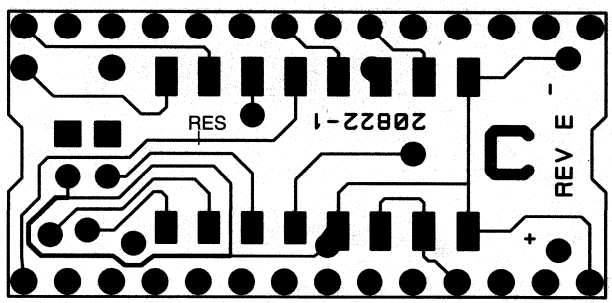


DS1613D

DS1216 SMART WATCH FAMILY Figure 2



DS1216B



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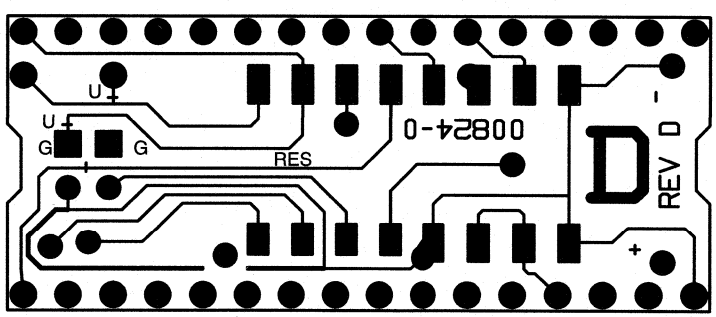
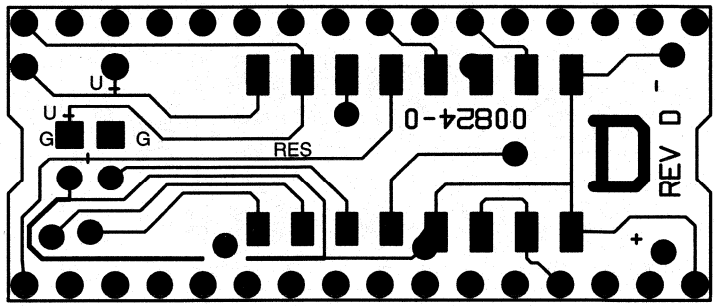


DS1216D

DS1216 SMART WATCH FAMILY Figure 2 (continued)



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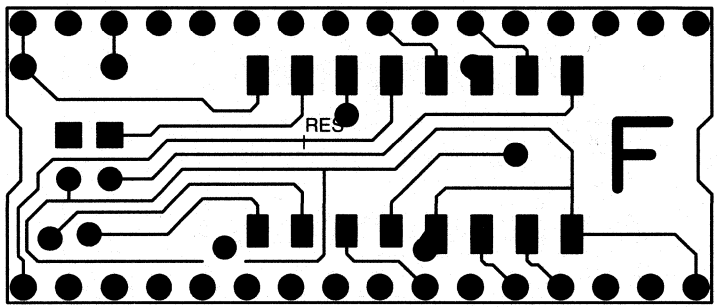


DS1216F

BATTERY BACKUP

5

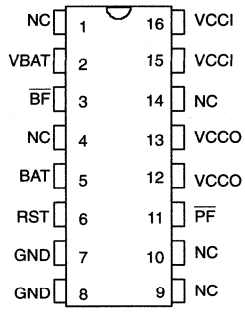
DALLAS SEMICONDUCTOR

DS1259
Battery Manager Chip

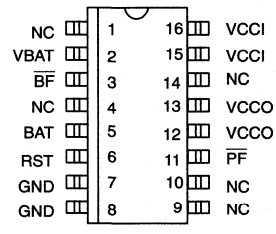
FEATURES

- Facilitates uninterruptible power
- Uses battery only when primary V_{CC} is not available
- Low forward voltage drop
- Power fail signal interrupts processor or write protects memory
- Consumes less than 100 nA of battery current
- Low battery warning signal
- Battery can be electrically disconnected upon command
- Battery will automatically reconnect when V_{CC} is applied
- Mates directly with DS1212 Nonvolatile Controller x 16 Chip to back up 16 RAMs
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



16–Pin DIP Package
(300 MIL)
See Mech. Drawings Section



16–Pin SOIC Package
(300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

NC	–	No Connection
V_{BAT}	–	Battery Input Connection
$\overline{BF}$	–	Battery Fail Output Signal
BAT	–	Battery Output
RST	–	Reset Input
GND	–	Ground
$\overline{PF}$	–	Power Fail Output Signal
V_{CCO}	–	RAM Supply
V_{CCI}	–	+5V Supply

DESCRIPTION

The DS1259 Battery Manager Chip is a low-cost battery management system for portable and nonvolatile electronic equipment. A battery connected to the battery input pin supplies power to CMOS electronic circuits when primary power is lost through an efficient switch via the V_{CCO} pins. When power is supplied from the battery, the power fail signal is active to warn electronic reset circuits of the power status. Energy loss during shipping and handling is avoided by pulsing reset, thereby causing the battery to be isolated from other elements in the circuits.

OPERATION

During normal operation, V_{CCI} (Pins 15 and 16) is the primary energy source and power is supplied to V_{CCO} (Pins 12 and 13) through an internal switch at a voltage level of V_{CCI}-0.2 volts at 250 mA. During this time the power fail signal ($\overline{PF}$) is held high, indicating valid V_{CCI} voltage (see Figure 1). However, if the V_{CCI} falls below the trip point (V_{TP}), a level of 1.26 times the battery level (V_{BAT}), the power fail signal is driven low. As V_{CCI} falls below the battery level, power is switched from V_{CCI} to V_{BAT} and the battery supplies power to the uninterruptible output (V_{CCO}) at V_{BAT}-0.2 volts at 15 mA.

On power-up, as the V_{CCI} supply rises above the battery, the primary energy source, V_{CCI}, becomes the supply. As V_{CCI} rises above the trip point (V_{TP}), the power fail signal is driven back to the high level. During normal operation, BAT (Pin 5) stays at the battery level regardless of the level of V_{CCI}.

BATTERY FAIL

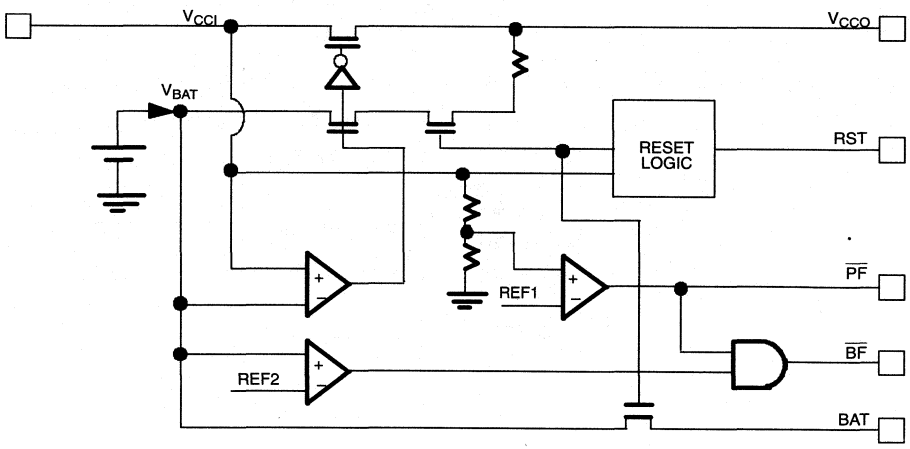
When power is being supplied from the primary energy source, $\overline{BF}$ (Pin 3) is held at a high level provided that the attached battery (V_{BAT}) is greater than 2 volts. If the battery level should decrease to below 2 volts, the $\overline{BF}$ signal is driven low, indicating a low battery. The $\overline{BF}$ signal is always low when the $\overline{PF}$ signal is low.

RESET

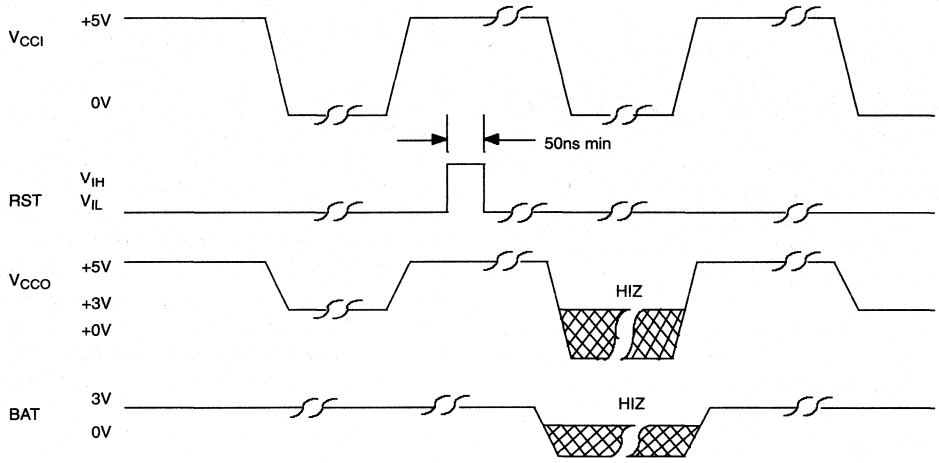
The reset input can be used to prevent the battery from supplying power to V_{CCO} and BAT even if V_{CCI} falls below the level of the battery. This feature is activated by applying a pulsed input on RST to high level for 50ns minimum while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the V_{CCO} output and BAT will go to high impedance. The next time primary power is applied such that V_{CCI} is greater than V_{BAT}, normal operation resumes and V_{CCO} will be supplied by the battery or V_{CCI}. The BAT output will also return to the level of the battery. Figure 3 shows the DS1259 in a typical application.

5

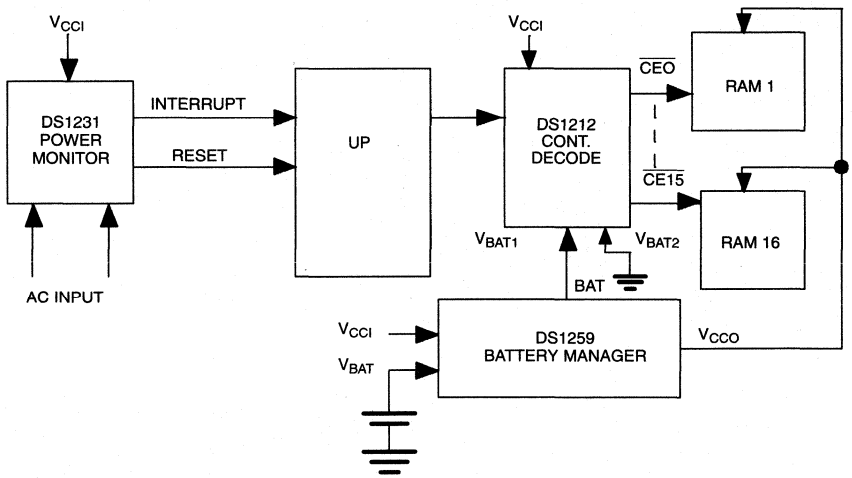
BLOCK DIAGRAM Figure 1



RESET TIMING Figure 2



TYPICAL APPLICATION Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}		5	5.5	V	1
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1
Battery Voltage Pin 2	V_{BAT}	2.5	3	3.7	V	6
Battery Output Pin 5	BAT	V_{BAT}- 0.1			V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	I_{LO}	-1.0		+250	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	1, 2
Output Current @ 0.4V	I_{OL}			+4.0	mA	1, 2
Input Supply Current	I_{CCI}			10	mA	3
Pins 12, 13 V_{CCO}=V_{CCI}-0.2	I_{CCO}			250	mA	
Pin 11 $\overline{PF}$ Detect	V_{TP}	(1.26xV_{BAT}) -250mV	(1.26xV_{BAT}) +250mV		V	4,6
Pin 3 $\overline{BF}$ Detect	V_{BATF}	1.5	2.0	2.6	V	7

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pins 12, 13 V_{CCO}=V_{BAT}-0.2V	I_{CCO2}			15	mA	5
Battery Leakage	I_{BAT}			100	nA	8
Pin 5 Battery Output Current	I_{BATOUT}			100	µA	

CAPACITANCE

(T_A = 25°C)

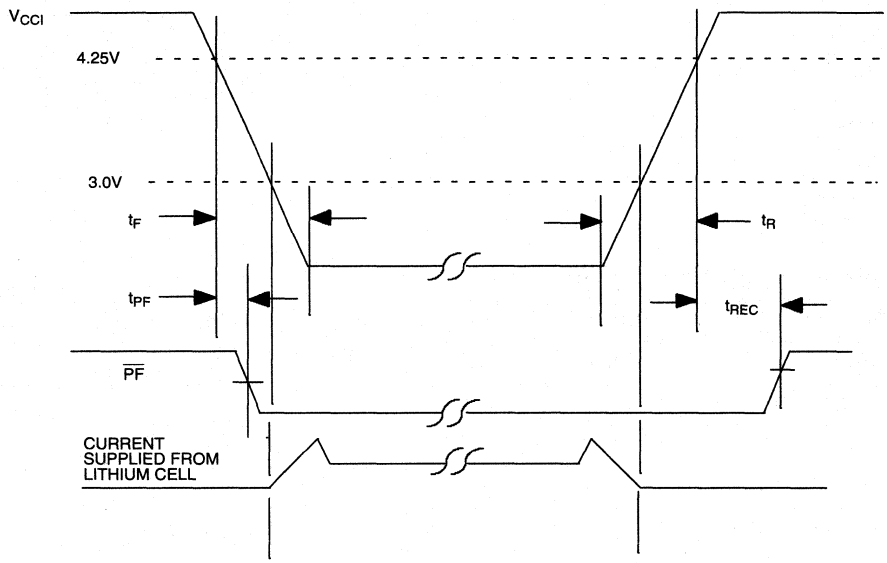
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Output Capacitance	C_{OUT}		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

($0°C$ to $70°C$; V_{CC} = 4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			µs	
V_{CCI} Slew Rate	t_R	1			µs	
Power-Down to $\overline{PF}$ Low	t_{PF}	0			µs	
$\overline{PF}$ High after Power-Up	t_{REC}			100	µs	9

POWER-DOWN/POWER-UP CONDITION



NOTES:

1. All voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13, and 3 open.
4. V_{TP} is the point that $\overline{PF}$ is driven low.
5. I_{CCO2} may be limited by the capability of the battery.
6. Trip Point Voltage for Power Fail Detect:
   $V_{TP} = 1.26 \times V_{BAT} \pm 250$ mV
   For 5% operation: V_{BAT} = 3.7V max.
   For 10% operation: V_{BAT} = 3.5 V max.
7. V_{BATF} is the point that $\overline{BF}$ is driven low. These limits are for 0°C to 70°C operation.
8. Battery leakage is the internal energy consumed by the DS1259.
9. V_{CC} = +5 volts, $t_A = 25°C$.

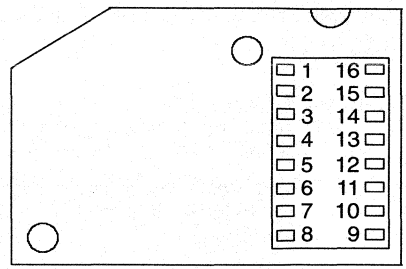
DALLAS SEMICONDUCTOR

DS1260
Smart Battery

FEATURES

- Encapsulated lithium energy cell with shelf life beyond 10 years
- Available with energy capacities of 250, 500, and 1,000 mAH @ 3 volts
- Plugs into a standard 16-pin DIP socket
- Lithium cell electrically disconnects from exposed pins upon command
- Battery isolation ensures full capacity after shipping and handling
- Lithium cell automatically reconnects when V_{CC} is applied
- Recessed pins prevent bending
- V_{CC} fail signal interrupts processor or write protects memory
- Exhausted energy cell warning signal
- Low profile permits mounting on 0.5-inch printed circuit board centers
- Mates directly with DS1212 Nonvolatile Controller to back up 16 SRAMs
- Uninterruptible supply for CMOS and portable devices

PIN ASSIGNMENT



See Mech. Drawings Section

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PIN DESCRIPTION

Pins 1, 2, 4, 7, 9, 10, and 14 are No-Connects
Pin 3 is Battery Fail ($\overline{BF}$)
Pin 5 is Battery Out (BAT)
Pin 6 is RESET (RST) Input
Pin 8 is Ground
Pin 11 is Power Fail ($\overline{PF}$)
Pins 12 and 13 are RAM Supply (V_{CCO})
Pins 15 and 16 are +5V Supply (V_{CCI})

DESCRIPTION

The DS1260 SmartBattery is a low-cost, backup energy supply for portable and nonvolatile electronic equipment. A lithium energy source of up to 1 amp hour can supply power to CMOS electronic circuits when primary power is lost through an intelligent and efficient switch. When power is supplied from the lithium power source, the power fail signal is held low to warn electronic (RESET) circuits of the power status. Energy loss during shipping and handling is avoided by pulsing RESET, thereby causing the backup energy source to be isolated from the exposed pins. The DS1260 can be plugged into a standard 16-pin, low-cost DIP socket, allowing for proven interconnect and simple replacement if the energy has been exhausted.

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OPERATION

During normal operation V_{CCI} (pins 15 and 16) is the primary energy source and power is supplied to V_{CCO} (pins 12 and 13) through an internal switch at a voltage level of V_{CCI} -0.2 volts @ 250 mA. During this time the power fail signal ($\overline{PF}$) is held high, indicating valid primary voltage (see Figure 1). However, if the V_{CCI} falls below the level of 4.25 volts, the power fail signal is driven low. As V_{CCI} falls below the level of the lithium supply (V_{BAT} = 3 volts), power is switched and the lithium energy source supplies power to the uninterruptible output (V_{CCO}) at V_{BAT} -0.2 volts @ 5 mA.

On power-up, as the V_{CCI} supply rises above 3 volts, the primary energy source, V_{CCI}, becomes the supply. As the V_{CCI} input rises above 4.25 volts, the power fail signal is driven back to the high level. During normal operation, BAT (Pin 5) stays at the battery level of 3 volts, regardless of the level of V_{CCI}.

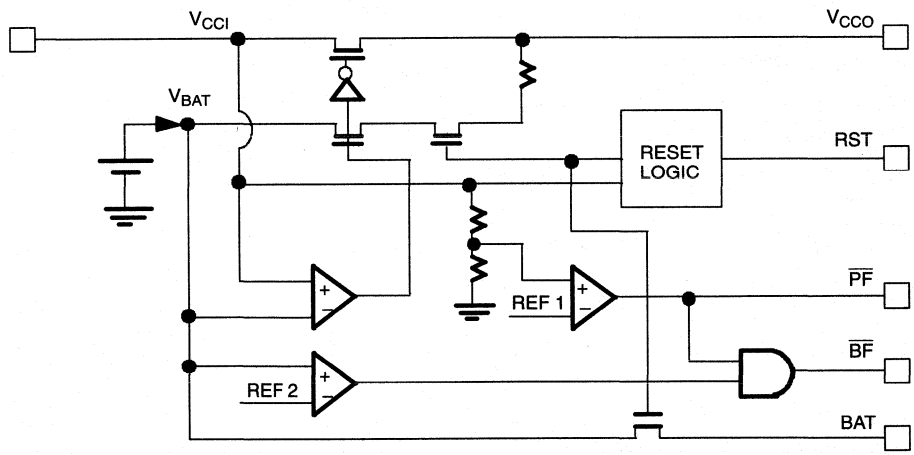
BATTERY FAIL

When power is being supplied from the primary energy source, $\overline{BF}$ (Pin 3) is held at a high level (V_{OH}) provided that the lithium energy source is greater than 2 volts. If the lithium energy source should decrease to below 2 volts, the $\overline{BF}$ signal is driven low (V_{OL}), indicating an exhausted lithium battery. The $\overline{BF}$ signal is always low when power is being supplied by the lithium energy source.

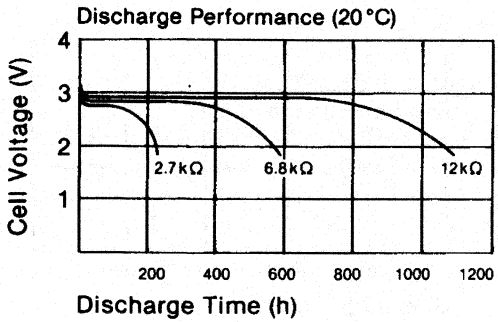
RESET

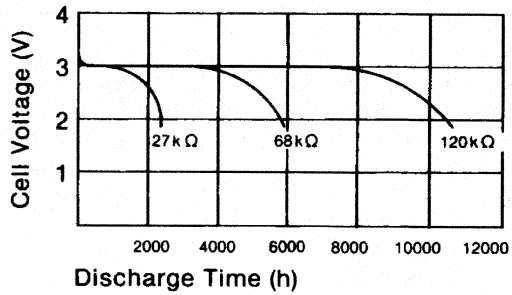
The reset input can be used to prevent the lithium energy source from supplying power to V_{CCO} and BAT even if V_{CCI} falls below 3 volts. This feature is activated by applying a pulsed input on RST to a high level (V_{IH}) for 50ns minimum while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the V_{CCO} output and BAT will go to high impedance. The next time primary power is applied such that V_{CCI} is greater than V_{BAT}, normal operation resumes and V_{CCO} will be supplied by the lithium energy source when V_{CCI} again falls below 3 volts. BAT will also return to the level V_{BAT}. Figure 3 shows how the SmartBattery is used in a system application.

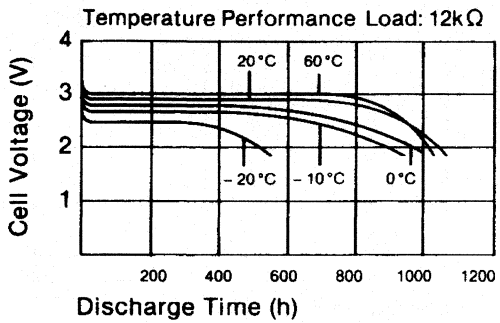
BLOCK DIAGRAM Figure 1

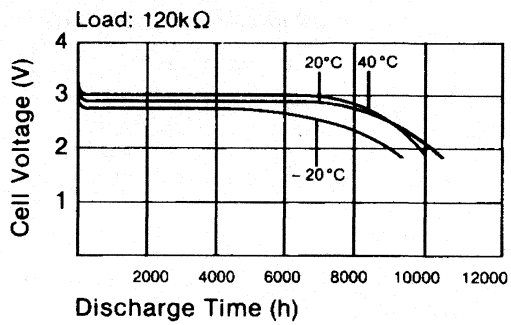


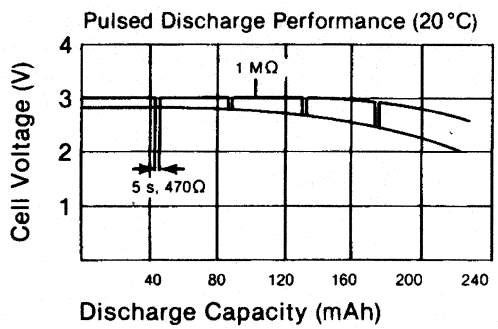
BATTERY PERFORMANCE DS1260-25



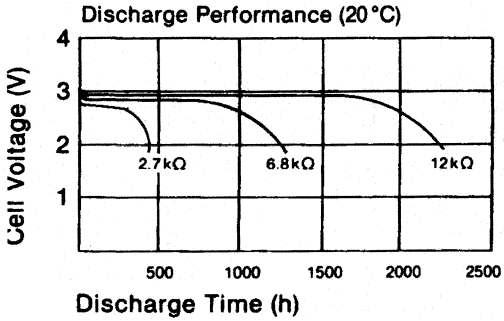


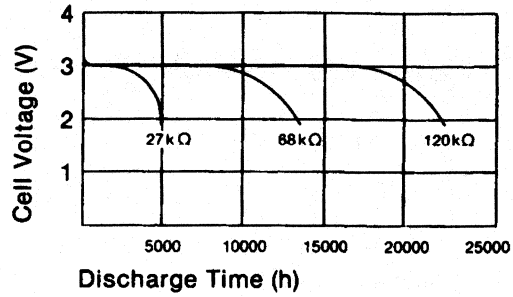


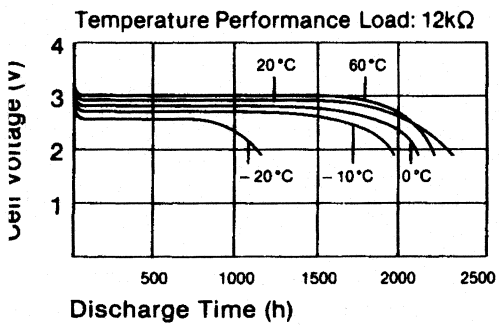


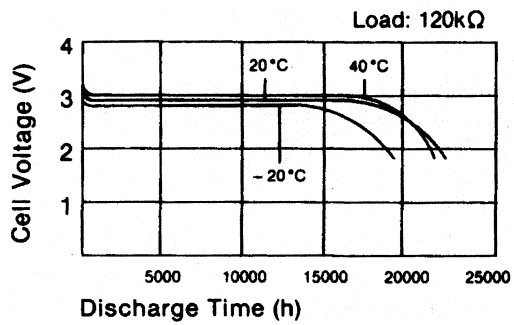


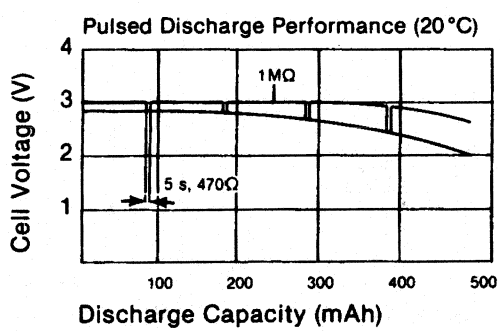
BATTERY PERFORMANCE DS1260-50



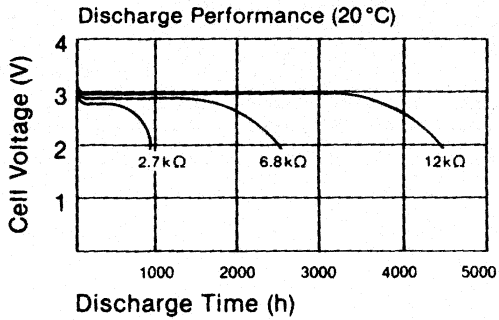


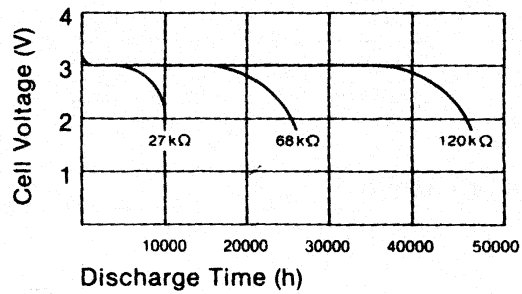


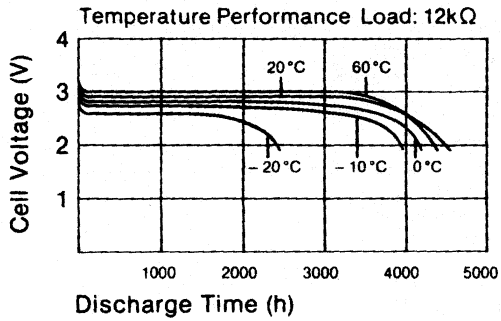


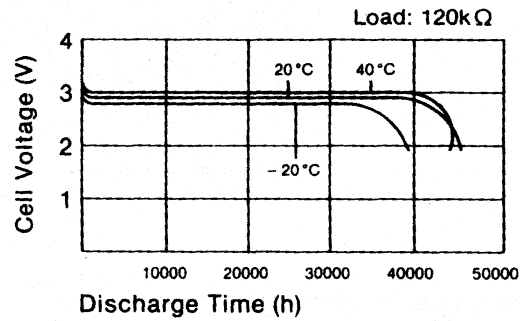


BATTERY PERFORMANCE DS1260-100









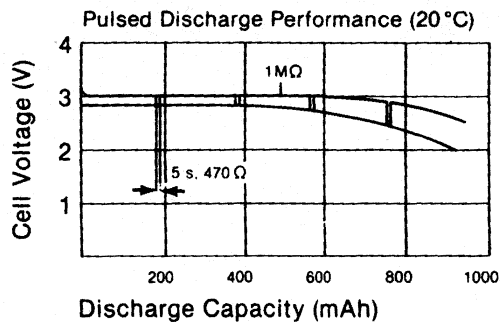
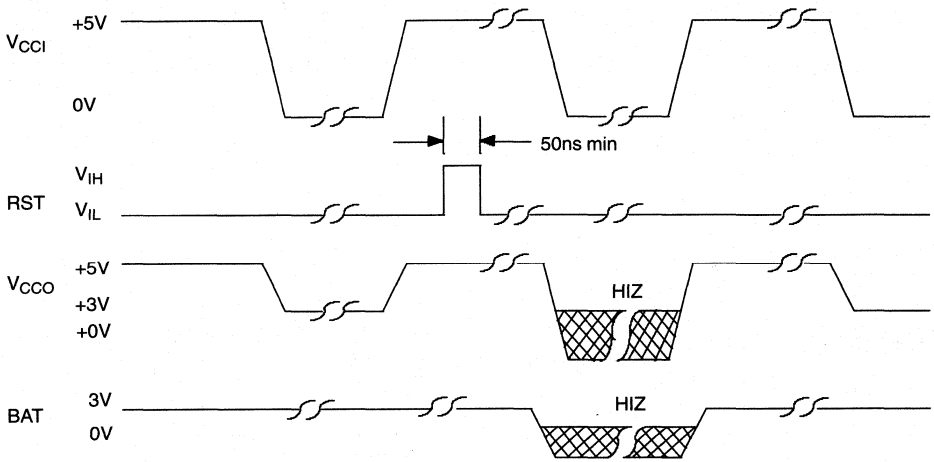


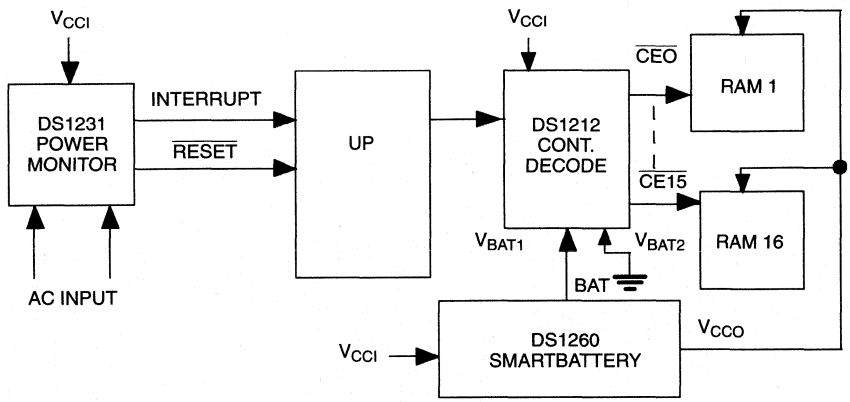
Table 1

PART NO.	CAPACITY	NOMINAL VOLTAGE
DS1260-25	250 mAH	3 volts
DS1260-50	480 mAH	3 volts
DS1260-100	960 mAH	3 volts

RESET TIMING Figure 2



INTEGRATED BATTERY BACKUP – APPLICATIONS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.0		V_{CCI}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	I_{LO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	1, 2
Output Current @ 0.4V	I_{OL}			+4.0	mA	1, 2
Input Supply Current	I_{CCI}			5	mA	3
Pins 12, 13 V_{CCO}=V_{CCI}-0.2	I_{CCO}			250	mA	
Pin 11 $\overline{PF}$ Detect	V_{TP}		4.25	4.5	V	4
Pin 3 $\overline{BF}$ Detect	V_{BATF}		2.0		V	7

(0°C to 70°C; $V_{CCI} < V_{BAT}$)

Pin 5 Battery Voltage	V_{BAT}		3		V	6
Pins 12, 13 V_{CCO}=V_{BAT}-0.2V	I_{CCO2}			15	mA	5
Battery Leakage	I_{BAT}			100	nA	8, 9
Pin 5 Battery Output Current	I_{BATOUT}			100	µA	

CAPACITANCE

(t_A = 25°C)

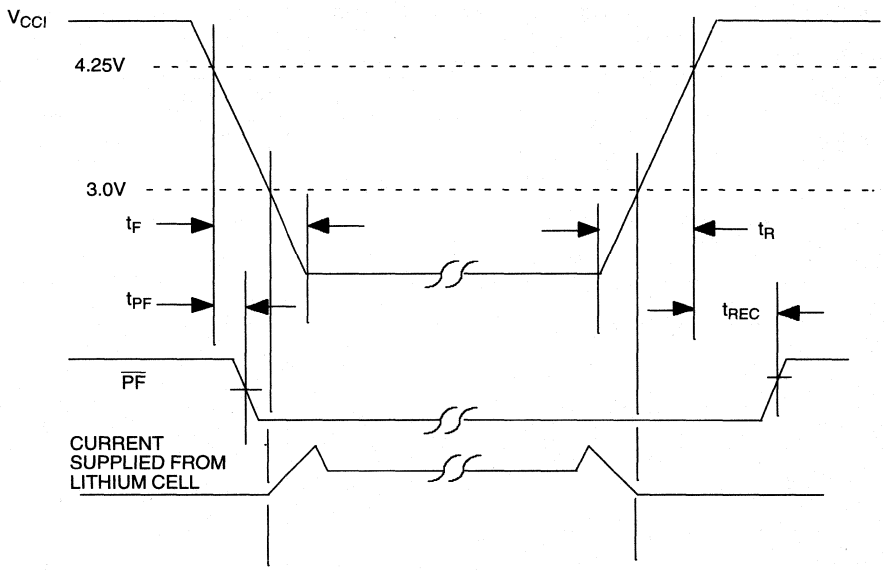
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Capacitance	C_O		5	10	pF	
Input Capacitance	C_I		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			µs	
V_{CCI} Slew Rate	t_R	1			µs	
Power-Down to $\overline{PF}$ Low	t_{PF}	0			µs	
$\overline{PF}$ High after Power-Up	t_{REC}			100	µs	

POWER-DOWN/POWER-UP CONDITION



WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.
Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

NOTES:

1. Voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13, and 3 open.
4. V_{TP} is the point that $\overline{PF}$ is driven low.
5. Sustained I_{CCO2} currents above 1 mA cause a significant drop in battery voltage.
6. V_{BAT} is the internal lithium energy source voltage.
7. V_{BATF} is the point that $\overline{BF}$ is driven low.
8. Battery leakage is the internal energy consumed by the DS1260.
9. Storage loss is less than 1% per year at 25°C.
10. V_{CCI} = +5 volts; t_A = 25°C.

DALLAS SEMICONDUCTOR

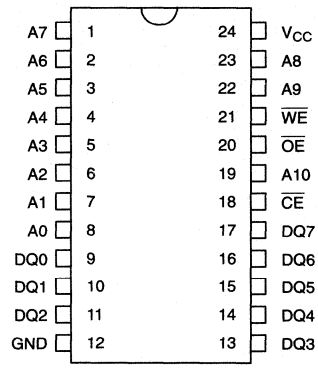
DS2016
2K x 8 3V/5V Operation Static RAM

FEATURES

- Low power CMOS design
- Standby current

  50 nA max at $t_A = 25^oC$ $V_{CC} = 3.0V$
  100 nA max at $t_A = 25^oC$ $V_{CC} = 5.5V$
  1 µA max at $t_A = 60^oC$ $V_{CC} = 5.5V$
- Full operation for V_{CC} = 5.5V to 2.7V
- Data Retention Voltage = 5.5V to 2.0V
- Access time equals 100 ns at 5.0V and 200 ns at 3.0V
- Operating temperature range of -40°C to +85°C
- Full static operation
- TTL compatible inputs and outputs over voltage range of 5.5V to 2.7 volts.
- Available in 24–pin DIP and 24–pin SOIC packages
- Suitable for both battery operate and battery backup applications

PIN ASSIGNMENT



DS2016 24–PIN DIP (600 MIL)
DS2016S 24–PIN SOIC (330 MIL)

PIN DESCRIPTION

A0 - A10	–	Address Inputs
DQ0 - DQ7	–	Data Input/Output
$\overline{CE}$	–	Chip Enable Input
$\overline{WE}$	–	Write Enable Input
$\overline{OE}$	–	Output Enable Input
V_{CC}	–	Power Supply Input 2.7V – 5.5V
GND	–	Ground

DESCRIPTION

The DS2016 is a 16384 bit low power, fully static random access memory organized as 2048 words by 8 bits using CMOS technology. The device operates from a single power supply with a voltage input between 2.7 volts and 5.5 volts. The chip enable input ($\overline{CE}$) is used for device selection and can be used in order to achieve the minimum standby current mode, which facilitates both battery operate and battery backup applications. The device provides fast access time of 100 ns when operated from a 5–volt power supply input, and also provides relatively good performance of 200 ns access while operating from a 3.0–volt input. The device maintains TTL–level inputs and outputs over the input voltage range of 2.7V to 5.5 volts. The DS2016 is most suitable for low power applications where battery operation or battery backup for nonvolatility are required. The DS2016 is a JEDEC–standard 2K x 8 SRAM and is pin-compatible with ROM and EPROM of similar density.

OPERATION MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0–A10	DQ–DQ7	POWER
READ	L	L	H	STABLE	DATA OUT	I_{CCO}
WRITE	L	X	L	STABLE	DATA IN	I_{CCO}
DESELECT	L	H	H	X	HIGH-Z	I_{CCO}
STANDBY	H	X	X	X	HIGH-Z	I_{CCS}

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING
V_{CC}	Power Supply Voltage	-0.3V to +7.0V
V_{IN}, $V_{I/O}$	Input, Input/Output Voltage	-0.3 to V_{CC} + 0.3V
T_{STG}	Storage Temperature	-55°C to +125°C
T_{OPR}	Operating Temperature	-40°C to +85°C
T_{SOLDER}	Soldering Temperature/Time	260°C for 10 seconds

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

6

+5 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS

(t_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Data Retention Voltage	V_{DR}	2.0		5.5	V	

DC CHARACTERISTICS

(t_A = -40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$			±0.1	µA
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$			±0.5	µA
Output High Current	I_{OH}	V_{OH} = 2.4V	-1.0			mA
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0			mA
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.0V			0.3	mA
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.5V t_A=60°C			1	µA
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.5V t_A=25°C			100	nA
Operating Current	I_{CCO}	$\overline{CE}$=0.8V, 200 ns cycle			55	mA

AC CHARACTERISTICS READ CYCLE

(t_A = -40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	100			ns	
Access Time	t_{ACC}			100	ns	
$\overline{OE}$ to Output Valid	t_{OE}			50	ns	
$\overline{CE}$ to Output Valid	t_{CO}			100	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5			ns	
Output High-Z from Deselection	t_{OD}	5		35	ns	
Output Hold from Address Change	t_{OH}	5			ns	

AC CHARACTERISTICS WRITE CYCLE

(t_A = -40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	100			ns	
Write Pulse Width	t_{WP}	75			ns	
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	10			ns	
Output High-Z from $\overline{WE}$	t_{ODW}			35	ns	
Output Active from $\overline{WE}$	t_{OEW}	5			ns	
Data Setup Time	t_{DS}	40			ns	
Data Hold Time	t_{DH}	0			ns	

DATA RETENTION CHARACTERISTICS

(t_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Supply Voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.5V$	2.0		5.5	V
Data Retention Current at 5.5V	I_{CCR1}	$\overline{CE} \geq V_{CC} - 0.5V$		0.1*	1	µA
Data Retention Current at 2.0V	I_{CCR2}	$\overline{CE} \geq V_{CC} - 0.5V$		50*	750	nA
Chip Deselect to Data Retention	t_{CDR}		0			µs
Recovery Time	t_R		2			ms

* Typical values are at 25°C

6

+3 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS

(t_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.7	3.0	3.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.6	V	
Data Retention Voltage	V_{DR}	2.0		3.5	V	

DC CHARACTERISTICS

(t_A = -40°C to +85°C; V_{CC} = 2.7V to 3.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$			±0.1	µA
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$			±0.5	µA
Output High Current	I_{OH}	V_{OH} = 2.2V	-0.5			mA
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0			mA
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.0V			0.1	mA
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=60°C			500	nA
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=25°C			50	nA
Operating Current	I_{CCO}	$\overline{CE}$=0.6V min cycle			25	mA

AC CHARACTERISTICS READ CYCLE

(t_A = -40°C to +85°C; V_{CC} = 2.7V to 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	200			ns	
Access Time	t_{ACC}			200	ns	
$\overline{OE}$ to Output Valid	t_{OE}			100	ns	
$\overline{CE}$ to Output Valid	t_{CO}			200	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5			ns	
Output High-Z from Deselection	t_{OD}	5		80	ns	
Output Hold from Address Change	t_{OH}	5			ns	

AC CHARACTERISTICS WRITE CYCLE

(t_A = -40°C to +85°C; V_{CC} = 2.7V to 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	200			ns	
Write Pulse Width	t_{WP}	150			ns	
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High-Z from $\overline{WE}$	t_{ODW}			75	ns	
Output Active from $\overline{WE}$	t_{OEW}	5			ns	
Data Setup Time	t_{DS}	80			ns	
Data Hold Time	t_{DH}	0			ns	

DATA RETENTION CHARACTERISTICS

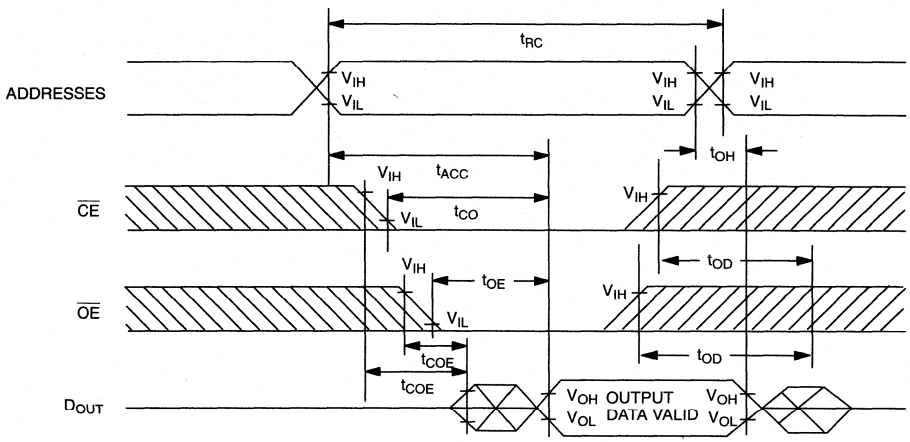
(t_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Supply Voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.3V$	2.0		3.5	V
Data Retention Current at 3.5V	I_{CCR1}	$\overline{CE} \geq V_{CC} - 0.3V$		50*	1000	nA
Data Retention Current at 2.0V	I_{CCR2}	$\overline{CE} \geq V_{CC} - 0.3V$		50*	750	nA
Chip Deselect to Data Retention	t_{CDR}		0			µs
Recovery Time	t_R		2			ms

* Typical values are at 25°C

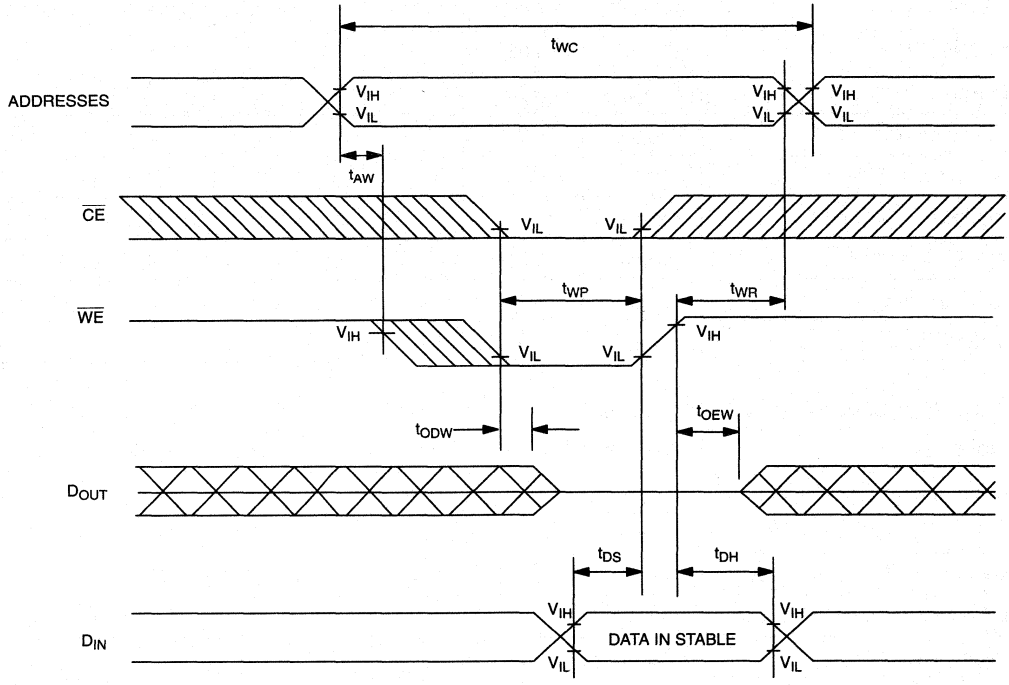
6

TIMING DIAGRAM: READ CYCLE



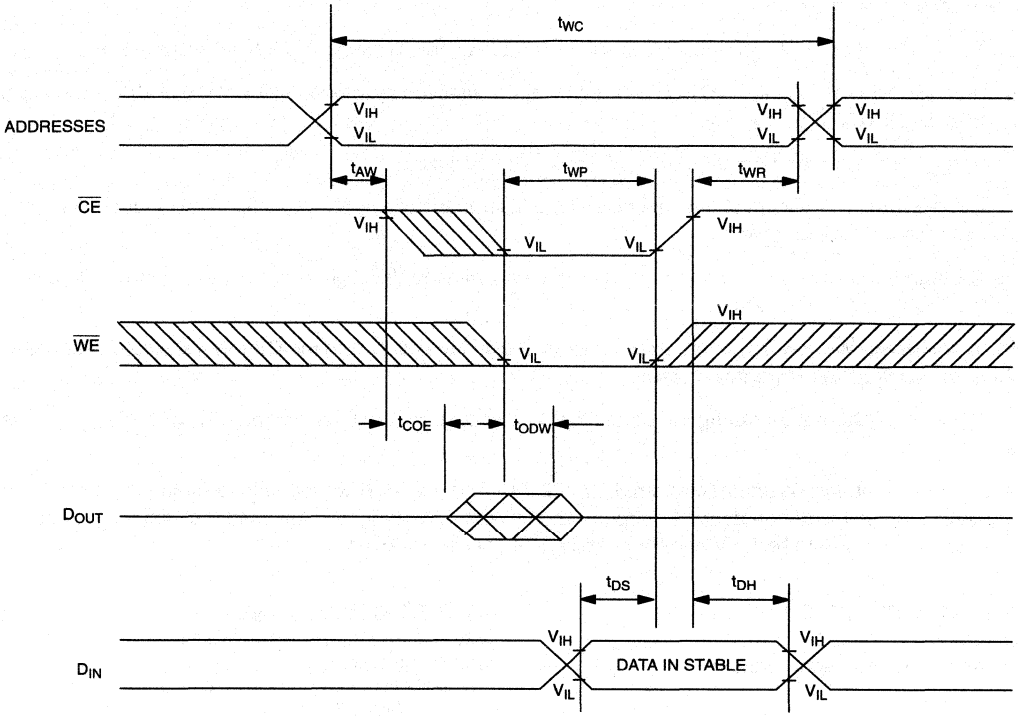
SEE NOTE 1

TIMING DIAGRAM: WRITE CYCLE 1



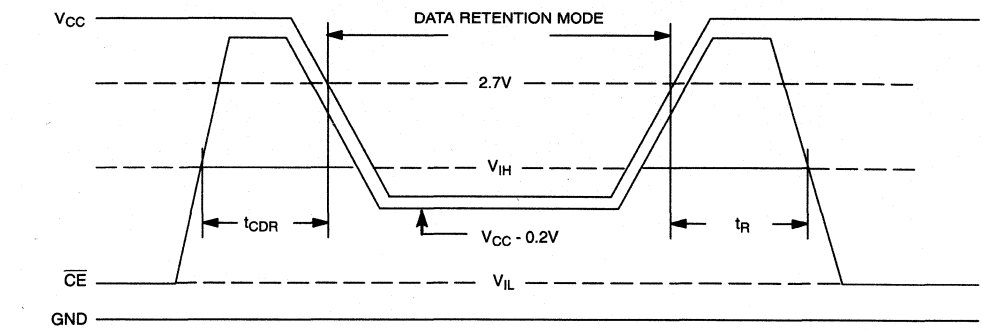
SEE NOTES 2, 3, 4, 5, 6 AND 7

TIMING DIAGRAM: WRITE CYCLE 2



SEE NOTES 2, 3, 4, 5, 6 AND 7

TIMING DIAGRAM: DATA RETENTION - POWER UP, POWER DOWN Figure 1



SEE NOTE 8

NOTES:

1. $\overline{WE}$ is high for read cycles.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH} and t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
6. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state.
7. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state.
8. If the V_{IH} level of $\overline{CE}$ is 2.0V during the period that V_{CC} voltage is going down from 4.5V to 2.7V, I_{CCS1} current flows.
9. The DS2016 maintains full operation from 5.5V to 2.7V. The electrical characteristics tables show two tested and guaranteed points of operation. For operation between 4.5V and 3.5 volts, used the composite worst case characteristics from both 5V and 3V operation for design purposes.

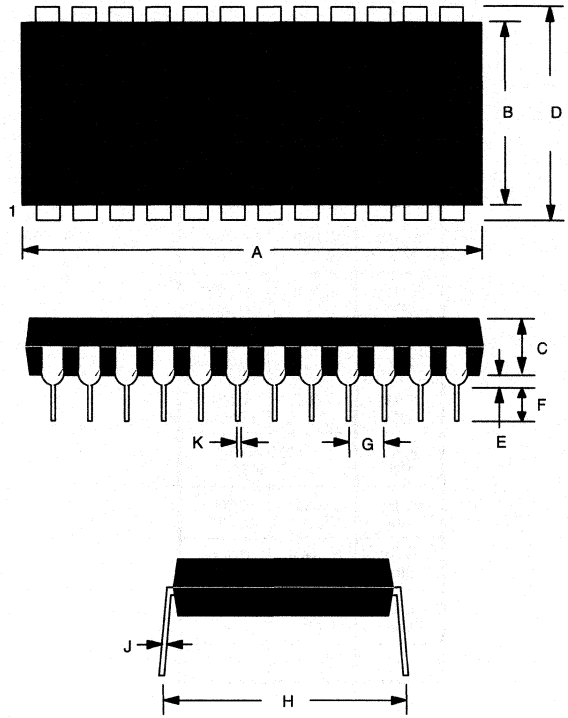
DC TEST CONDITIONS

Outputs Open
All voltages are referenced to ground.

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0V - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

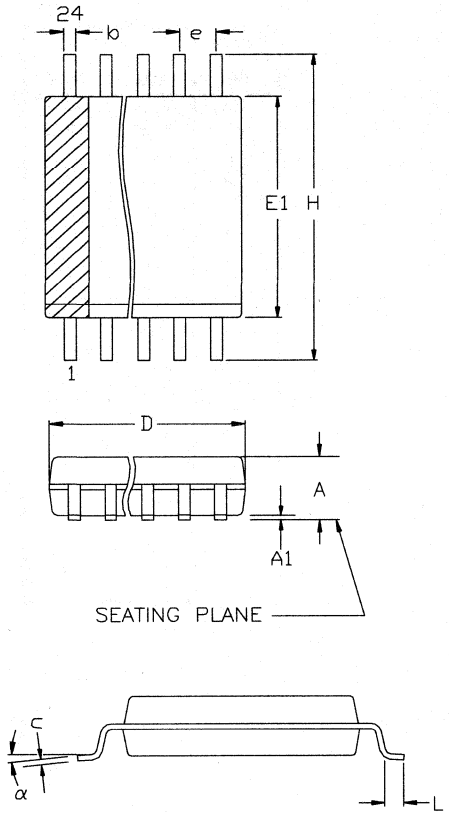
DS2016 24–PIN DIP



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.245	1.270
MM	31.62	32.25
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.050
MM	0.380	1.27
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

6

DS2016S 24–PIN SOIC



PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	0.080 2.04	0.120 3.05
A1 IN. MM	0.002 0.05	0.014 0.35
b IN. MM	0.012 0.30	0.020 0.50
C IN MM	0.004 0.10	0.0125 0.32
D IN. MM	0.595 15.1	0.634 16.1
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN. MM	0.324 8.23	0.350 8.90
H IN MM	0.453 11.5	0.500 12.7
L IN MM	0.016 0.40	0.051 1.30
α	0°	10°

The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

DALLAS SEMICONDUCTOR

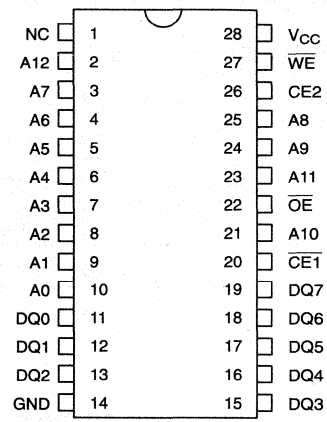
DS2064
8K x 8 3V/5V Operation Static RAM

FEATURES

- Low power CMOS design
- Standby current

  50 nA max at $t_A = 25^oC$ $V_{CC} = 3.0V$
  100 nA max at $t_A = 25^oC$ $V_{CC} = 5.5V$
  1 µA max at $t_A = 60^oC$ $V_{CC} = 5.5V$
- Full operation for V_{CC} = 5.5V to 2.7V
- Data Retention Voltage = 5.5V to 2.0V
- Access time equals 200 ns at 5.0V and 300 ns at 3.0V
- Operating temperature range of -40°C to +85°C
- Full static operation
- TTL compatible inputs and outputs over voltage range of 5.5V to 2.7 volts.
- Available in 28–pin DIP and 28–pin SOIC packages
- Suitable for both battery operated and battery backup applications

PIN ASSIGNMENT



DS2064–200 28–PIN DIP (600 MIL)
DS2064S–200 28–PIN SOIC (330 MIL)

PIN DESCRIPTION

A0 - A12	–	Address Inputs
DQ0 - DQ7	–	Data Input/Output
$\overline{CE1}$, CE2	–	Chip Enable Inputs
$\overline{WE}$	–	Write Enable Input
$\overline{OE}$	–	Output Enable Input
V_{CC}	–	Power Supply Input 2.7V - 5.5V
GND	–	Ground
NC	–	No Connection

DESCRIPTION

The DS2064 is a 65536 bit low power, fully static random access memory organized as 8192 words by 8 bits using CMOS technology. The device operates from a single power supply with a voltage input between 2.7 volts and 5.5 volts. The chip enable inputs ($\overline{CE1}$ and CE2) are used for device selection and can be used in order to achieve the minimum standby current mode, which facilitates both battery operate and battery backup applications. The device provides fast access time of 200 ns when operated from a 5–volt power supply input, and also provides relatively good performance of 300 ns access while operating from a 3.0–volt input. The device maintains TTL–level inputs and outputs over the input voltage range of 2.7V to 5.5 volts. The DS2064 is most suitable for low power applications where battery operation or battery backup for nonvolatility are required. The DS2064 is a JEDEC–standard 8K x 8 SRAM and is pin–compatible with ROM and EPROM of similar density.

OPERATION MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	A0 - A12	DQ - DQ7	POWER
READ	L	H	L	H	STABLE	DATA OUT	I_{CCO}
WRITE	L	H	X	L	STABLE	DATA IN	I_{CCO}
DESELECT	L	H	H	H	X	HIGH-Z	I_{CCO}
STANDBY	H	X	X	X	X	HIGH-Z	I_{CCS}
STANDBY	X	L	X	X	X	HIGH-Z	I_{CCS}

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING
V_{CC}	Power Supply Voltage	-0.3V to +7.0V
V_{IN}, $V_{I/O}$	Input, Input/Output Voltage	-0.3 to V_{CC} + 0.3V
T_{STG}	Storage Temperature	-55°C to +125°C
T_{OPR}	Operating Temperature	-40°C to +85°C
T_{SOLDER}	Soldering Temperature/Time	260°C for 10 seconds

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

+5 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS

(t_A = –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Data Retention Voltage	V_{DR}	2.0		5.5	V	

DC CHARACTERISTICS

(t_A = –40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$			±0.1	µA
I/O Leakage Current	I_{LO}	$\overline{CE1}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$			±0.5	µA
Output High Current	I_{OH}	V_{OH} = 2.4V	-1.0			mA
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0			mA
Standby Current	I_{CCS1}	$\overline{CE1}$ = 2.0V			0.3	mA
Standby Current	I_{CCS2}	$\overline{CE1} \ge V_{CC}$-0.5V t_A=60°C			1	µA
Standby Current	I_{CCS2}	$\overline{CE1} \ge V_{CC}$-0.5V t_A=25°C			100	nA
Operating Current	I_{CCO}	$\overline{CE1}$=0.8V, 200 ns cycle			55	mA

AC CHARACTERISTICS READ CYCLE

(t_A = –40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	200			ns	
Access Time	t_{ACC}			200	ns	
$\overline{OE}$ to Output Valid	t_{OE}			100	ns	
$\overline{CE}$ to Output Valid	t_{CO}			200	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5			ns	
Output to High–Z from Deselection	t_{OD}	10		60	ns	
Output Hold from Address Change	t_{OH}	5			ns	

6

AC CHARACTERISTICS WRITE CYCLE

(t_A = –40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	200			ns	
Write Pulse Width	t_{WP}	150			ns	
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	10			ns	
Output High–Z from $\overline{WE}$	t_{ODW}			70	ns	7
Output Active from $\overline{WE}$	t_{OEW}	5			ns	7
Data Setup Time	t_{DS}	80			ns	
Data Hold Time	t_{DH}	0			ns	

DATA RETENTION CHARACTERISTICS

(t_A=–40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Supply Voltage	V_{DR}	$\overline{CE1} \geq V_{CC} - 0.5V$	2.0		5.5	V
Data Retention Current at 5.5V	I_{CCR1}	$\overline{CE1} \geq V_{CC} - 5.0V$		0.1*	1	µA
Data Retention Current at 2.0V	I_{CCR2}	$\overline{CE1} \geq V_{CC} - 5.0V$		50*	750	nA
Chip Deselect to Data Retention	t_{CDR}		0			µs
Recovery Time	t_R		2			ms

* Typical values are at 25°C

+3 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS

(t_A = –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.7	3.0	3.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	–0.3		0.6	V	
Data Retention Voltage	V_{DR}	2.0		3.5	V	

DC CHARACTERISTICS

(t_A = –40°C to +85°C;V_{CC}=2.7V to 3.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	0V ≤ V_{IN} ≤ V_{CC}			±0.1	µA
I/O Leakage Current	I_{LO}	$\overline{CE1}$=V_{IH} 0V≤V_{IO}≤V_{CC}			±0.5	µA
Output High Current	I_{OH}	V_{OH} = 2.2V	-0.5			mA
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0			mA
Standby Current	I_{CCS1}	$\overline{CE1}$ = 2.0V			0.1	mA
Standby Current	I_{CCS2}	$\overline{CE1}$≥V_{CC}-0.3V t_A=60°C			500	nA
Standby Current	I_{CCS2}	$\overline{CE1}$≥V_{CC}-0.3V t_A=25°C			50	nA
Operating Current	I_{CCO}	$\overline{CE1}$=0.6V min cycle			25	mA

AC CHARACTERISTICS READ CYCLE

(t_A=–40°C to +85°C; V_{CC}=2.7V to 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	300			ns	
Access Time	t_{ACC}			300	ns	
$\overline{OE}$ to Output Valid	t_{OE}			150	ns	
$\overline{CE}$ to Output Valid	t_{CO}			300	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5			ns	
Output High–Z from Deselection	t_{OD}	5		120	ns	
Output Hold from Address Change	t_{OH}	15			ns	

6

AC CHARACTERISTICS WRITE CYCLE

(t_A = –40°C to +85°C; V_{CC}=2.7V to 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	300			ns	
Write Pulse Width	t_{WP}	225			ns	
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	25			ns	
Output High–Z from $\overline{WE}$	t_{ODW}			100	ns	7
Output Active from $\overline{WE}$	t_{OEW}	5			ns	7
Data Setup Time	t_{DS}	150			ns	
Data Hold Time	t_{DH}	0			ns	

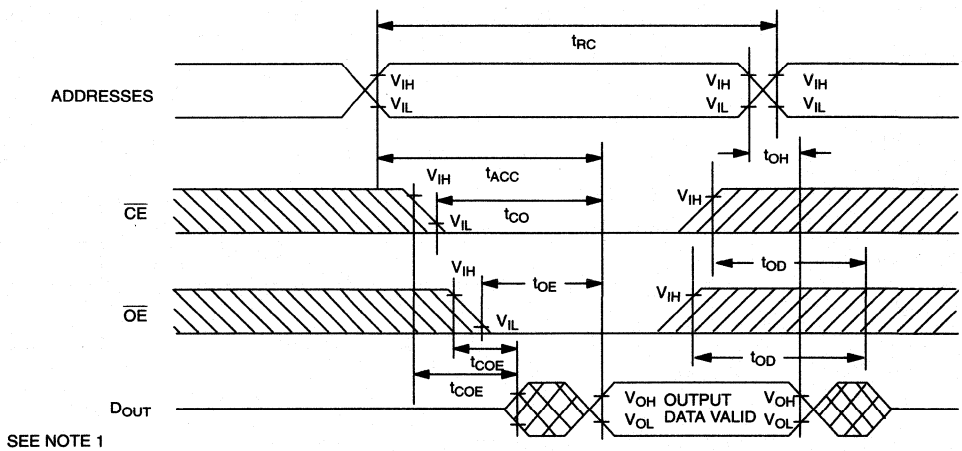
DATA RETENTION CHARACTERISTICS

(t_A = –40°C to +85°C)

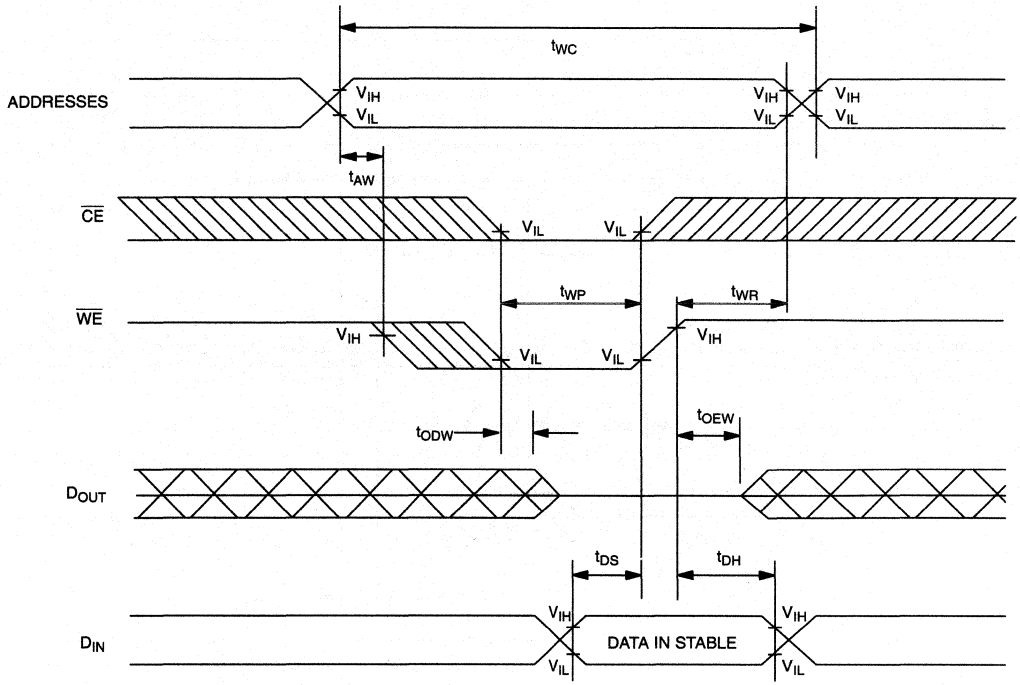
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Supply Voltage	V_{DR}	$\overline{CE1} \geq V_{CC} - 0.3V$	2.0		3.5	V
Data Retention Current at 3.5V	I_{CCR1}	$\overline{CE1} \geq V_{CC} - 0.3V$		50*	1000	nA
Data Retention Current at 2.0V	I_{CCR2}	$\overline{CE1} \geq V_{CC} - 0.3V$		50*	750	nA
Chip Deselect to Data Retention	t_{CDR}		0			µs
Recovery Time	t_R		2			ms

* Typical values are at 25°C

TIMING DIAGRAM: READ CYCLE



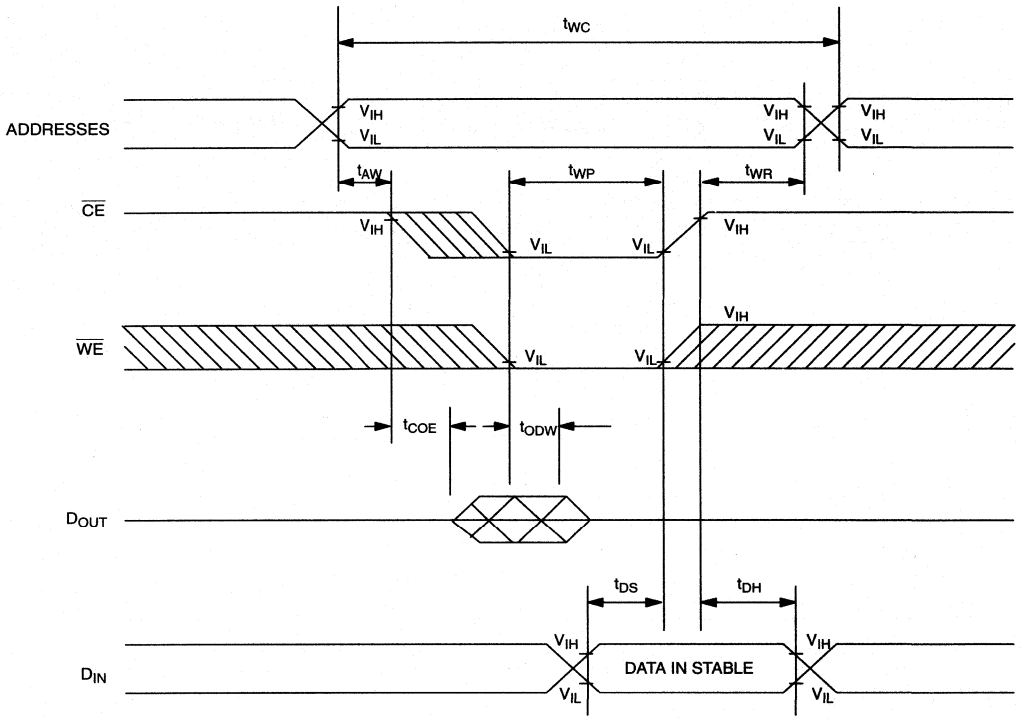
TIMING DIAGRAM: WRITE CYCLE 1



SEE NOTES 2, 3, 4, 5, 6 AND 7

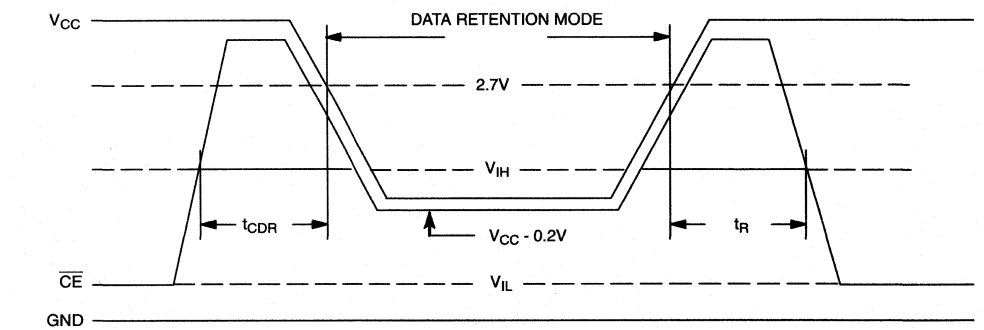
6

TIMING DIAGRAM: WRITE CYCLE 2



SEE NOTES 2, 3, 4, 5, 6 AND 7

TIMING DIAGRAM: DATA RETENTION - POWER UP, POWER DOWN



SEE NOTE 8

NOTES:

1. WE is high for read cycles.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH} and t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
6. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state.
7. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state.
8. If the V_{IH} level of $\overline{CE}$ is 2.0V during the period that V_{CC} voltage is going down from 4.5V to 2.7V, I_{CCS1} current flows.
9. The DS2064 maintains full operation from 5.5V to 2.7V. The electrical characteristics tables show two tested and guaranteed points of operation. For operation between 4.5V and 3.5 volts, used the composit worst case characteristics from both 5V and 3V operation for deisgn purposes.

DC TEST CONDITIONS

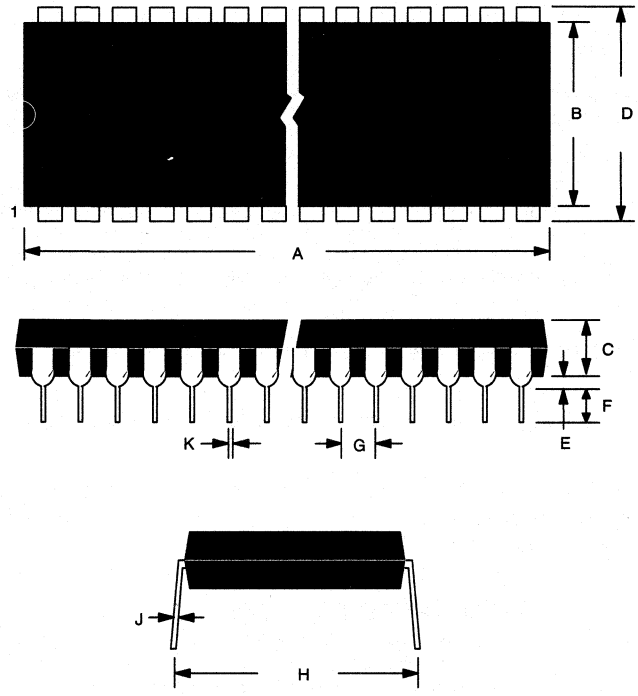
Outputs Open
All voltages are referenced to ground.

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0V - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

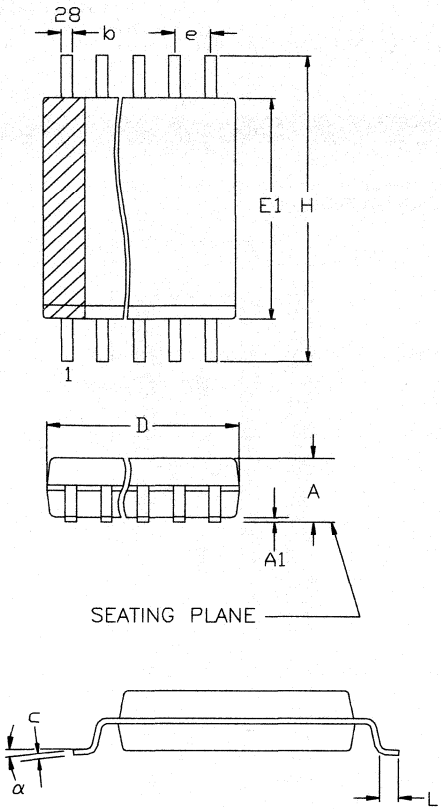
6

DS2064 28–PIN DIP



PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.440	1.460
MM	30.99	32.00
B IN.	0.540	0.560
MM	13.72	14.22
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.590	0.625
MM	14.99	15.88
E IN.	0.015	0.040
MM	0.380	1.02
F IN.	0.110	0.135
MM	2.79	3.43
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS2064S 28-PIN SOIC



PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	0.080 2.04	0.120 3.05
A1 IN. MM	0.002 0.05	0.014 0.35
b IN. MM	0.012 0.30	0.020 0.50
C IN MM	0.004 0.10	0.0125 0.32
D IN. MM	0.697 17.70	0.728 18.50
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN. MM	0.324 8.23	0.350 8.90
H IN MM	0.453 11.5	0.500 12.7
L IN MM	0.016 0.40	0.051 1.30
α	0°	10°

The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

6

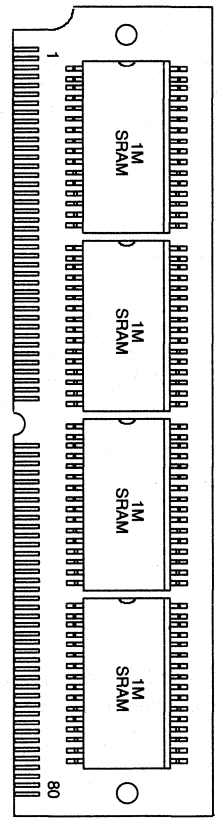
DALLAS SEMICONDUCTOR

DS2229
Word-Wide 8 Meg SRAM Stik

FEATURES

- Organized as a high density 512K x 16 bit Stik™
- Fast access time of 85 ns
- Unlimited write cycles
- Employs popular JEDEC standard 80-position SIMM connector
- Full ±10% operating range
- Read cycle time equals write cycle time
- Ultra-low standby current < 10 µA
- Suitable for battery-backed applications

PIN ASSIGNMENT



80-pin SIP Stik

DESCRIPTION

The DS2229 is a 8,388,608-bit low-power fully static Random Access Memory organized as a 524,888 word by 16 bits using CMOS technology. The device employs the popular JEDEC standard 80-pin SIMM connection scheme with no additional circuitry required. The device operates from a single power supply with a voltage input of 4.5 to 5.5 volts. The Chip Enable inputs ($\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$) are used for device selection and can be used in order to achieve the minimum standby current mode which facilitates battery backup. The device provides a fast access time of 85 ns. The DS2229 maintains TTL levels over input voltage range 4.5V to 5.5V. The DS2229 is JEDEC pin compatible (see Figure 1) with flash EEPROM memory SIMM boards of similar density.

PIN DESCRIPTION Figure 1

PIN #	PIN NAME	PIN #	PIN NAME	PIN #	PIN NAME
1	GND	32	NC	63	DQ_7
2	V_{CC}	33	NC	64	DQ_6
3	NC	34	NC	65	DQ_5
4	$\overline{OE}$	35	NC	66	DQ_4
5	$\overline{WEH}$	36	A_{16}	67	DQ_3
6	$\overline{WEL}$	37	A_{15}	68	DQ_2
7	NC	38	A_{14}	69	DQ_1
8	CS	39	A_{13}	70	DQ_0
9	NC	40	A_{12}	71	NC
10	NC	41	A_{11}	72	V_{CC}
11	NC	42	A_{10}	73	NC
12	NC	43	A_9	74	GND
13	NC	44	A_8	75	NC
14	NC	45	A_7	76	GND
15	NC	46	A_6	77	GND
16	NC	47	A_5	78	NC
17	NC	48	A_4	79	NC
18	NC	49	A_3	80	GND
19	NC	50	A_2		
20	NC	51	A_1		
21	$\overline{CE3}$	52	A_0		
22	$\overline{CE2}$	53	GND		
23	$\overline{CE1}$	54	GND		
24	$\overline{CE0}$	55	DQ_{15}		
25	GND	56	DQ_{14}		
26	NC	57	DQ_{13}		
27	NC	58	DQ_{12}		
28	NC	59	DQ_{11}		
29	NC	60	DQ_{10}		
30	NC	61	DQ_9		
31	NC	62	DQ_8		

PIN NAME	DESCRIPTION
$A_0 - A_{16}$	Address Input
$\overline{WEL}$	Write Enable Input Low
$\overline{WEH}$	Write Enable Input High
$\overline{OE}$	Output Enable Input
NC	No Connect
$\overline{CE0} - \overline{CE3}$	Chip Enable Input
CS	Chip Select
$DQ_0 - DQ_{15}$	Data Input/Output
V_{CC}	+5 Volts
GND	Ground

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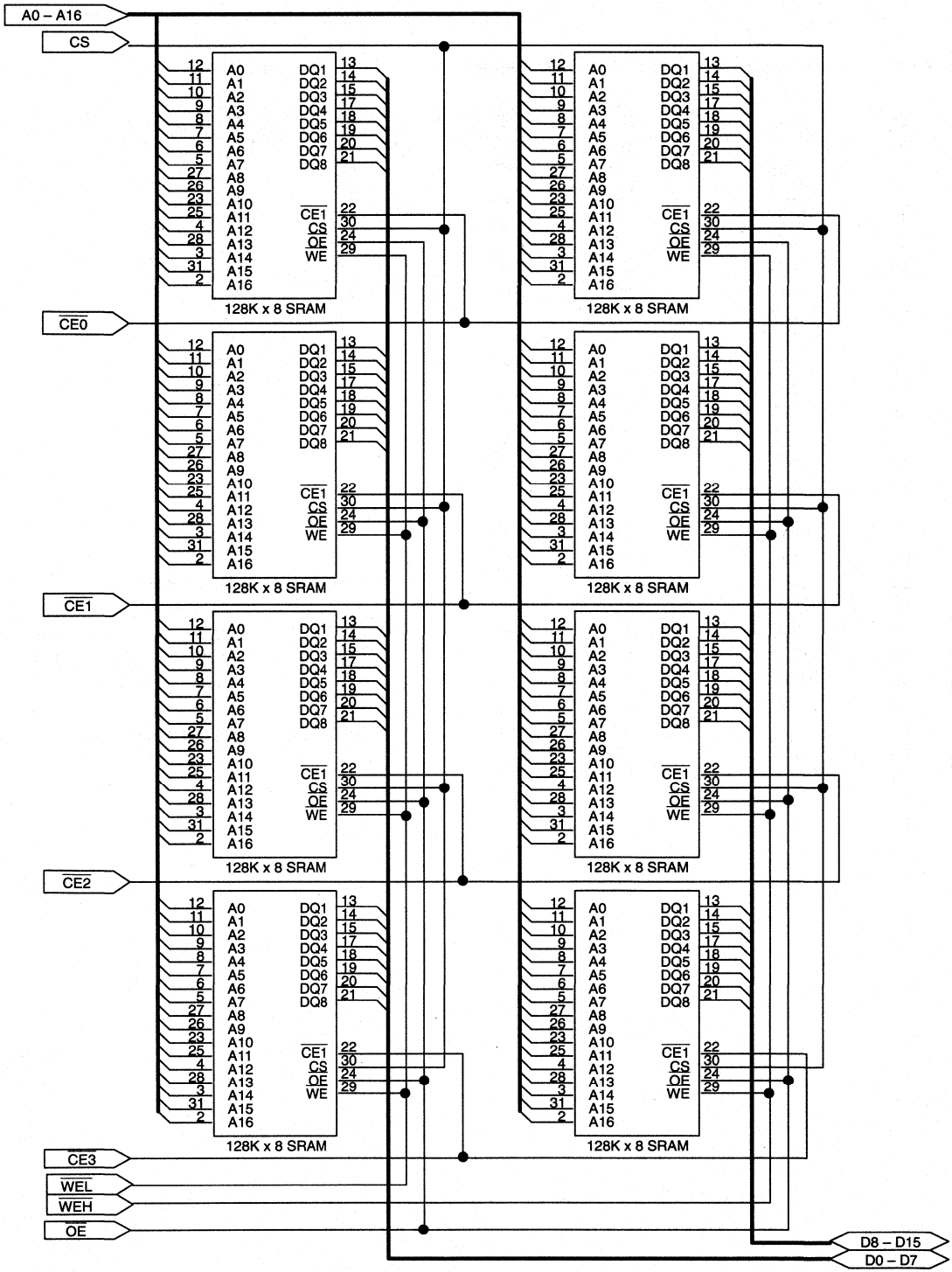
DS2229 STATIC RAM MODULE FUNCTION DIAGRAM Figure 2



ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage	-0.3V to +7.0V
Input, Input/Output Voltage	-0.3 to V_{CC} +0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

OPERATION MODE

MODE	$\overline{CE0}$ - $\overline{CE3}$	CS	$\overline{OE}$	$\overline{WE}$	A0 – A16	DQ – DQ15	POWER
READ	L	H	L	H	STABLE	DATA OUT	I_{CC0}
WRITE	L	H	X	L	STABLE	DATA IN	I_{CC0}
DESELECT	L	H	H	H	X	HIGH-Z	I_{CC0}
STANDBY	H	X	X	X	X	HIGH-Z	I_{CCS1}, I_{CCS2}
STANDBY	X	L	X	X	X	HIGH-Z	I_{CCS1}, I_{CCS2}

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			64	pF	
Input/Output Capacitance	$C_{I/O}$			80	pF	

RECOMMENDED DC OPERATING CONDITIONS

(t_A = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	V	

DC CHARACTERISTICS

(t_A = 0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$		8	µA	
I/O Leakage Current	I_{LO}	$\overline{CE0} - \overline{CE3} = V_{IH}$, $0V \le V_{I/O} \le V_{CC}$		8	µA	
Output High Current	I_{OH}	V_{OH} = 2.4V	-1.0		mA	
Output Low Current	I_{OL}	V_{OL} = 0.4V	2.1		mA	
Standby Current	I_{CCS1}	$\overline{CE0} - \overline{CE3}$ = 2.0V t_A = 25°C		8	mA	
Standby Current	I_{CCS2}	$\overline{CE0} - \overline{CE3} \ge V_{CC}$ -0.3V t_A=25°C		10	µA	
Operating Current	I_{CCO}	$\overline{CE0} - \overline{CE3}$ = 0.8V; Cycle=100 ns t_A= 25°C		100	mA	9

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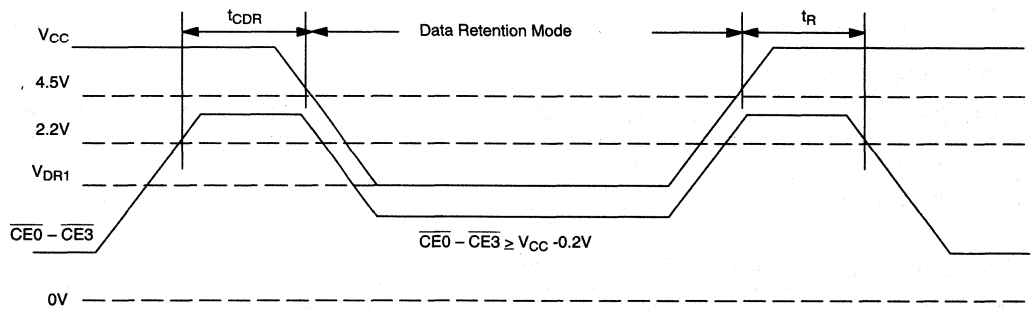
LOW VCC DATA RETENTION CHARACTERISTICS

(t_A = 0°C to 70°C)

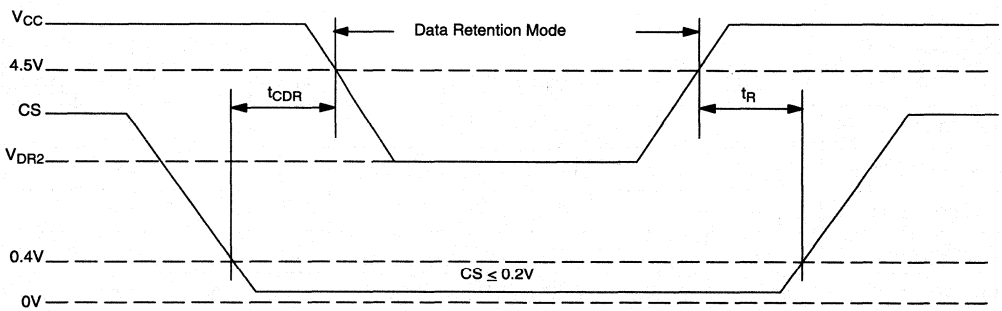
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITION
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CE0}$ – $\overline{CE3}$ ≥ V_{CC} -0.2V, CS ≥ V_{CC} -0.2V or 0V ≤ CS ≤ 0.2V V_{IN} ≥ 0V
Data Retention Current	I_{CCDR}	–	1	8	µA	V_{CC} = 3.0V, V_{IN} ≥ 0V $\overline{CE0}$ – $\overline{CE3}$ ≥ V_{CC} -0.2V, CS ≥ V_{CC} –0.2V or 0V ≤ CS ≤ 0.2V t_A=25°C
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	See Retention Waveform
Operation Recovery Time	t_R	5	–	–	ms	

LOW V_{CC} DATA RETENTION TIMING WAVEFORM (1) ($\overline{CE0}$ – $\overline{CE3}$ Controlled) Figure 3



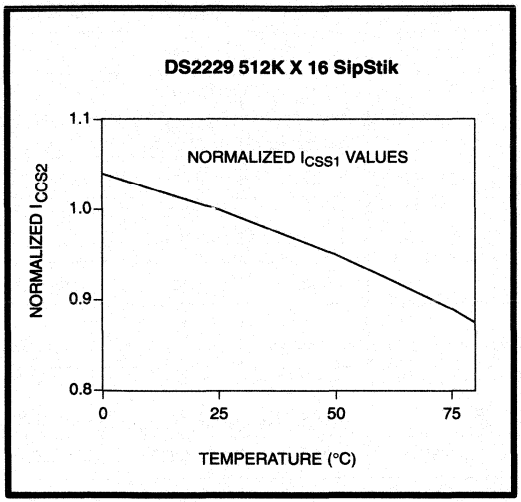
SEE NOTE 5

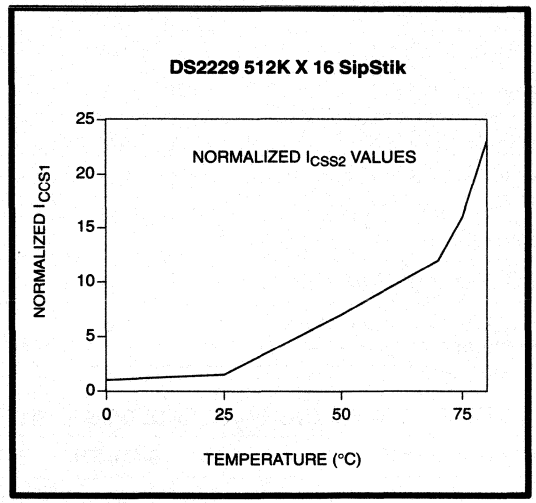
LOW V_{CC} DATA RETENTION TIMING WAVEFORM (2) (CS Controlled) Figure 4

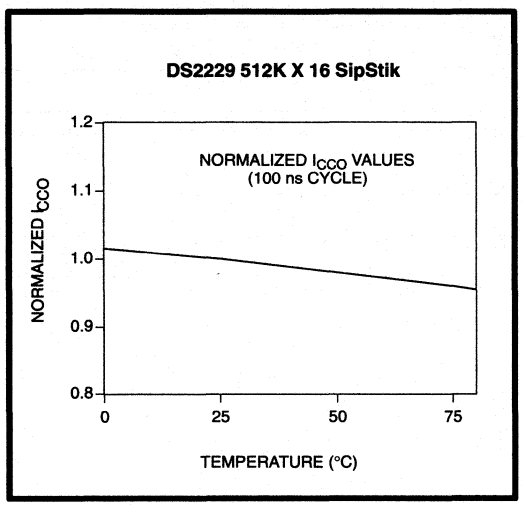


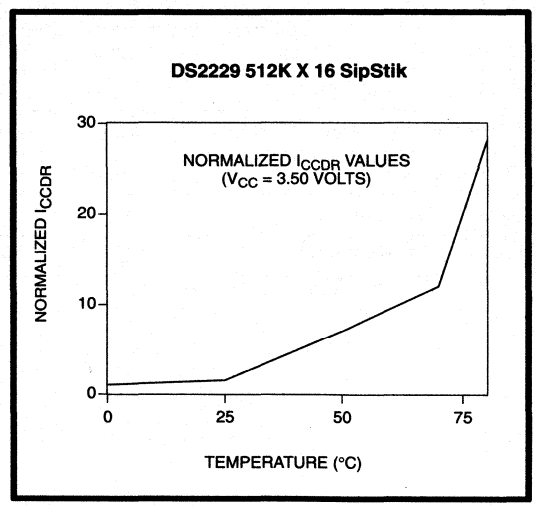
SEE NOTE 5

PRODUCT CHARACTERISTICS









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AC ELECTRICAL CHARACTERISTICS READ CYCLE

(0°C to 70°C; V_{CC} = 5V ± 10%)

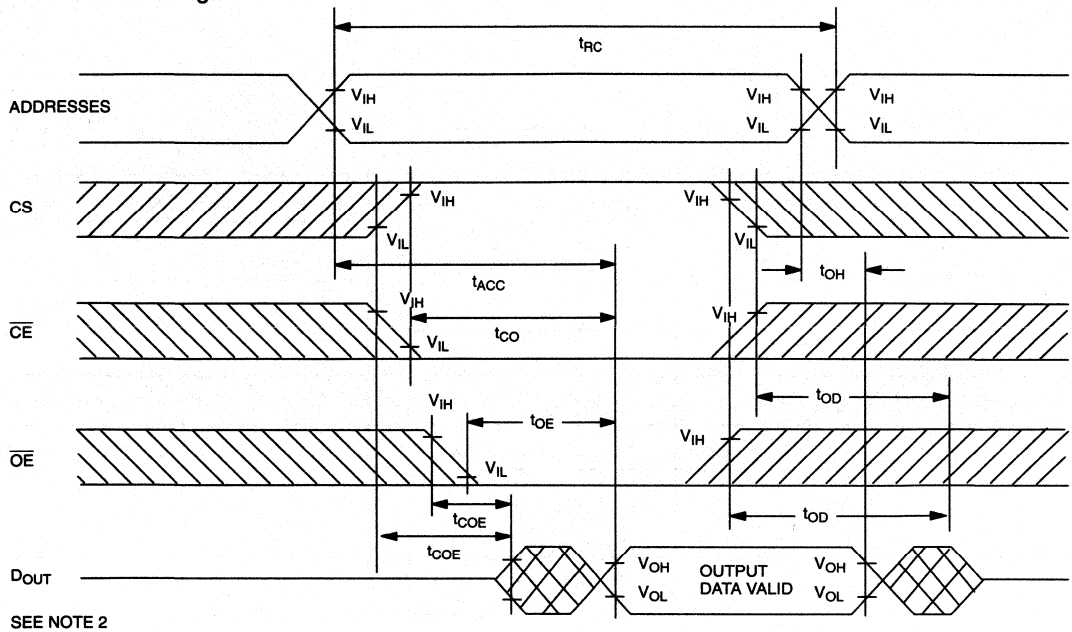
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	85			ns	
Access Time	t_{ACC}			85	ns	
$\overline{OE}$ to Output Valid	t_{OE}			45	ns	
$\overline{CE0}$ – $\overline{CE3}$ to Output Valid	t_{CO}			85	ns	
$\overline{OE}$ or $\overline{CE0}$ – $\overline{CE3}$ to Output In Low-Z	t_{COE}	10			ns	8
Output High-Z from Deselection	t_{OD}	0		30	ns	8
Output Hold from Address Change	t_{OH}	10			ns	

AC ELECTRICAL CHARACTERISTICS WRITE CYCLE

(0°C to 70°C; V_{CC} = 5V ± 10%)

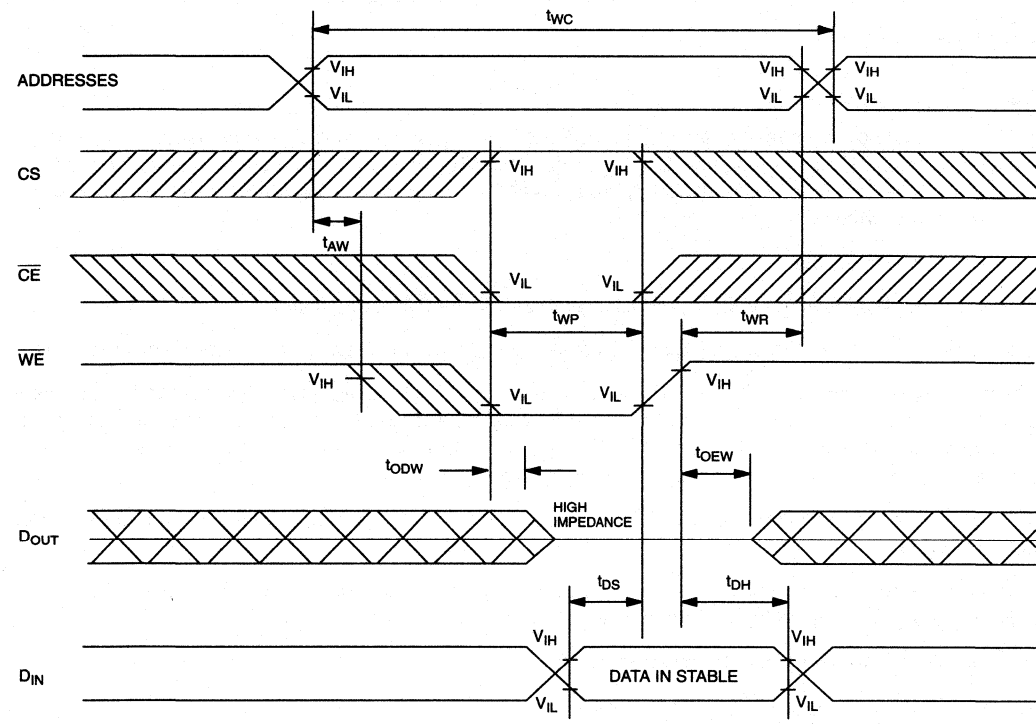
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	85			ns	
Write Pulse Width	t_{WP}	65			ns	1
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	10			ns	4
Output High-Z from $\overline{WE}$	t_{ODW}	0		30	ns	8
Output Active from $\overline{WE}$	t_{OEW}	5			ns	8
Data Setup Time	t_{DS}	35			ns	3
Data Hold Time from $\overline{WE}$	t_{DH}	0			ns	3

READ CYCLE Figure 5



SEE NOTE 2

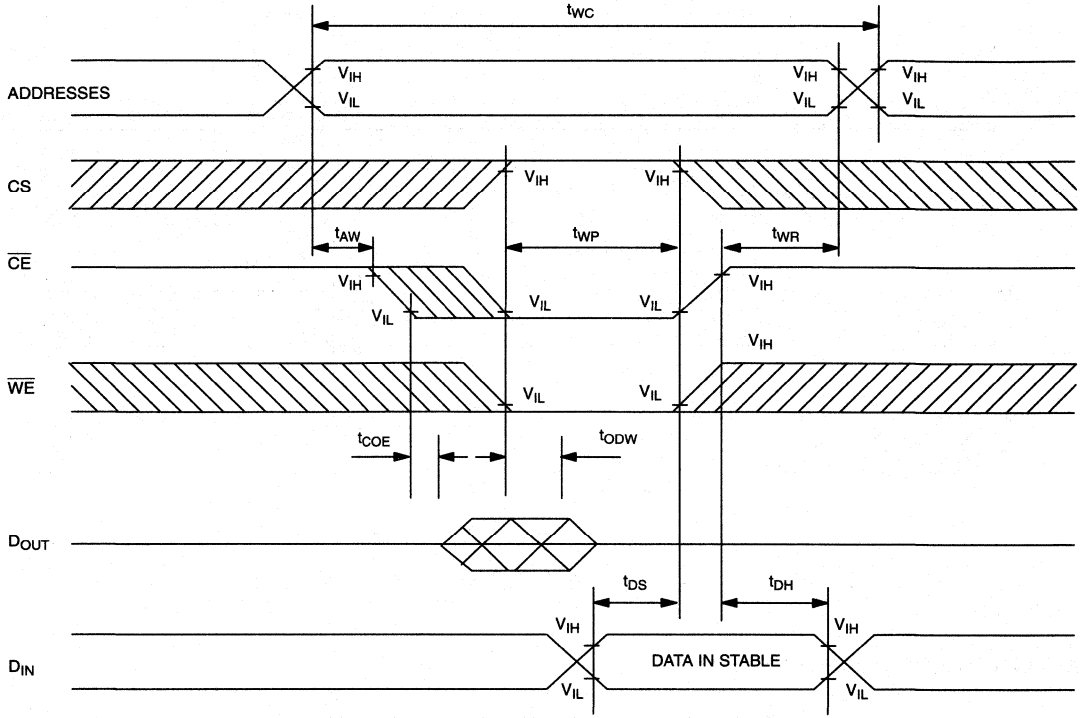
WRITE CYCLE1 Figure 6



SEE NOTES 1, 3, 4, 6, 7, AND 9

6

WRITE CYCLE 2 Figure 7

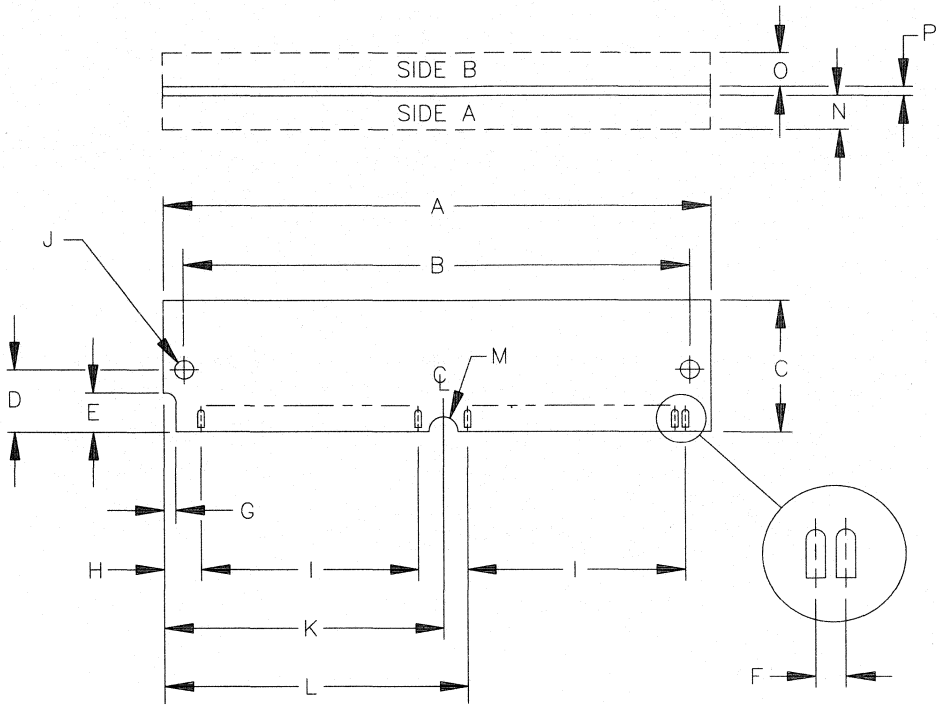


SEE NOTES 1, 3, 4, 6, 7, AND 9

NOTES:

1. A write occurs during the overlap of a low $\overline{CE0}$ – $\overline{CE3}$, a high CS, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CE0}$ – $\overline{CE3}$ going low, CS going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CE0}$ – $\overline{CE3}$ going high, CS going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. $\overline{WE}$ is high for a read cycle.
3. t_{DS} ends and t_{DH} begins at the earliest transaction among $\overline{CE0}$ – $\overline{CE3}$ going high.
4. t_{WR} is measured from the earliest of $\overline{CE0}$ – $\overline{CE3}$ or $\overline{WE}$ going high or CS going low to the end of write cycle.
5. CS controls address buffer, $\overline{WE}$ buffer, $\overline{CE0}$ – $\overline{CE3}$ buffer, $\overline{OE}$ buffer and D_{IN} buffer. If CS controls data retention mode, V_{IN} levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CE0}$ – $\overline{CE3}$, I/O) can be in the high impedance state. If $\overline{CE0}$ – $\overline{CE3}$ controls data retention mode, CS must be $CS \geq V_{CC} - 0.2V$ or $0V \leq CS \leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.
6. If $\overline{CE0}$ – $\overline{CE3}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in a high impedance state.
7. If $\overline{CE0}$ – $\overline{CE3}$ is low and CS is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
8. This parameter is sampled and not 100% tested.
9. Only one $\overline{CE}$ active during any read or write cycle.

DS2229 80-PIN SIP STIK



PKG	80–PIN	
DIM	MIN	MAX
A	4.645	4.655
B	4.379	4.389
C	0.729	0.739
D	0.395	0.405
E	0.245	0.255
F	0.050 BSC	
G	0.075	0.085
H	0.245	0.255
I	1.950 BSC	
J	0.120	0.130
K	2.320	2.330
L	2.445	2.455
M	0.057	0.067
N		0.130
O		0.130
P		0.054

6

USER INSERTABLE MEMORY

7

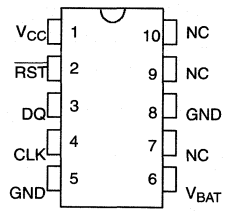
DALLAS SEMICONDUCTOR

DS1200
Serial RAM Chip

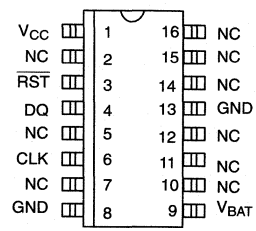
FEATURES

- 1024 bits of read/write memory
- Low data retention current for battery backup applications
- 4 million bits/second data rate
- Single byte or multiple byte data transfer capability
- No restrictions on the number of write cycles
- Low-power CMOS circuitry
- Applications include:
  - software authorization
  - computer identification
  - system access control
  - secure personnel areas
  - calibration
  - automatic system setup
  - traveling work record

PIN ASSIGNMENT



10-Pin DIP (300 MIL)
See Mech. Drawings Section



16-Pin SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}	– +5 Volts
$\overline{RST}$	– RESET
DQ	– Data Input/Output
CLK	– Clock
GND	– Ground
V_{BAT}	– Battery (+)
NC	– No Connection

DESCRIPTION

The DS1200 Serial RAM Chip is a miniature read/write memory which can randomly access individual 8-bit strings (bytes) or sequentially access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, $\overline{RST}$, and DATA INPUT/OUTPUT.

Nonvolatility can be achieved by connecting a battery of 2 to 4 volts at the battery input V_{BAT}. A load of 0.5 µA should be used to size the external battery for the required data retention time. If nonvolatility is not required the V_{BAT} pin should be grounded.

For a complete description of operating conditions, electrical characteristics, bus timing, and signal descriptions other than V_{BAT}, see the DS1201 Electronic Tag 1024-Bit data sheet.

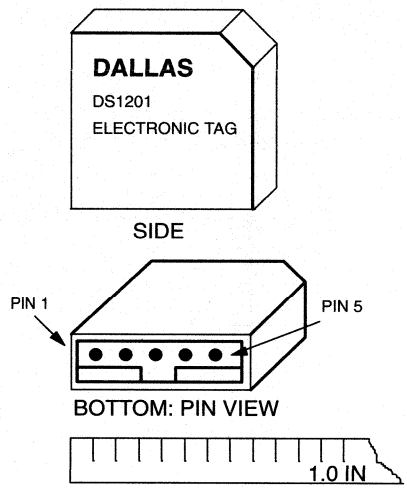
DALLAS SEMICONDUCTOR

DS1201
Electronic Tag

FEATURES

- User-insertable, nonvolatile 1024 bits of read/write memory
- Low-power CMOS circuitry allows for 10 years of data retention
- Miniature and transportable
- Durable and rugged
- Impervious to handling
- Four million bits/second data rate
- Single-byte or multiple-byte data transfer capability
- No restrictions on the number of write cycles
- Applications include computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling work record.

PIN ASSIGNMENT



See Mech. Drawings Section

PIN DESCRIPTION

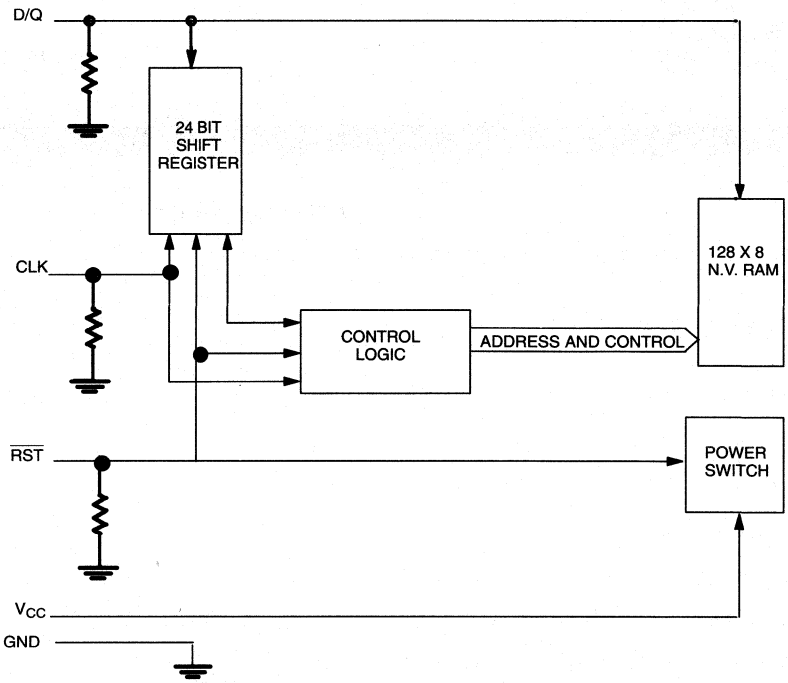
Pin 1	Vcc	+5 Volts
Pin 2	$\overline{RST}$	$\overline{RESET}$
Pin 3	DQ	Data Input/Output
Pin 4	CLK	Clock
Pin 5	GND	Ground

7

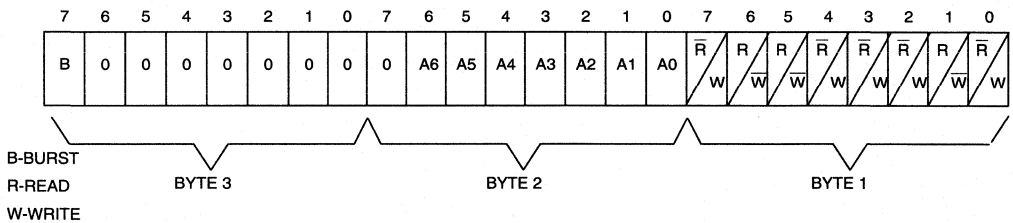
DESCRIPTION

The DS1201 Electronic Tag is a miniature nonvolatile, read/write memory system which can randomly access individual 8-bit strings (bytes) or sequentially access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, $\overline{RESET}$, and DATA INPUT/OUTPUT. Low pin count and a guided entry for a mating receptacle overcome mechanical problems normally encountered when a conventional integrated circuit package is inserted by the end user.

ELECTRONIC TAG BLOCK DIAGRAM Figure 1



ADDRESS/COMMAND Figure 2



OPERATION

The block diagram (Figure 1) of the Electronic Tag illustrates the main elements of the device: shift register, control logic, nonvolatile RAM, and power switch. To initiate a memory cycle $\overline{\text{RESET}}$ is taken high and 24 bits are loaded into the shift register, providing both address and command information. Each bit is input serially on the rising edge of the CLOCK input. Seven address bits specify one of the 128 RAM locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 CLOCKs which load the shift register, additional CLOCKs will output data for a read or input data for a write. The number of CLOCK pulses equals 24 plus 8 for byte mode or 24 plus 1024 for burst mode.

The tag can be used as a four-pin or five-pin device, depending on the application. For hardwired applications, active power is supplied by the Vcc pin. Alternatively, for user-insertable applications, power can be supplied by the $\overline{\text{RESET}}$ pin.

ADDRESS/COMMAND

Each memory transfer consists of a three-byte input called the address/command. The address/command is shown in Figure 2. As defined, the first byte of the address/command specifies whether the memory will be written into or read . If any one of the bits of the first byte of the address/command fails to meet the exact pattern of read or write, the cycle is aborted and all future inputs to the tag are ignored until $\overline{RESET}$ is brought low and then high again to begin a new cycle. The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address inputs A0 in bit 0 through A6 in bit 6. Bit 7 of the second byte of the address/command word must be set to logic 0. This bit is reserved for future higher density versions of the tag. If bit 7 does not equal logic 0, the cycle is aborted and all future inputs to the tag are ignored until $\overline{RESET}$ is brought low and then high again to begin a new cycle. The third byte of the address/command is also set aside for future expansion. Bits 0 through 6 must be set to logic 0 or the cycle is aborted and all future inputs are ignored until $\overline{RESET}$ is brought low and then high again to begin a new cycle. Bit 7 of byte 3 of the address/command is used along with address bits A0 through A6 to define burst mode. When A0 through A6 equals logic 0 and bit 7 of byte 3 of the address command equals logic 1, the tag will enter the burst mode after the address/command sequence is complete.

BURST MODE

Burst mode is specified for the Electronic Tag when all address bits (A0-A6) of the address/command are set to logic 0 and bit 7 of byte 3 to logic 1. The burst mode causes 128 consecutive bytes to be read or written. Burst mode terminates when the $\overline{RESET}$ input is driven low.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RESET}$ input high. The $\overline{RESET}$ input serves three functions. First, $\overline{RESET}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{RESET}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RESET}$ of 2 mA @ 3.8 volts is required. However if the Vcc pin is connected to a 5-volt source within nominal limits, then the $\overline{RESET}$ pin is not used as a source of power and input levels revert to normal V_{IH} and V_{IL} inputs with a drive current requirement of 500 µA. Finally, the $\overline{RESET}$ signal provides a method of terminating either single byte or multiple byte data transfers. A CLOCK cycle is a sequence of falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of the CLOCK cycle. Address/command bits and data bits are input on the rising edge of the CLOCK and data bits are output on the falling edge of the CLOCK. All data transfer terminates if the $\overline{RESET}$ input is low and D/Q pin goes to a high impedance state. When data transfer to the tag is terminated using $\overline{RESET}$, the transition of $\overline{RESET}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 3.

DATA INPUT

Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next eight CLOCK cycles, assuming that the read/write and write/read bits are properly set (for data input byte 1, bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1).

DATA OUTPUT

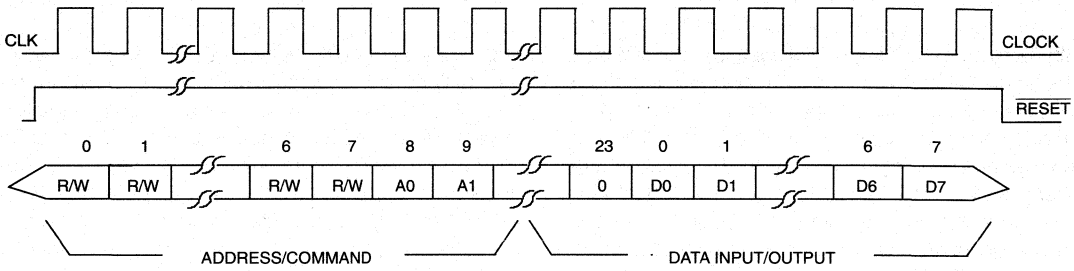
Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles (for data output byte 1, bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0).

TAG CONNECTIONS

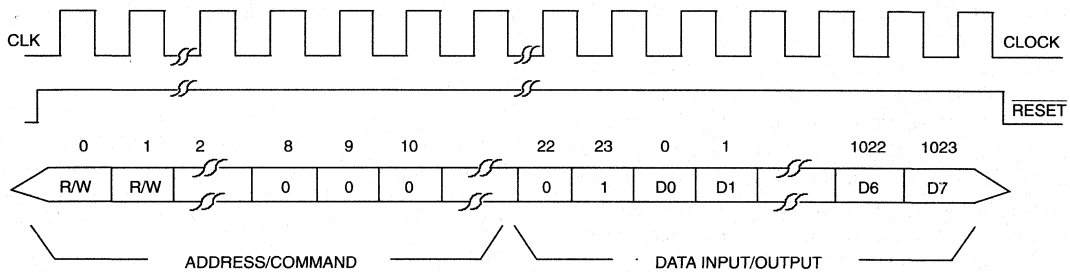
The tag is designed to be plugged into a standard 5-pin, 0.1-inch center SIP receptacle. A key is provided to prevent the tag from being plugged in backwards and to aid in alignment of the receptacle. For portable applications, contact to the tag pins can be determined to ensure connection integrity before data transfer begins. CLOCK, $\overline{RESET}$, and DATA INPUT/OUTPUT all have internal 40K ohm pulldown resistors to ground which can be sensed by a reading device.

DATA TRANSFER Figure 3

SINGLE BYTE TRANSFER



BURST MODE TRANSFER

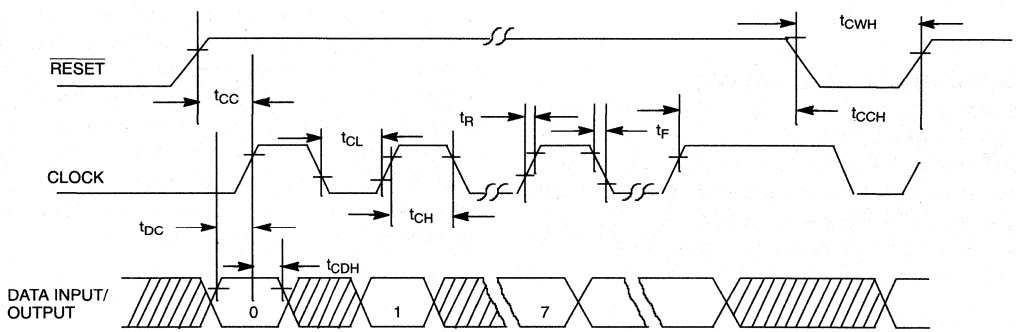


NOTES:

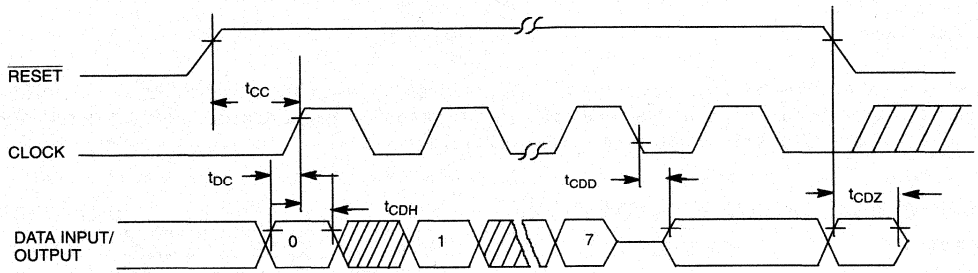
1. Data input sampled on rising edge of clock cycle.
2. Data output changes on falling edge of clock.

READ/WRITE DATA TRANSFER Figure 4

WRITE DATA TRANSFER



READ DATA TRANSFER



NOTES:

1. All voltages and resistances are referenced to ground.
2. Input levels apply to CLK, D/Q, and $\overline{RST}$ while V_{CC} is within nominal limits. When V_{CC} is not connected to the tag, then $\overline{RST}$ input reverts to V_{IHE}.
3. Measured at V_{IH} = 2.0 or V_{IL} = 0.8V and 10 ns maximum rise and fall time.
4. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
5. For CLK, D/Q, $\overline{RST}$ and V_{CC} at 5 volts.
6. Load capacitance = 50 pF.
7. Applies to $\overline{RST}$ when V_{CC} < 3.8 volts.
8. Measured with outputs open.
9. Measured at V_{IH} of $\overline{RST}$ greater than or equal to 3.8V when $\overline{RST}$ supplies power.
10. Logic 1 maximum is V_{CC} + 0.3V if the V_{CC} pin supplies power and $\overline{RST}$ +0.3V if the $\overline{RST}$ pin supplies power.
11. $\overline{RST}$ logic 1 maximum is V_{CC} + 0.3V if the V_{cc} pin supplies power and 5.5V maximum if $\overline{RST}$ supplies power.
12. Each DS1201 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
13. Average AC $\overline{RST}$ current can be determined using the following formula:
    $I_{TOTAL} = 2 + I_{LOAD\ DC} + (4 \times 10^{-3})(CL + 140)f$
    I_{TOTAL} and I_{LOAD} are in mA; CL is in pF; f is in MHz.
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHz gives an I_{TOTAL} current of 5 mA.
14. When $\overline{RST}$ is supplying power t_{CWH} must be increased to 100 ms.

7

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0 to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1,2,10
Logic 0	V_{IL}	-0.3		0.8	V	1
$\overline{\text{RESET}}$ Logic 1	V_{IHE}	3.8			V	1,7,11
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_L			+500	µA	5
Output Leakage	I_{LO}			+500	µA	5
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			+2	mA	
$\overline{\text{RST}}$ Input Resistance	Z_{RST}	10		40	K ohms	1
D/Q Input Resistance	Z_{DQ}	10		40	K ohms	1
CLK Input Resistance	Z_{CLK}	10		40	K ohms	1
Active Current	I_{CC1}			6	mA	8
Standby Current	I_{CC2}			2.5	mA	8
$\overline{\text{RST}}$ Current	I_{RST}				mA	7,8,13

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	3,9
Data to CLK Hold	t_{CDH}	40			ns	3,9
Data to CLK Delay	t_{CDD}			125	ns	3,4,6,9
CLK Low Time	t_{CL}	125			ns	3,9
CLK High Time	t_{CH}	125			ns	3,9
CLK Frequency	f_{CLK}	DC		4.0	MHz	3,9
CLK Rise & Fall	t_R,t_F			500	ns	9
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	3,9
CLK to RST Hold	t_{CCH}	40			ns	3,9
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	3,9,14
$\overline{RST}$ to I/O High Z	t_{CDZ}			50	ns	3,9
Expected Data Retention Time	t_{DR}	10			Years	12

7

DALLAS SEMICONDUCTOR

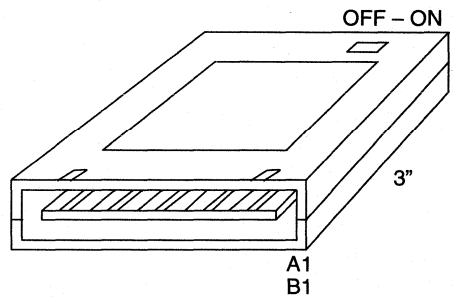
DS1217A
Nonvolatile Read/Write Cartridge

FEATURES

- User-insertable
- Capacity up to 32K x 8
- Standard bytewide pinout facilitates connection to JEDEC 28-pin DIP socket via ribbon cable
- Data retention greater than 10 years
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0°C to 70°C

PIN ASSIGNMENT

Name	Position		Name
Ground	A1	B1	No Connect
+5 Volts	A2	B2	Address 14
$\overline{\text{Write Enable}}$	A3	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
$\overline{\text{Output Enable}}$	A8	B8	Address 3
Address 10	A9	B9	Address 2
$\overline{\text{Cartridge Enable}}$	A10	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data I/O 0
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground



See Mech. Drawings Section

DESCRIPTION

The DS1217A is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge is available in densities ranging from 2K x 8 to 32K x 8 in 8K byte increments. A card edge connector is required for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a 28-conductor ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems that have JEDEC 28-pin bytewide memory sites.

The DS1217A cartridge has a lifetime energy source to retain data and circuitry needed to automatically protect memory contents. Reading and writing the memory locations is the same as using conventional static RAM. If the user wants to convert from read/write memory to read-only memory, a manual switch is provided to unconditionally protect memory contents.

READ MODE

The DS1217A executes a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$); the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS1217A is in the write mode whenever both the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The last falling edge to occur of either $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the first rising edge of either $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write protected.

DATA RETENTION MODE

The Nonvolatile Cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217A constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM. To retain data during power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS1217A checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge, the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. For this reason, the cartridge provides battery redundancy. The DS1217A features an internal isolation switch that provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts.

REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems that contain 28-pin bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin ribbon cable connected to a 30-contact card edge connector, AMP Part Number 499188-4. The 28-pin ribbon cable must be right-justified such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B15) on the card edge connector should be grounded to further enhance data integrity. Access time push-out may occur as the distance between the cartridge and driving circuitry is increased.

CARTRIDGE NUMBERING Table 1

PART NO.	DENSITY	UNUSED ADDRESS INPUTS
DS1217A/16K-25	2K x 8	*Address 11, 12, 13, 14
DS1217A/64K-25	8K x 8	*Address 13, 14
DS1217A/128K-25	16K x 8	*Address 14
DS1217A/192K-25	24K x 8	
DS1217A/256K-25	32K x 8	

*Unused address inputs must be held low (V_{IL}).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Connection Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX.	UNITS	NOTES
Input Leakage Current	I_{IL}	-60		+60	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-10		+10	µA	
Output Current @ 2.4V	I_{OH}	-1.0	-2.0		mA	
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA	
Standby Current $\overline{CE}$=2.2V	I_{CCS1}		5.0	10	mA	
Operating Current	I_{CCO1}		35	75	mA	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX.	UNITS	NOTES
Input Capacitance	C_{IN}			75	pF	
Input/Output Capacitance	$C_{I/O}$			75	pF	

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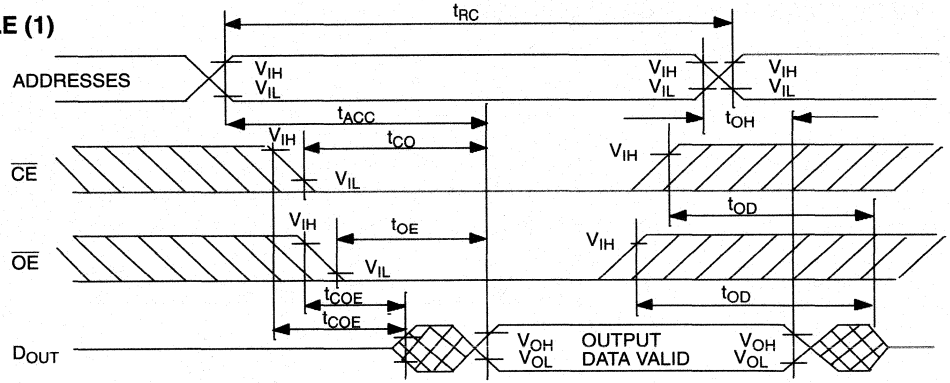
AC ELECTRICAL CHARACTERISTICS

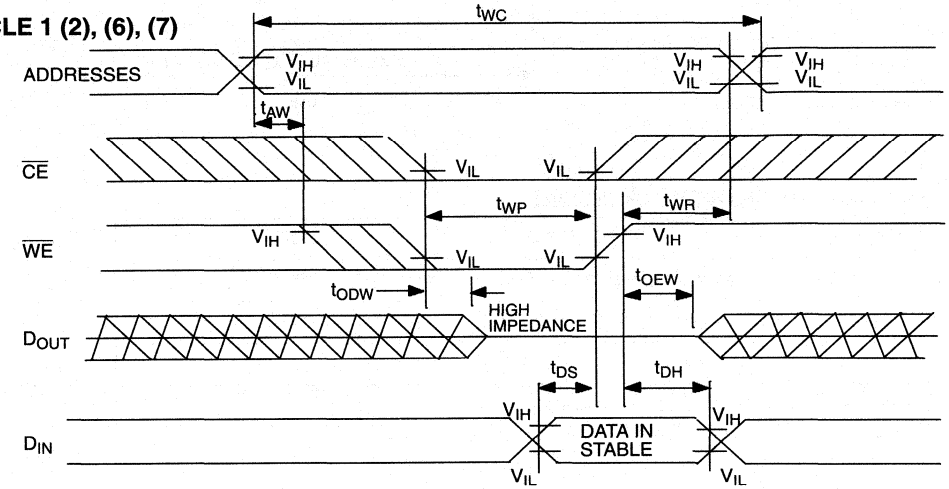
(0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			250	ns	
$\overline{OE}$ to Output Valid	t_{OE}			125	ns	
$\overline{CE}$ to Output Valid	t_{CO}			250	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5			ns	5
Output High Z from Deselection	t_{OD}			125	ns	5
Output Hold from Address Change	t_{OH}	5			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High Z from $\overline{WE}$	t_{ODW}			100	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5			ns	5
Data Setup Time	t_{DS}	100			ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20			ns	4

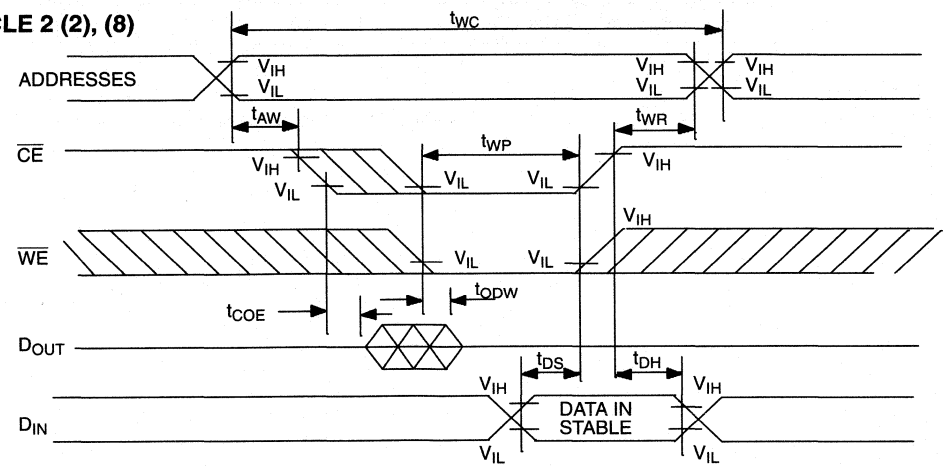
READ CYCLE (1)



WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



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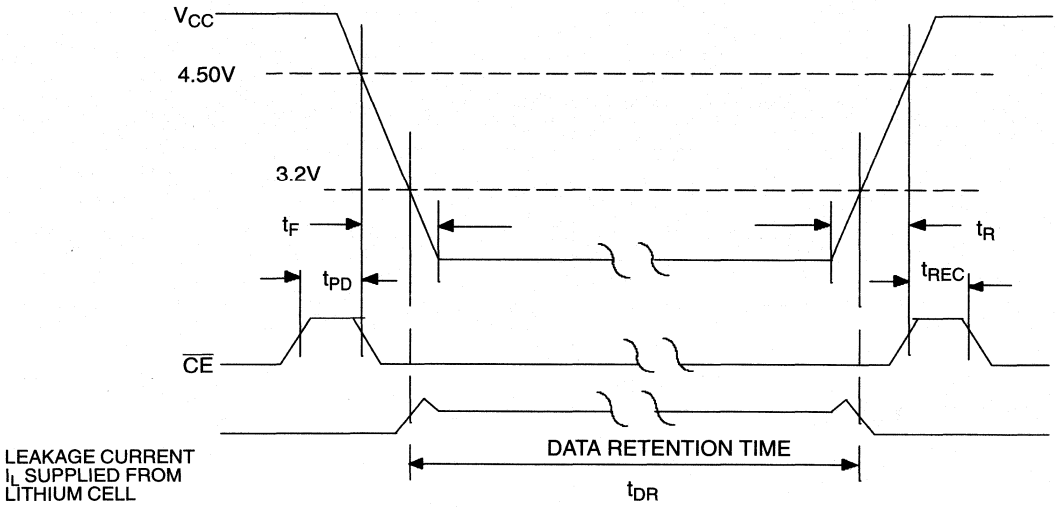
POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(0°C to 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power-Down	0		µs	10
t_F	V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		µs	
t_R	V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		µs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up	2	125	ms	10

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when the device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during the write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remains in a high impedance state during this period.
9. Each DS1217A is marked with a 4-digit date code AABB. AA designates the year of manufacture; BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.

DC TEST CONDITIONS

Outputs Open
t Cycle = 250ns
All Voltages Are Referenced to Ground

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5 V

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DALLAS SEMICONDUCTOR

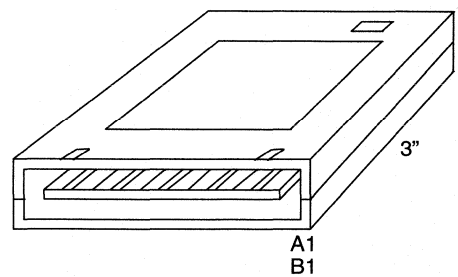
DS1217M
Nonvolatile Read/Write Cartridge

FEATURES

- User-insertable
- Data retention greater than 5 years
- Capacity up to 512K x 8
- Standard bytewide pinout facilitates connection to JEDEC 28-pin DIP via ribbon cable
- Software-controlled banks maintain 32 x 8 JEDEC 28-pin compatibility
- Multiple cartridges can reside on a common bus
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0°C to 70°C

PIN ASSIGNMENT

Name	Position		Name
Ground	A1	B1	No Connect
+5 Volts	A2	B2	Address 14
$\overline{\text{Write Enable}}$	A3	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
$\overline{\text{Output Enable}}$	A8	B8	Address 3
Address 10	A9	B9	Address 2
$\overline{\text{Cartridge Enable}}$	A10	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data I/O 0
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground



See Mech. Drawings Section

DESCRIPTION

The DS1217M is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The Nonvolatile Cartridge has memory capacities from 64K x 8 to 512K x 8. The cartridge is accessed in continuous 32K byte banks. Bank switching is accomplished under software control by pattern recognition from the address bus. A card edge connector is required for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems which have JEDEC 28-pin bytewide memory sites.

READ MODE

The DS1217M executes a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low). The unique address specified by the address inputs (A0-A14) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ (cartridge enable) and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the late occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS1217M is in the write mode whenever both the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The last occurring falling edge of either $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the first rising edge of either $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated.The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write-protected.

DATA RETENTION MODE

The Nonvolatile Cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217M constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write-protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS1217M checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge thus has redundant batteries and an internal isolation switch which provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

BANK SWITCHING

Bank switching is accomplished via address lines A8, A9, A10, and A11. Initially, on power-up all banks are deselected so that multiple cartridges can reside on a common bus. Bank switching requires that a predefined pattern of 64 bits is matched by sequencing 4 address inputs (A8 through A11) 16 times while ignoring all other address inputs. Prior to entering the 64-bit pattern which will set the band switch, a read cycle of 1111 (address inputs A8 through A11) must be executed to guarantee that pattern entry starts with the first set of 3 bits. Each set of address inputs is entered into the DS1217M by executing read cycles.The first eleven cycles must match the exact bit pattern as shown in Table 2. The last five cycles must match the exact bit pattern for addresses A9, A10, and A11. However, address line 8 defines which of the 16 banks is to be enabled, or all banks are deselected, as per Table 3. Switching from one bank to another occurs as the last of the 16 read cycles is completed. A single bank is selected at any one time. A selected bank will remain active until a new bank is selected, all banks are deselected, or until power is lost. (See DS1222 BankSwitch Chip data sheet for more detail.)

REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems which contain 28-pin bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin cable connected to a 30-contact card edge connector, AMP Part Number 499188-4. The 28-pin ribbon cable must be right-justified, such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B1) on the card edge connector should be grounded to further enhance data integrity. Access time push-out may occur as the distance between the cartridge and the driving circuitry is increased.

CARTRIDGE NUMBERING Table 1

PART NO.	DENSITY	NO. OF BANKS
DS1217M 1/2-25	64K x 8	2
DS1217M 1-25	128K x 8	4
DS1217M 2-25	156K x 8	8
DS1217M 3-25	384K x 8	12
DS1217M 4-25	512K x 8	16

ADDRESS INPUT PATTERN Table 2

ADDRESS INPUTS	BIT SEQUENCE															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A8	1	0	1	0	0	0	1	1	0	1	0	X	X	X	X	X
A9	0	1	0	1	1	1	0	0	1	1	0	0	0	0	1	1
A10	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A11	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X = See Table 3

BANK SELECT TABLE Table 3

BANK	A8 BIT SEQUENCE				
SELECTED	11	12	13	14	15
BANKS OFF	0	X	X	X	X
BANK 0	1	0	0	0	0
BANK 1	1	0	0	0	1
BANK 2	1	0	0	1	0
BANK 3	1	0	0	1	1
BANK 4	1	0	1	0	0
BANK 5	1	0	1	0	1
BANK 6	1	0	1	1	0

BANK	A8 BIT SEQUENCE				
BANK 7	1	0	1	1	1
BANK 8	1	1	0	0	0
BANK 9	1	1	0	0	1
BANK 10	1	1	0	1	0
BANK 11	1	1	0	1	1
BANK 12	1	1	1	0	0
BANK 13	1	1	1	0	1
BANK 14	1	1	1	1	0
BANK 15	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS*

Voltage on Connection Relative to Ground	-0.3V to + 7.0V
Operation Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-60		+60	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-10		+10	µA	
Output Current @ 2.4V	I_{OH}	-1.0	-2.0		mA	
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		15	25	mA	
Operating Current	I_{CCO1}		50	100	mA	

CAPACITANCE

(t_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			100	pF	
Input/Output Capacitance	C_{OUT}			100	pF	

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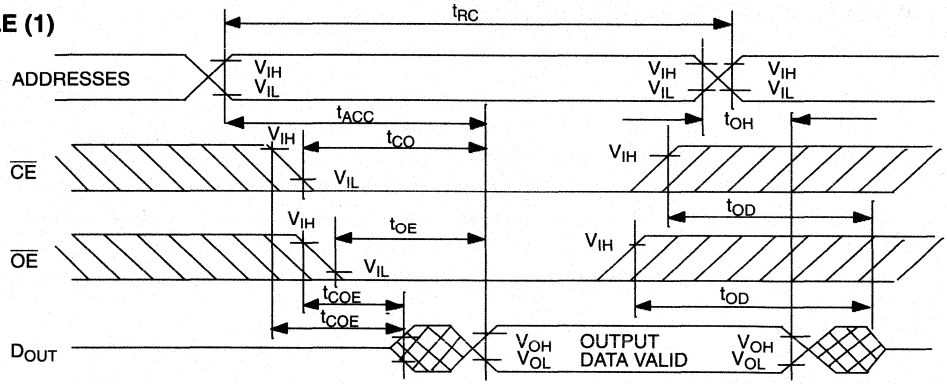
AC ELECTRICAL CHARACTERISTICS

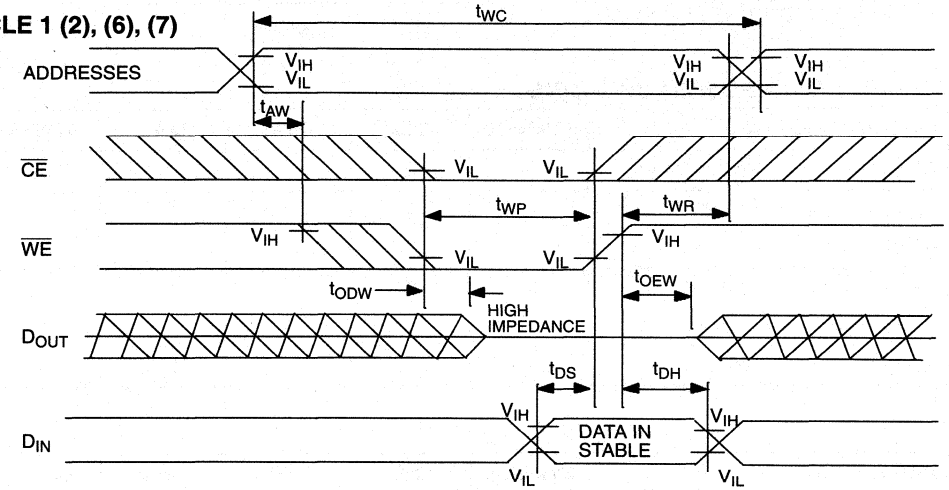
(0°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			250	ns	
$\overline{OE}$ to Output Valid	t_{OE}			125	ns	
$\overline{CE}$ to Output Valid	t_{CO}			210	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5			ns	5
Output High Z From Deselection	t_{OD}			125	ns	5
Output Hold From Address Change	t_{OH}	5			ns	
Read Recovery Time	t_{RR}	40			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High Z From $\overline{WE}$	t_{ODW}			100	ns	5
Output Active From $\overline{WE}$	t_{OEW}	5			ns	5
Data Setup Time	t_{DS}	100			ns	4
Data Hold Time From $\overline{WE}$	t_{DH}	20			ns	4

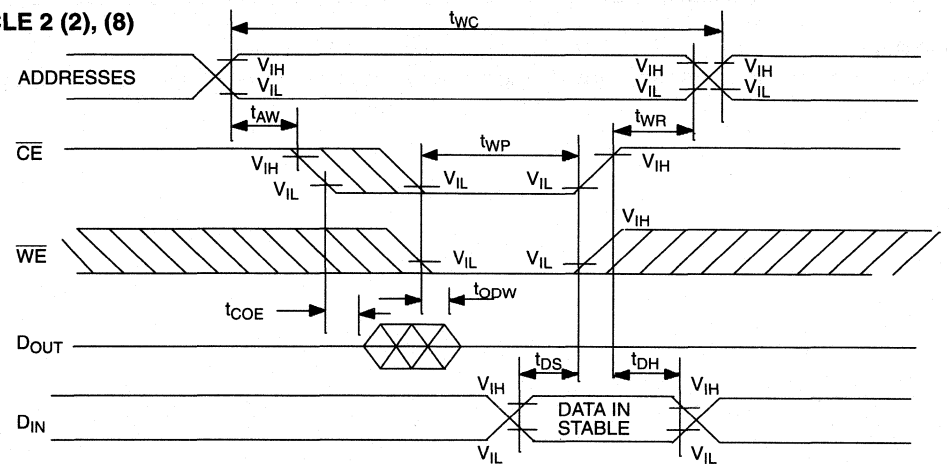
READ CYCLE (1)



WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



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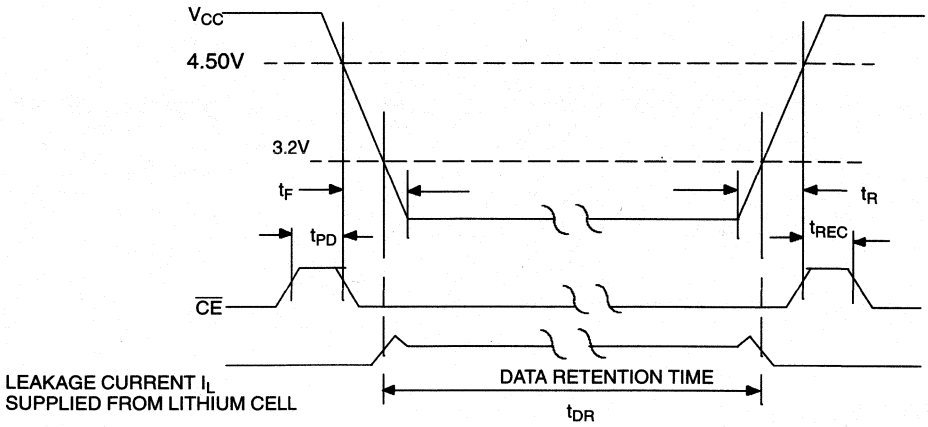
POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(0° to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at VIH before Power-Down	t_{PD}	0			µs	10
V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	t_F	100			µs	
V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}	2		125	ms	10

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	5			years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during a write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ of $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state in this period.
9. Each DS1217M is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.

DC TEST CONDITIONS

Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

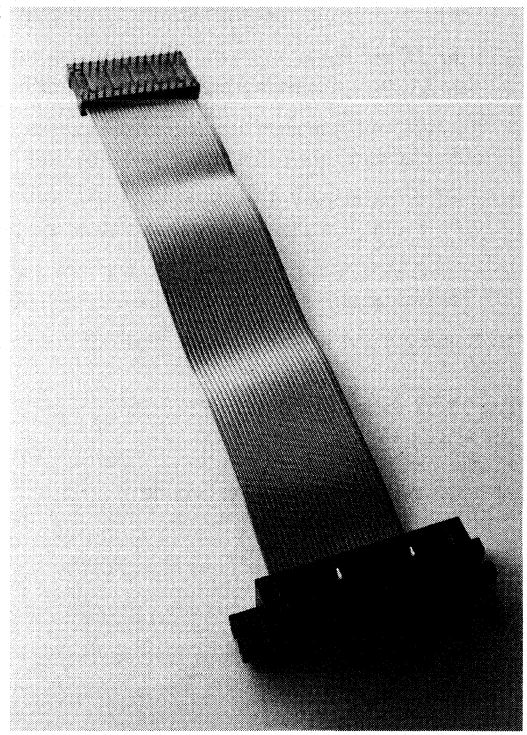
7

DALLAS SEMICONDUCTOR

DS9000
Bytewide Cable Harness

FEATURES

- Converts 30-position card edge to popular bytewide 28-pin DIP socket
- Bifurcated cantilever beam card edge design provides redundant contact
- Mechanical keys provide proper insertion and withdrawal of Dallas Semiconductor DS1217 Nonvolatile Read/Write Cartridges
- 28-position DIP plug inserts into any standard 28-position IC DIP socket
- Color stripe indicates pin one on 28-pin DIP plug
- Standard six-inch cable length



DESCRIPTION

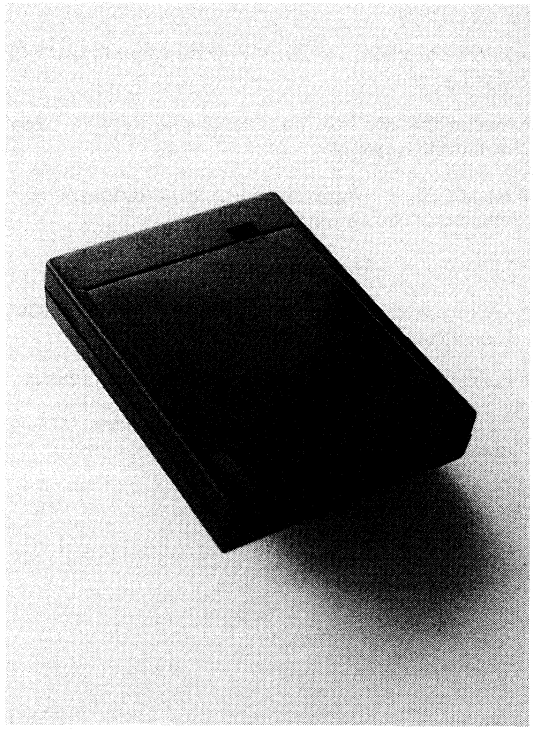
The DS9000 Bytewide Cable Harness is a specially designed cable harness which converts Dallas Semiconductor DS1217 Nonvolatile Read/Write Cartridges or any other 30-position card edge to the popular bytewide 28-pin DIP socket. An additional ground lead and dual key positions allow for proper insertion and withdrawal of Nonvolatile Read/Write Cartridges. A six-inch cable length allows for flexibility in end applications but does not substantially affect the performance characteristics of the DS1217.

DALLAS SEMICONDUCTOR

DS9002
Cartridge Housing

FEATURES

- Two-piece, snap together construction
- Matches form factor of Dallas Semiconductor DS1217 Nonvolatile Read/Write Cartridges
- Made of rugged, flame-retardant ABS plastic
- Accepts DS9003 Cartridge Proto Board
- Opening for switch or jumper
- Component clearance of .175" solder side, .200" circuit side using .062" PCB



7

DESCRIPTION

The DS9002 Cartridge Housing is a rugged, two-piece snap together cartridge housing designed for use in any portable cartridge application. Components can be either through-hole mounted or surface mounted on both sides depending upon density requirement and board design. The outside profile of the PCB should match the DS9003 Cartridge Proto Board. Applications include nonvolatile static RAM, ROM, or EPROM memory cartridges.

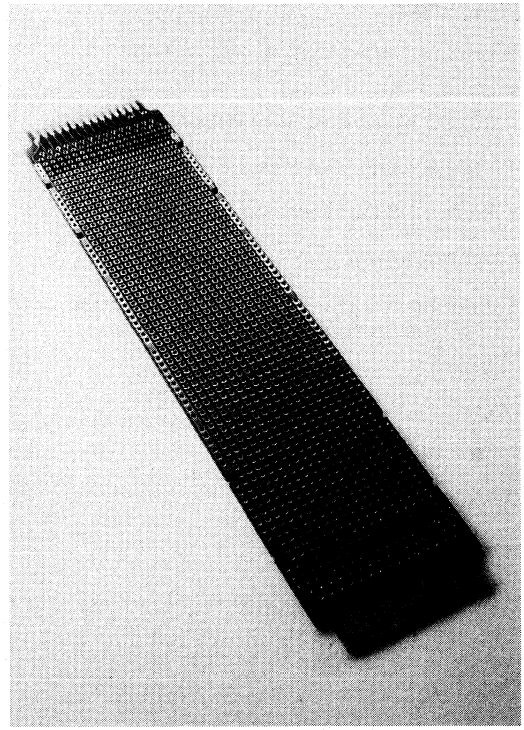
062690 1/1

DALLAS SEMICONDUCTOR

DS9003
Cartridge Proto Board

FEATURES

- Matches profile of DS1217 Nonvolatile Read/Write Cartridges
- Plated through-hole pattern for wire wrap or solder mount development
- Allows for a single double-size cartridge or two standard-size cartridges
- Gold-plated card edge fingers
- Connects to standard 28-pin DIP socket via DS9000 Bytewide Cable Harness
- Key slots provide for proper insertion and removal
- Separate full length power and ground buses for ease of layout



FEATURES

The DS9003 Cartridge Proto Board is a developmental printed circuit board for prototyping portable hand-held cartridges. The gold-plated card edge connections conform to the popular 28-pin bytewide DIP socket pinout when used with the DS9000 Bytewide Cable Harness. The card profile matches that of the DS1217 Nonvolatile Read/Write Cartridges and can be used with the DS9002 Cartridge Housing.

MULTIPORT MEMORY

8

DALLAS SEMICONDUCTOR

DS1280
3-Wire to Bytewide Converter Chip

FEATURES

- Adapts JEDEC bytewide memory to a 3-wire serial port
- Supports 512K bytes of memory
- 68-pin version provides arbitration mechanisms for dual port operation
- CMOS circuitry design for battery backup and battery operate applications
- Cyclic redundancy check monitors serial data transmission for error
- Available in 44- or 80-pin quad flat pack for high density requirements

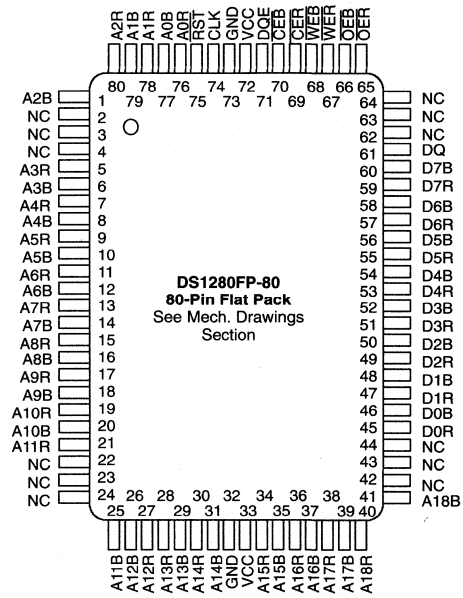
ORDERING INFORMATION

DS1280FP-XX	-80	80-pin Flat Pack
	-44	44-pin Flat Pack

PIN DESCRIPTION

$\overline{RST}$	–	Reset For Serial Port
DQ	–	Data Input/Output For Serial Port
CLK	–	Clock Input For Serial Port
DQE	–	Serial Port Active Output
$\overline{CEB}$	–	System Bus Enable
$\overline{OEB}$	–	System Bus Read Enable
$\overline{WEB}$	–	System Bus Write Enable
A0B-A18B	–	System Address Bus
D0B-D7B	–	System Data Bus
$\overline{CER}$	–	RAM Chip Enable
$\overline{WER}$	–	RAM Write Enable
$\overline{OER}$	–	RAM Output Enable
A0R-A18R	–	RAM Address Bus
D0R-D7R	–	RAM Data Bus
GND	–	Ground
V_{CC}	–	+5 Volts

PIN ASSIGNMENT



DESCRIPTION

The DS1280 adds a 3-wire serial port to a bytewide static RAM yet maintains the existing bytewide port. Memory capacity of up to 512K bytes can be addressed directly. Arbitration between the serial and bytewide port is accomplished by handshaking or using predictable idle time as an access window. The serial port requires a 6-byte protocol to set up memory transfers. Cyclic redundancy check circuitry is included to monitor serial data transmission for error.

PIN DESCRIPTION

$\overline{RST}$ – The 3-wire serial port selection signal input. When RST is low, all communications to the serial port are inhibited. When high, data is clocked into or out of the serial port.

CLK – The clock input signal is used to input or extract data from the 3-wire serial port. A clock cycle is defined as a falling edge followed by a rising edge. Data is driven out onto the 3-wire bus after a falling edge during read cycles and latched into the port on the rising edge during write cycles.

DQ – The DQ signal is the bidirectional data signal for the 3-wire serial port. Byte 0 bit 0 is the first bit input/output.

DQE – The DQE output signal is active (high level) whenever the 3-wire serial port is driving the DQ line. Therefore, this pin will be high whenever data is being read. Otherwise it will be low and the DQ line will be an input. This signal can be used as a means of tri-stating the DQ driver on the other end.

$\overline{CER}$ – Chip enable output to RAM. This signal is asserted active (low) during RAM read or write cycles. This signal is either derived from the system bus chip enable ($\overline{CEB}$) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

$\overline{WER}$ – Write enable output to RAM. This signal is asserted active (low) during RAM write cycles. This signal is either derived from the system bus write enable ($\overline{WEB}$) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

$\overline{OER}$ – Output enable to RAM. This signal is asserted active (low) during RAM read cycles. This signal is either derived from the system bus read enable ($\overline{OEB}$) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

A0R-A18R – Addresses supplied to RAM. These signals allow access to up to 512K bytes of RAM controlled by the DS1280. The addresses are either derived from the system address bus (A0B-A18B) or from the protocol and internal binary counter provided by the 3-wire serial port and associated timing circuits.

D0R–D7R – Data bus supplied to RAM. These eight signals comprise the bidirectional data bus between external bytewide RAM and the DS1280. This data bus is either derived from the system data bus (D0B-D7B) or from the protocol and data stream provided by the 3-wire serial port and associated timing circuits.

$\overline{CEB}$ – System bus chip enable to the DS1280. This signal is used to generate the RAM chip enable for transfer of data to and from the parallel system bus to RAM (68-pin package only).

$\overline{OEB}$ – System bus output enable (read) for transfer of data from RAM to the parallel system bus (68-pin package only).

$\overline{WEB}$ – System bus write enable to the DS1280. This signal is used to generate the RAM write enable for transfer of data from the parallel system bus to the RAM (68-pin package only).

A0B-A18B – System bus addresses to the DS1280. These signals are used to specify the address location for data transfer to and from RAM (68-pin package only).

D0B-D7B – System data bus to and from the DS1280. This bidirectional bus is used to carry data to and from the parallel system bus and RAM (68-pin package only).

Vcc – +5volt power from the DS1280 (2 pins).

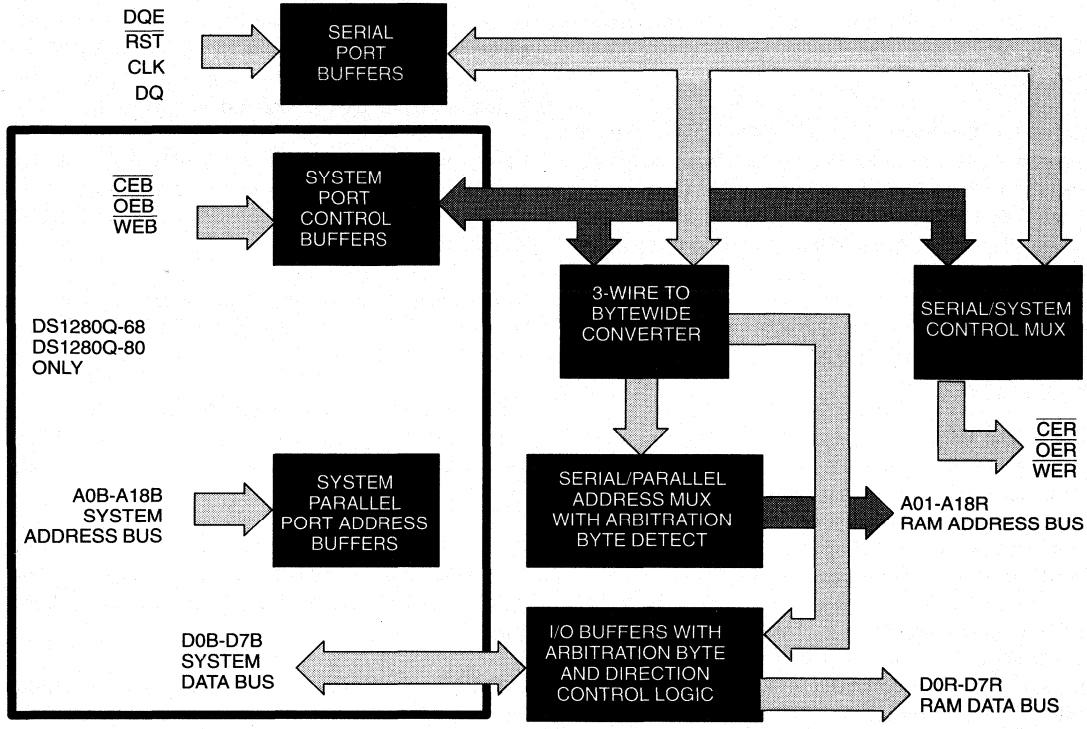
GND – Ground for the DS1280 (2 pins).

OPERATION

Figure 1 illustrates the main elements of the DS1280. As shown, the DS1280 has two major sections: a 3-wire to bytewide converter and a serial/parallel multiplexer. The source of the serial/parallel multiplexer is either a 3–wire serial port or a bytewide system bus. Arbitration of the serial/parallel multiplexer is controlled by signals from the 3-wire to bytewide converter. The 3-wire serial port, therefore, has priority in accessing the RAM and the methods used to avoid collisions are primarily directed by the 3-wire to bytewide converter.

8

DS1280 BLOCK DIAGRAM Figure 1



SYSTEM BYTEWIDE PARALLEL BUS

If the $\overline{RST}$ signal for the 3-wire serial port is low (inactive), the bytewide parallel port can access associated RAM directly. The bytewide parallel bus addresses (A0B-A18B) and control signals ($\overline{CEB}$, $\overline{OEB}$ and $\overline{WEB}$) are buffered by the DS1280 and become outputs A0R-A18R, $\overline{CER}$, $\overline{OER}$, and $\overline{WER}$ respectively, which are connected directly to RAM. The data input/output signals (D0B-D7B) are internally buffered and sent to RAM on the data input/output signals D0R-D7R. The buffering is designed to handle bidirectional data transfer. Data will be written from the bytewide parallel bus to RAM when $\overline{CEB}$ and $\overline{WEB}$ inputs are both active (low). The $\overline{OEB}$ signal is a "don't care" signal during a write cycle. Data is read from RAM via the byte wide parallel port when $\overline{CEB}$ and $\overline{OEB}$ signals are both low and $\overline{WEB}$ is high.

3-WIRE SERIAL BUS

If the RST signal for the 3-wire serial port is active (high), the 3-wire to bytewide converter controls the RAM through the control/address/data multiplexers. The 3-wire to bytewide converter uses a 56-bit protocol written serially using $\overline{RST}$, DQ, and CLK to determine the action required and also the starting address location in the RAM to be used. Data is entered into the 3-wire while $\overline{RST}$ is high on the low-to-high transition of the CLK signal provided the data is stable on the DQ line with the proper setup and hold times. The last eight bits of the 56-bit protocol are a cyclic redundancy check byte (CRC) that ensures that all bits of the protocol have been received correctly. If the 56 bits of protocol have not been received correctly, further action will be aborted. The CRC check byte can catch up to three single bit errors within the 56-bit protocol and can also be used on incoming and outgoing serial data streams to check the integrity of data being read or written. More discussion on CRC use and CRC generation will follow later in this text.

PROTOCOL: 3-WIRE SERIAL BUS

The 3-wire serial bus protocol can cause eight different actions to occur as shown in Table 1.

The organization of the 56-bit protocol is shown in Figure 2. As defined, the first byte of the protocol determines whether the action which is to occur involves a read or write. A read function is defined by the binary pattern 11101000. This pattern, therefore, applies to commands 1, 3, 5, and 6 of Table 1. A write function is defined by the binary pattern 00010111. This pattern, therefore, applies to commands 2, 4, 7, and 8 of Table 1. Any other pattern which is entered into the read/write field will cause further action to terminate. Additional differentiation as to which read or write command is determined by the last five bits of the third byte of the protocol called the command field. The control field bits are defined in Table 2 .

A burst read uses a 19-bit address field which consists of the second, third, and bits 0, 1, and 2 of the fourth byte of the protocol to determine the starting address of information to be read from RAM. The byte of data resident in that location is loaded into an 8-bit shift register within the DS1280. The byte of data is then transferred from the shift register to the 3-wire bus by driving the DQ line on the falling edge of the next eight clocks with the LSB first. A burst write uses the same 19-bit address field to determine the starting address of information to be written into RAM. Data is shifted from the DQ line of the 3-wire bus into an 8-bit shift register within the DS1280 on the next eight rising clock edges. After a byte is loaded, the data is written into the RAM location immediately after the rising edge of the eighth clock. Burst reads and writes will continue on a byte-by-byte basis, automatically incrementing the selected address by one location for each successive byte.

PROTOCOL COMMANDS Table 1

1. Burst read
2. Burst write
3. Read protocol select bits
4. Write protocol select bits
5. Burst read masking portions of the protocol select bits
6. Read CRC register
7. Set the address arbitration byte location
8. Poll arbitration byte for status and control

Termination of a current operation will occur at any time when $\overline{RST}$ is taken low. If a byte of data has been loaded into the shift register, a write cycle is allowed to finish, so corrupted data is not written into the RAM. If a full byte of data has not been loaded into the shift register when $\overline{RST}$ goes low, no writing occurs. Reads can be terminated at any point since there is no potential for corruption of data. The read CRC command provides a method for checking the integrity of data sent over the 3-wire bus. The CRC byte resides in the last byte (byte 6) of the protocol. The 8-bit CRC byte not only operates on the protocol bits as they are written in, but also on all data that is written or read from RAM.

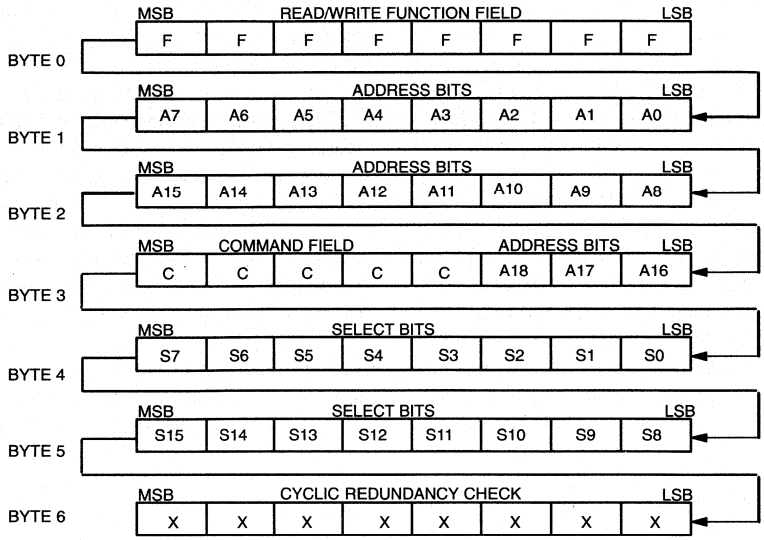
After a burst read or write has finished and $\overline{RST}$ has gone low, the final value of the CRC is stored in the DS1280. If a read CRC register command is issued, the stored CRC value is driven onto the DQ line by the first eight clock cycles after the protocol is received. The CRC value generated by the DS1280 should match exactly with the value generated in the host system which is transmitting or receiving data on the other end of the 3-wire bus. If it does not, data has been corrupted and a retransmission should occur. It should be noted that the CRC for the previous transaction can only be obtained if a read CRC command is issued immediately after $\overline{RST}$ goes low to reset the DS1280, then high to accept a read CRC command. If any other sequence is followed, an intermediate CRC will be generated and stored whenever $\overline{RST}$ goes low again, destroying the CRC value of interest. Generation of the CRC byte by the external unit on the 3-wire bus will be covered later in this data sheet.

COMMAND FIELD Table 2

00110	Burst read
10001	Burst write
00011	Read CRC register
10110	Set arbitration byte address to 00000 or 7FFFF
01001	Poll arbitration byte for access to RAM
00101	Read protocol select bits
01110	Write protocol select bits
11XXX	Burst read masking portions of the select bits

8

PROTOCOL Figure 2



In any 2-port system there is a potential for access collisions. To solve this problem, an arbitration byte is provided so that the serial and parallel ports of the DS1280 can determine the status of the other port. A special byte in RAM address space is reserved to allow for handshaking between the two ports. This arbitration byte has a special attribute in that it is simultaneously accessible by both ports.

Two commands are used by the 3-wire serial port protocol to manage the arbitration byte. First, since this byte will create a hole in RAM address space for the parallel bytewide port, a command is added to move the arbitration byte to either address location "00000" or address location "7FFFF." When setting the arbitration byte address location, the correct read/write field and command field must be entered along with all zeroes or all ones in the address field. It is important to note that the arbitration byte is located in the parallel memory location assigned by the serial port using the appropriate commands. However, the physical byte of RAM is located within the DS1280. The existence of this physical byte is transparent to the bytewide parallel port and looks like normal RAM space with some read/write restriction. However, the serial port can still address the actual RAM location at either 00000 or 7FFFF in addition to accessing the arbitration byte.

The second command used by the 3-wire serial port provides for polling of the arbitration byte to determine the status of the parallel port. In addition, the arbitration byte can be set to indicate to the parallel port that the serial port is taking over the RAM. The second command protocol allows the serial port to do a compressed read-write-read operation that causes the arbitration byte to be read by the first eight clocks following the protocol. The next eight clocks cause data to be written into the arbitration byte, and the last eight clock cycles allow for a second read of the data for verification. The 24 cycles occur by entering the 56-bit protocol only once. The protocol pattern entered is a write function in the read/write field (00010111) and the correct command field.

SELECT BITS

Three other commands are used to set the select bits in the protocol. Once the select bits are set to a binary value they must be matched exactly when protocol is sent or further activity is prevented. The bits allow for 65,536 different binary combinations. Therefore, multiple DS1280s can be connected on the same serial bus and only the appropriate device will respond. To write the select bits, a write function in the read/write field is required along with the appropriate command in the command field.

To read the select bits, a read cycle in the read/write field is required along with the appropriate command in the command field. The arrangement of reading and writing select bits allows the user to have multiple DS1280s in

use and uniquely identify each. A read can occur successfully without knowing the select bits but a write cannot occur without matching the current select field.

A third command masking specific select bits provides a means for determining the identity of a specific DS1280 when more than one is used. A read in the read/write field and a "11000" in the command field will execute a mask read that ignores all select bits to determine the presence of one or more DS1280s. With the detection of at least one device, a search can begin by masking all but a single pair of DS1280 select bits. A read in the read/write field and a "11001" in the command field will unmask the first two LSBs of byte 4 of the select bits (see Figure 3). With these two select bits unmasked, only an exact match of four possible combinations of these two select bits will allow access through the 3-wire port to RAM. The combinations are 00, 01, 10, and 11. Therefore, repeating the unmasking of the first two bits of the select field up to four times will give the binary value of these select bits.

Having determined the first two select bits, the next two select bits can be unmasked, and the process of matching one of four combinations can proceed as before. Repetition of unmasking select bit pairs will yield an exact match of 65,536 possible DS1280s in no more than 32 attempts.

ARBITRATION

As mentioned earlier, one byte of RAM has been reserved for arbitration between the 3-wire port and the bytewide parallel bus. The location of this byte within the memory map will be at address 00000 or at address 7FFFF as determined by the protocol input from the 3-wire serial port. The arbitration byte has special restrictions and disciplines so that the 3-wire serial bus and the bytewide parallel bus are never in contention for RAM access. This byte is shown in Figure 4.

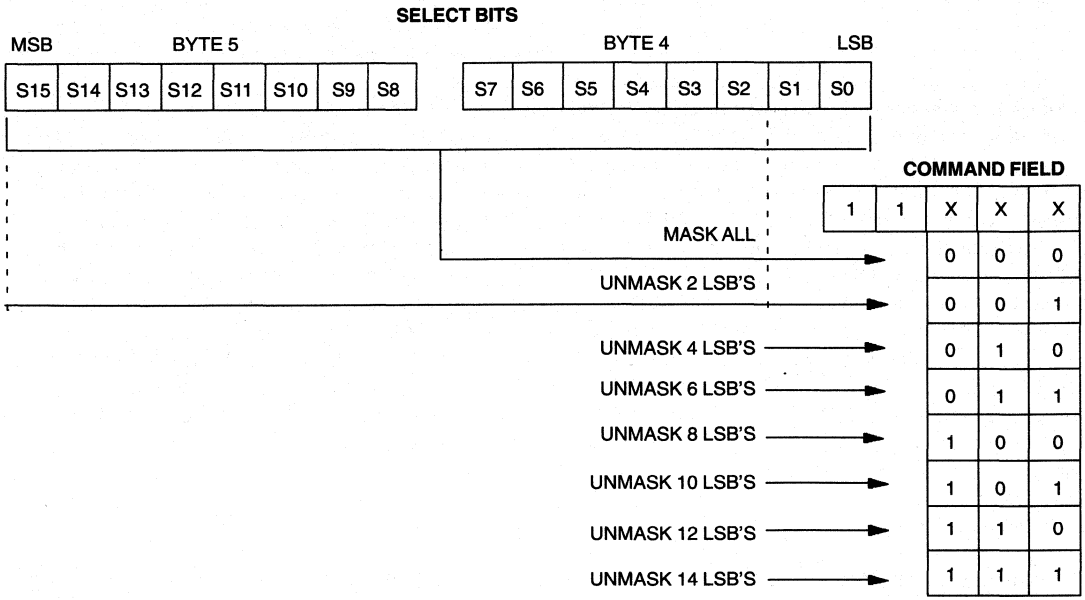
As defined, the 3-wire serial port can read the whole byte but can only write bits S2-S0. The bytewide parallel port can read the whole byte but can only write bits B1-B0. An internal counter controls bits C2-C0 that cannot be written by either port. Arbitration is accomplished when the status bits are read and written by the respective ports. If the 3-wire serial port wants to access RAM, the arbitration byte should be polled by the serial port until bit B1 equals zero. If B1 equals zero, the 3-wire serial port should then write a one into bit S2. After the write of bit S2, the 3-wire serial port should then read the arbitration byte to confirm that B1=0 and S2=1. This operation must be executed with the protocol for the compressed read/write/read sequence which minimizes overhead.

The 3-wire serial port should always abort any attempt to access RAM if B1 equals one. When the 3-wire serial port completes any transfer of data to or from RAM, bit S2 should be written back to zero so that the bytewide parallel port will know that the 3-wire serial port is not using the RAM. The bytewide serial bus can gain access to RAM by polling the arbitration byte until S2 bit equals zero. When S2 equals zero, the bytewide parallel port then writes a one into bit B1. A read cycle verifying that S2 equals zero and B1 equals one confirms that the bytewide parallel port has access to RAM. The bytewide parallel port can then read or write RAM as required. When the entire transaction is complete, the bytewide parallel port should write the B1 bit to zero, signaling the 3-wire serial port that the RAM is not in use.

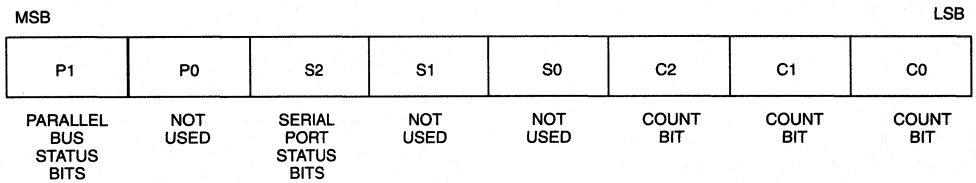
The bits B0, S1, and S0 can be defined by the user to pass additional arbitration information, making possible more elaborate handshaking schemes between the two ports. Some typical uses for these bits could be an indication that a port desires access to RAM or the amount of RAM written. Another method of arbitration between the 3-wire serial port and the bytewide parallel bus is the use of the count bits C0-C2. The 3-wire port reads or writes from RAM only once every eight clock cycles. This action occurs when the internal byte counter transitions from a "111" state to a "000" state. The access occurs regardless of the arbitration byte status bits. C0-C2 are updated as the internal serial bit counter is incremented. The bytewide port can execute reads or writes depending on the status of C0-C2. These bits indicate the number of bits the 3-wire serial port has loaded and, therefore, indicate when a read or write will occur from the 3-wire port.

Since the 3-wire port always reads or writes at the ends of a byte (C0-C2 = 1) the bytewide parallel bus should never access RAM if the count bits read all ones. The bytewide parallel port can determine the minimum time left before the 3-wire serial port will access the memory from the count bits and the minimum clock cycle applied to the 3-wire clock input. Essentially the 3-wire serial port is given priority on access to RAM and the bytewide parallel port determines when it can access the RAM to avoid colliding with the 3-wire serial port.

SELECT BITS MASK Figure 3



ARBITRATION BYTE Figure 4



CRC GENERATION

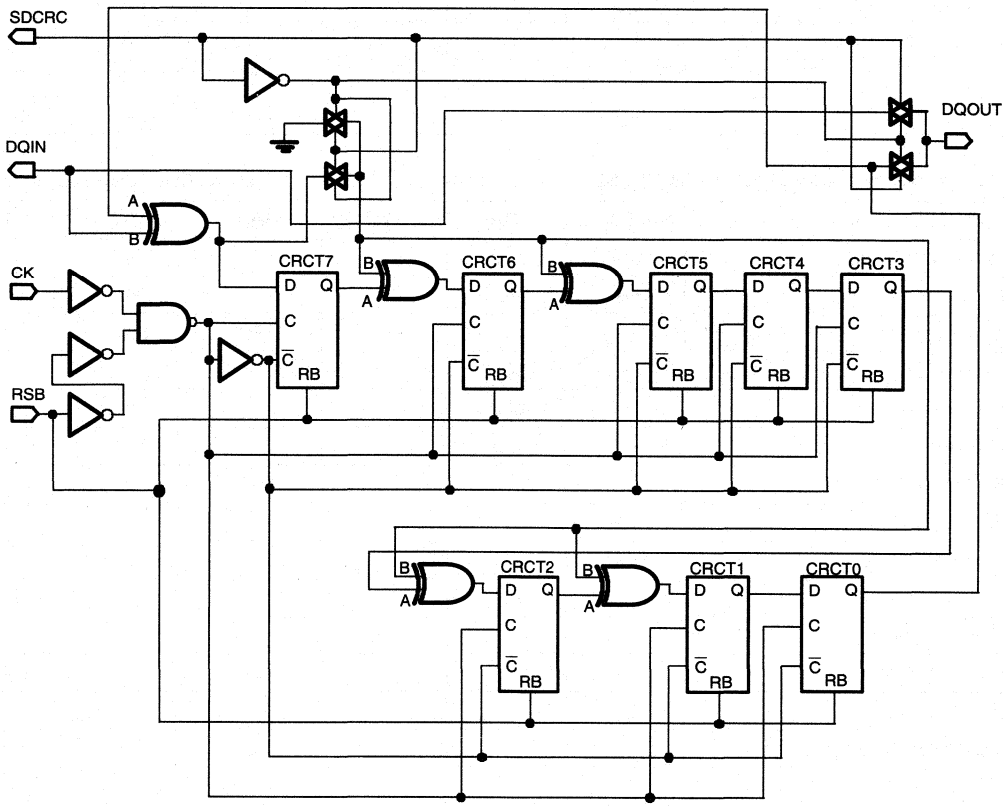
The logic involved in CRC generation is shown in Figure 5. It is comprised of an 8-bit shift register, four exclusive OR gates, and two sets of transmission gates. The transmission gates serve to divert data from DQIN to the CRC generator while each byte is being assembled and, at the same time, output data to the output (DQ OUT). When input select CRC (SDCRC) is driven to an active level (high), data is output at DQOUT from the CRC generator using the clock input (CK) in the same manner as described earlier for operation of the 3-wire serial bus.

The reset signal (RSB) must be high while the CRC generator is being used, as an inactive state will disable the 8-bit shift register. This signal is the same as the reset described for the 3-wire serial bus. A CRC generator for serial port communications can be constructed as described above to satisfy the DS1280 CRC requirements. However, another approach is to generate the CRC using software. An example of how this is accomplished using assembly language follows. This assembly language code is written for the DS5000 Soft Microcontroller. The assembly language procedure DO CRC given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to calculate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and DO CRC is called to update the CRC. After all the data has been passed to DO CRC, the variable CRC will contain the result.

CRC GENERATION LOGIC Table 3

```
DO_CRC:
        PUSH    ACC             ; Save the Accumulator
        PUSH    B               ; Save the B register
        PUSH    ACC             ; Save bits to be shifted
        MOV     B,      #8      ; Set to shift eight bits
CRC_LOOP:
        XRL     A,      CRC     ; Calculate DQIN xor CRCTO
        RRC     A               ; Move it to the last
        MOV     A,      CRC     ; Get the last CRC value
        JNC     ZERO            ; Skip if DQIN xor CRCTO = 0
        XRL     A,      #0CCH   ; Update the CRC value
ZERO:
        RRC     A               ; Position the new CRC
        MOV     CRC,    A       : Store the new CRC
        POP     ACC             : Get the remaining bits
        RR      A               ; Position next bit in LSB
        PUSH    ACC             ; Save the remaining bits
        DJNZ    B,      CRC_LOOP ; Repeat for eight bits
        POP     ACC             ; Clean up the stack
        POP     B               ; Restore the B register
        POP     ACC             ; Restore the Accumulator
        RET                     ; Return
```

CRC GENERATION Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to+125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A=0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply	V_{CC}	3.25	5.0	6.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3V	V	
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(t_A=0°C to 70°C ; V_{CC}=+5V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		+1	µA	9
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}	+2			mA	
Supply Current	I_{CC1}			15	mA	2
Supply Current	I_{CC2}			50	mA	3

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±10%; 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	4
Data to CLK Hold	t_{CDH}	40			ns	4
Data to CLK Delay	t_{CDD}			125	ns	4,5,6
CLK Low Time	t_{CL}	500			ns	4
CLK High Time	t_{CH}	500			ns	4
CLK Frequency	f_{CLK}	DC		1	MHz	4,10
CLK Rise & Fall Time	$t_R t_F$			100	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	4
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	4
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	4
$\overline{RST}$ to D/Q High Z	t_{CDZ}			50	ns	4,6
Serial Port Active	t_{DI}			25	ns	4,6
Serial Port Inactive	t_{DI}			25	ns	4,6
Parallel Port Propagation	t_{PD}		12	20	ns	4,6,8

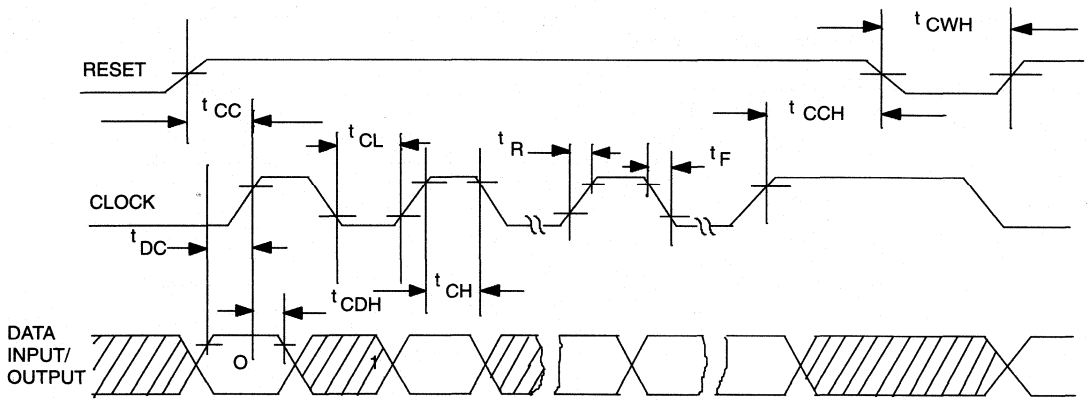
CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			15	pF	

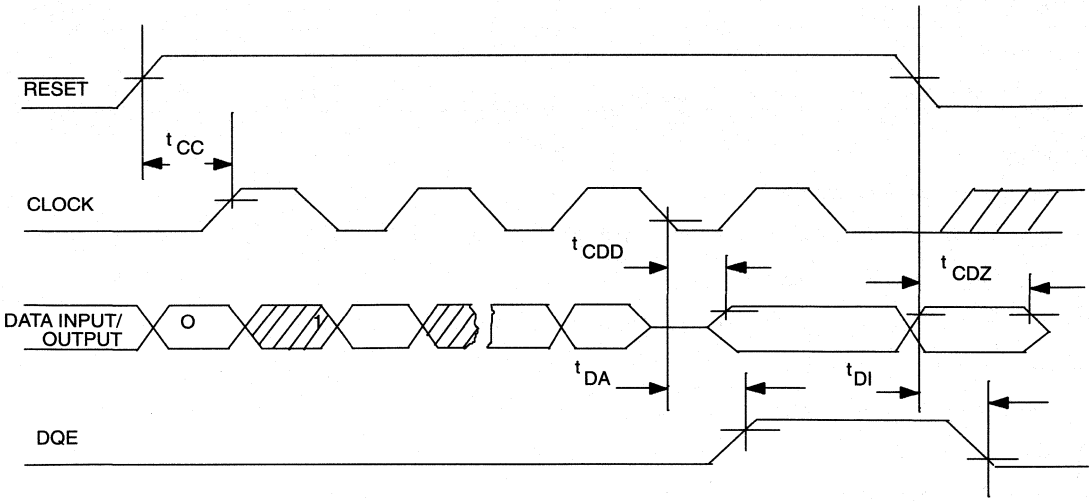
NOTES:

1. All voltages are referenced to ground.
2. I_{CC1} is measured with all outputs open and both the 3-wire serial port or the bytewide parallel port inactive.
3. I_{CC2} is measured with all outputs open.
4. Measured at V_{IH} = 2.0 V or V_{IL} = 0.8V and 10ns maximum rise and fall time.
5. Measured at V_{OH}= 2.4 V and V_{OL} = 0.4V.
6. Measured with a load capacitance of 50 pF.
7. The 3-wire serial port will correctly read and write any static RAM with an effective access time of 200ns.
8. Propagation delay is the same for data going either way on the bytewide parallel bus.
9. Pins A0B through A18B, $\overline{RST}$, DQ, $\overline{CEB}$ have pulldown resistors which will leak approximately 50 µA.
10. Arbitration byte must be accessed at a maximum clock frequency of 500 KHz with a symmetrical waveform.

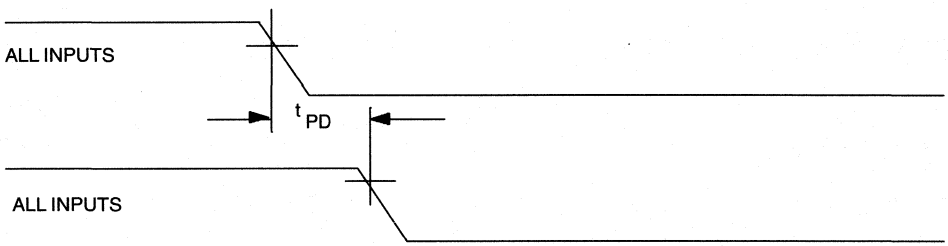
TIMING DIAGRAM: WRITE DATA TRANSFER 3-WIRE SERIAL PORT (7)



TIMING DIAGRAM: READ DATA TRANSFER 3-WIRE SERIAL PORT (7)



PROPAGATION DELAY: DATA TRANSFER: BYTEWIDE PARALLEL DATA BUS (8)



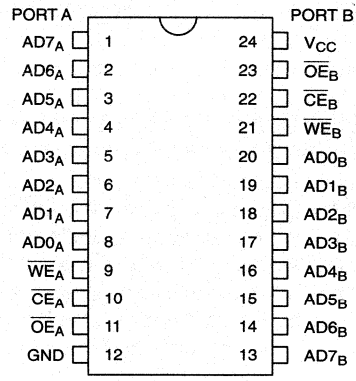
DALLAS SEMICONDUCTOR

DS1609
Dual Port RAM

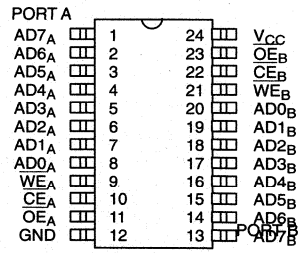
FEATURES

- Totally asynchronous 256 byte dual port memory
- Multiplexed address and data bus keeps pin count low
- Dual port memory cell allows random access with minimum arbitration
- Each port has standard independent RAM control signals
- Fast access time
- Low power CMOS design
- 24–pin DIP or 24–pin SOIC surface mount package
- Both CMOS and TTL compatible
- Reduced performance operation down to 2.5 volts
- Operating temperature of -40°C to +85°C
- Standby current of 100 nA @ 25°C makes the device ideal for battery backup or battery operate applications.

PIN ASSIGNMENT



DS1609
24–PIN DIP (600 MIL)
See Mech. Drawings Section



DS1609S
24–PIN SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

AD0-AD7	–	Port address/data
$\overline{CE}$	–	Port enable
$\overline{WE}$	–	Write enable
$\overline{OE}$	–	Output enable
V_{CC}	–	+5 volt supply
GND	–	Ground

DESCRIPTION

The DS1609 is a random access 256 byte dual port memory designed to connect two asyncronous address/data buses together with a common memory element. Both ports have unrestricted access to all 256 bytes of memory and with modest system discipline no arbitration is required. Each port is controlled by three control signals: output enable, write enable, and port enable. The device is packaged in plastic 24–pin DIP and 24–pin SOIC. Output enable access time of 50 ns is available when operating at 5 volts. Reduced perform-

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ance operation at reduced voltage can be achieved down to 2.5 volts.

OPERATION – READ CYCLE

The main elements of the dual port RAM are shown in Figure 1.

A read cycle to either port begins by placing an address on the multiplexed bus pins AD0 - AD7. The port enable control ($\overline{CE}$) is then transitioned low. This control signal causes address to be latched internally. Addresses can be removed from the bus provided address hold time is met. Next, the output enable control ($\overline{OE}$) is transitioned low, which begins the data access portion of the read cycle. With both $\overline{CE}$ and $\overline{OE}$ active low, data will appear valid after the output enable access time t_{OEA}. Data will remain valid as long as both port enable and output enable remains low. A read cycle is terminated with the first occurring rising edge of either $\overline{CE}$ or $\overline{OE}$. The address/data bus will return to a high impedance state after time t_{CEZ} or t_{OEZ} as referenced to the first occurring rising edge. $\overline{WE}$ must remain high during read cycles.

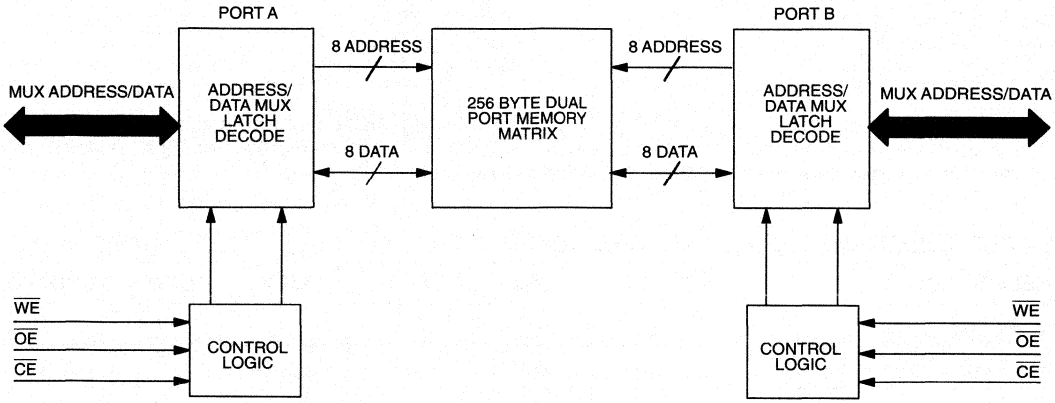
OPERATION – WRITE CYCLE

A write cycle to either port begins by placing an address on the multiplexed bus pins AD0 - AD7. The port enable control ($\overline{CE}$) is then transitioned low. This control signal causes address to be latched internally. As with a read cycle, the address can be removed from the bus provided address hold time is met. Next the write enable control signal ($\overline{WE}$) is transitioned low which begins the write data portion of the write cycle. With both $\overline{CE}$ and $\overline{WE}$ active low the data to be written to the selected memory location is placed on the multiplexed bus. Provided that data setup (t_{DS}) and data hold (t_{DH}) times are met, data is written into the memory and the write cycle is terminated on the first occurring rising edge of either $\overline{CE}$ or $\overline{WE}$. Data can be removed from the bus as soon as the write cycle is terminated. $\overline{OE}$ must remain high during write cycles.

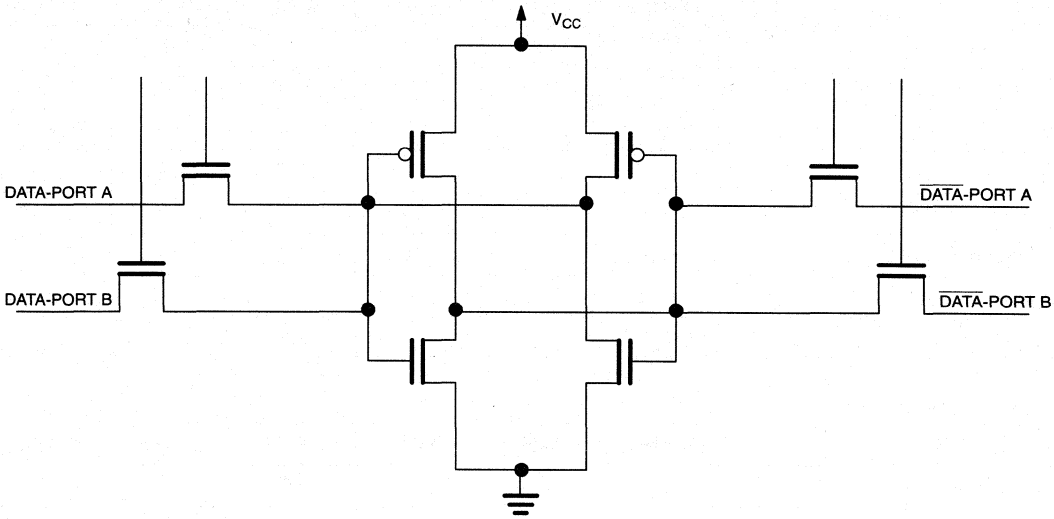
ARBITRATION

The DS1609 dual port RAM has a special cell design that allows for simultaneous accesses from two ports (see Figure 2). Because of this cell design, no arbitration is required for read cycles occurring at the same instant. However, an argument for arbitration can be made for reading and writing the cell at the exact same instant or for writing from both ports at the same instant. If a write cycle occurs while a read cycle is in progress, the read cycle will likely recover either the old data or new data and not some combination of both. However, the write cycle will update the memory with correct data. Simultaneous write cycles to the same memory location pose the additional concern that the cell may be in contention causing a metastable state. Depending on the timing of the write cycles of port A and port B, the memory location could be left containing the data written from port A or the data from port B or some combination thereof. However, both concerns expressed above can be eliminated by disciplined system software design. A simple way to assure that read/write conflicts don't occur is to perform redundant read cycles. Write/write arbitration needs can be avoided by assigning groups of addresses for write operation to one port only. Groups of data can be assigned check sum bytes which would guarantee correct transmission. A software arbitration system using a "mail box" to pass status information can also be employed. Each port could be assigned a unique byte for writing status information which the other port would read. The status information could tell the reading port if any activity is in progress and indicate when activity is going to occur.

BLOCK DIAGRAM: DUAL PORT RAM Figure 1



DUAL PORT MEMORY CELL Figure 2



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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC} + 0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Impedance	Z_{IN}	50K			Ω	2
$\overline{CE}$, $\overline{WE}$, $\overline{OE}$ Leakage	I_{LO}	-1.0		+1.0	µA	
Standby Current	I_{CCS1}		3.0	5.0	mA	3, 4, 13
Standby Current	I_{CCS2}		50	300	µA	3, 5, 13
Standby Current	I_{CCS3}		100		nA	3, 6, 13
Operating Current	I_{CC}		18	30	mA	7, 13
Logic 1 Output	V_{OH}	2.4			V	8
Logic 0 Output	V_{OL}			0.4	V	9

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
I/O Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	5			ns	
Address Hold Time	t_{AH}	25			ns	
Output Enable Access	t_{OEA}	0		50	ns	10
$\overline{OE}$ to High Z	t_{OEZ}	0		20	ns	
$\overline{CE}$ to High Z	t_{CEZ}	0		20	ns	
Data Setup Time	t_{DS}	0			ns	
Data Hold Time	t_{DH}	10			ns	
Write Pulse Width	t_{WP}	50			ns	11
$\overline{CE}$ Recovery Time	t_{CER}	20			ns	12
$\overline{WE}$ Recovery Time	t_{WER}	20			ns	12
$\overline{OE}$ Recovery Time	t_{OER}	20			ns	12
$\overline{CE}$ to $\overline{OE}$ Setup Time	t_{COE}	25			ns	
$\overline{CE}$ to $\overline{WE}$ Setup Time	t_{CWE}	25			ns	

AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; V_{CC} = 2.5V – 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	5			ns	
Address Hold Time	t_{AH}	25			ns	
Output Enable Access	t_{OEA}	0		100	ns	10
$\overline{OE}$ to High Z	t_{OEZ}	0		20	ns	
$\overline{CE}$ to High Z	t_{CEZ}	0		20	ns	
Data Setup Time	t_{DS}	0			ns	
Data Hold Time	t_{DH}	10			ns	
Write Pulse Width	t_{WP}	100			ns	11
$\overline{CE}$ Recovery Time	t_{CER}	20			ns	12
$\overline{WE}$ Recovery Time	t_{WER}	20			ns	12
$\overline{OE}$ Recovery Time	t_{OER}	20			ns	12
$\overline{CE}$ to $\overline{OE}$ Setup Time	t_{COE}	25			ns	
$\overline{CE}$ to $\overline{WE}$ Setup Time	t_{CWE}	25			ns	

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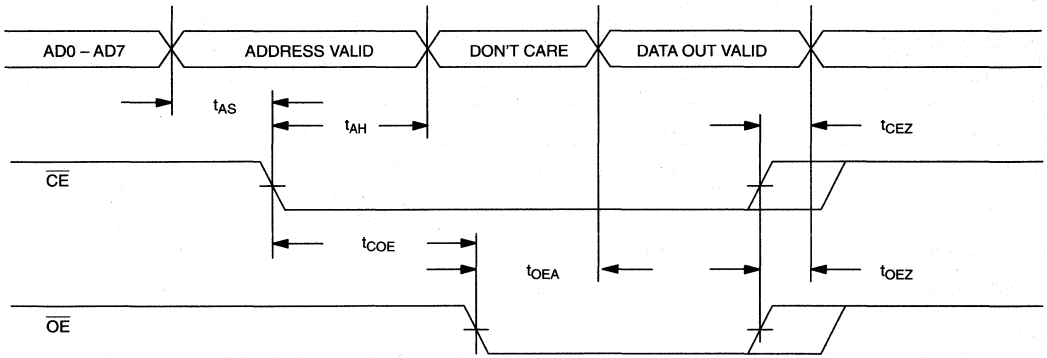
DUAL PORT RAM TIMING: READ CYCLE

DURING READ CYCLE $\overline{WE} = V_{IH}$

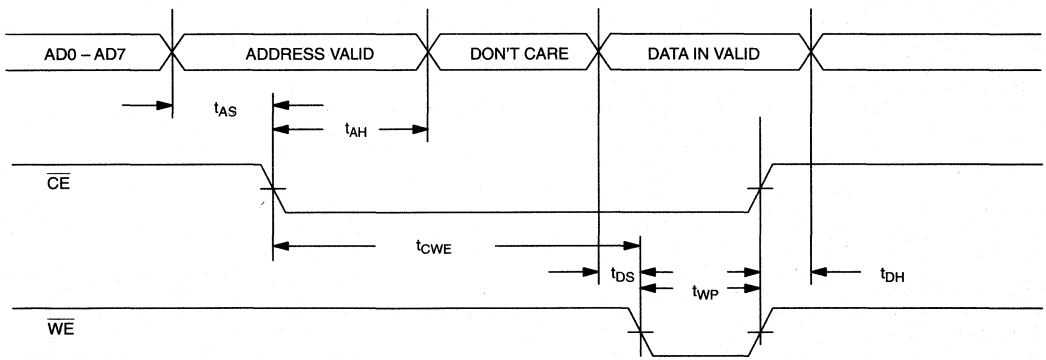


NOTES:

1. During read cycle the address must be off the bus prior to t_{OEA} minimum to avoid bus contention.
2. Read cycles are terminated by the first occurring rising edge of $\overline{OE}$ or $\overline{CE}$.

DUAL PORT RAM TIMING: WRITE CYCLE

DURING WRITE CYCLE $\overline{OE} = V_{IH}$



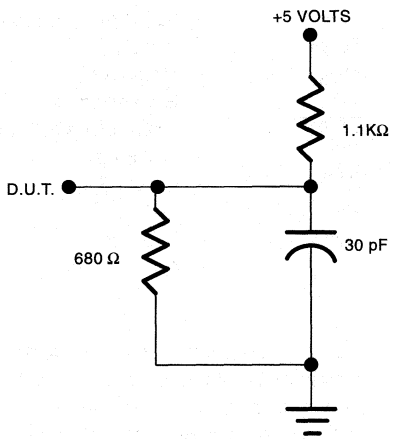
NOTE:

1. Write cycles are terminated by the first occurring edge of $\overline{WE}$ or $\overline{CE}$.

NOTES:

1. All Voltages are referenced to ground.
2. All pins other than $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, V_{CC} and ground are continuously driven by a feedback latch in order to hold the inputs at one power supply rail or the other when an input is tristated. The minimum driving impedance presented to any pin is 50KΩ. If a pin is at a logic low level, this impedance will be pulling the pin to ground. If a pin is at a logic high level, this impedance will be pulling the pin to V_{CC}.
3. Standby current is measured with outputs open circuited.
4. I_{CCS1} is measured with all pins within 0.3V of V_{CC} or GND and with $\overline{CE}$ at a logic high or logic low level.
5. I_{CCS2} is measured with all pins within 0.3V of V_{CC} or ground and with $\overline{CE}$ within 0.3V of V_{CC}.
6. I_{CCS3} is measured with all pins at V_{CC} or ground potential and with $\overline{CE} = V_{CC}$. Note that if a pin is floating, the internal feedback latches will pull all the pins to one power supply rail or the other.
7. Active current is measured with outputs open circuited, and inputs swinging full supply levels with one port reading and one port writing at 100 ns cycle time. Active currents are a DC average with respect to the number of 0's and 1's being read or written.
8. Logic one voltages are specified at a source current of 1 mA.
9. Logic zero voltages are specified at a sink current of 4 mA.
10. Measured with a load as shown in Figure 3.
11. t_{WP} is defined as the time from $\overline{WE}$ going low to the first of the rising edges of $\overline{WE}$ and $\overline{CE}$.
12. Recovery time is the amount of time control signals must remain high between successive cycles.
13. Typical values are at 25°C.

LOAD SCHEMATIC Figure 3



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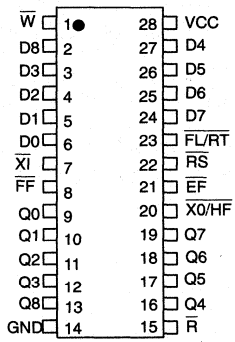
DALLAS SEMICONDUCTOR

DS2009
512 x 9 FIFO Chip

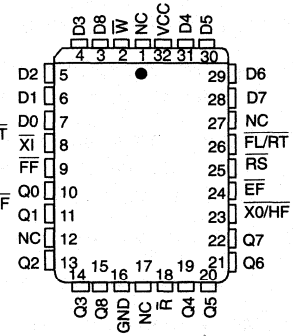
FEATURES

- First-in, first-out memory-based architecture
- Flexible 512 x 9 organization
- Low-power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 35 ns, 50 ns, 65 ns, 80 ns, and 120 ns access times
- Optional industrial temperature range -40°C to +85°C available, designated N

PIN ASSIGNMENT



28-Pin DIP(300 and 600 Mil)
See Mech. Drawings Section



32-Pin PLCC
See Mech. Drawings Section

PIN DESCRIPTION

$\overline{W}$	–	WRITE
$\overline{R}$	–	READ
$\overline{RS}$	–	RESET
$\overline{FL/RT}$	–	First Load/Retransmit
D_{0-8}	–	Data In
Q_{0-8}	–	Data Out
$\overline{XI}$	–	Expansion In
$\overline{XO/HF}$	–	Expansion Out/Half Full
$\overline{FF}$	–	Full Flag
$\overline{EF}$	–	Empty Flag
V_{CC}	–	5 Volts
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS2009 512 x 9 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The main application of the DS2009 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a first-in, first-out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

OPERATION

Unlike conventional shift register-based FIFOs, the DS2009 employs a memory-based architecture wherein a byte written into the device does not ripple through. Instead, a byte written into the DS2009 is stored at a specific location where it remains until over-written. The byte can be read and re-read as often as desired.

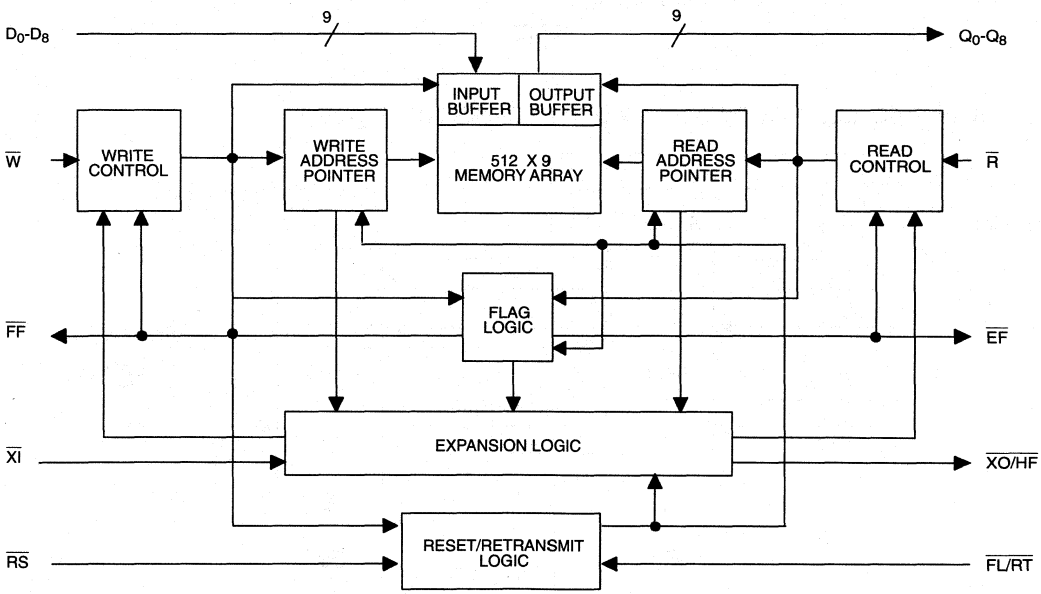
Twin address pointers (ring counters) automatically generate the address required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading unwritten bytes (reading while empty) or over-writing unread bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

Address pointers automatically loop back to address zero after reaching address 511. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The DS2009 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the DS2009 can connect the read, write, data in, and data out lines of the DS2009 in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion in and expansion out pins as appropriate (see the "Expansion Timing" section for a more complete discussion).

BLOCK DIAGRAM Figure 1



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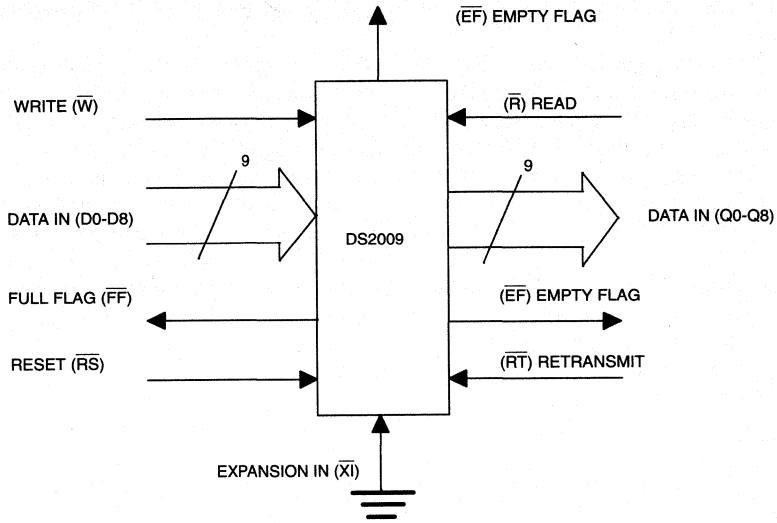
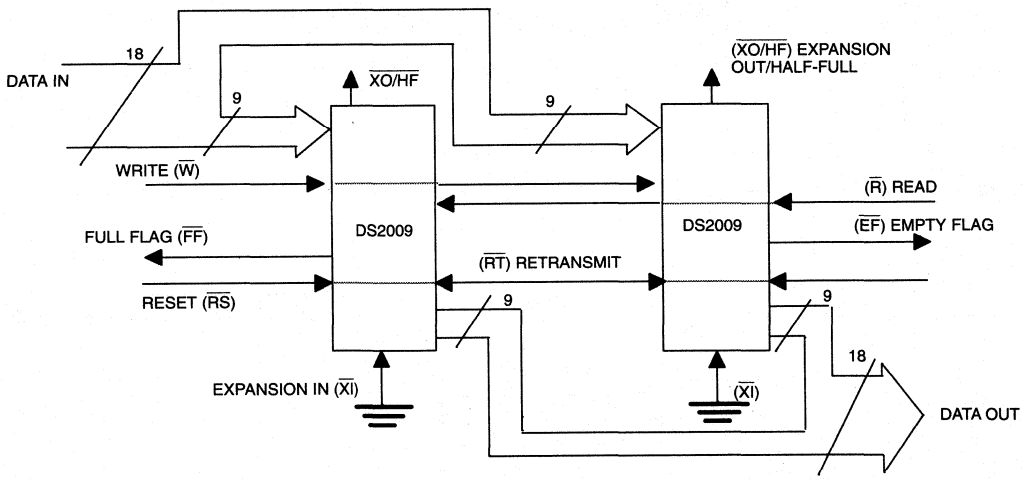
SINGLE DEVICE CONFIGURATION

A single DS2009 can be used when application requirements are for 512 words or less. The DS2009 is placed in single device configuration mode when the chip is reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 2).

A SINGLE 512 X 9 FIFO CONFIGURATION Figure 2



A 512 X 18 FIFO CONFIGURATION (WIDTH EXPANSION) Figure 3



NOTE:

Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (DAISY CHAIN)

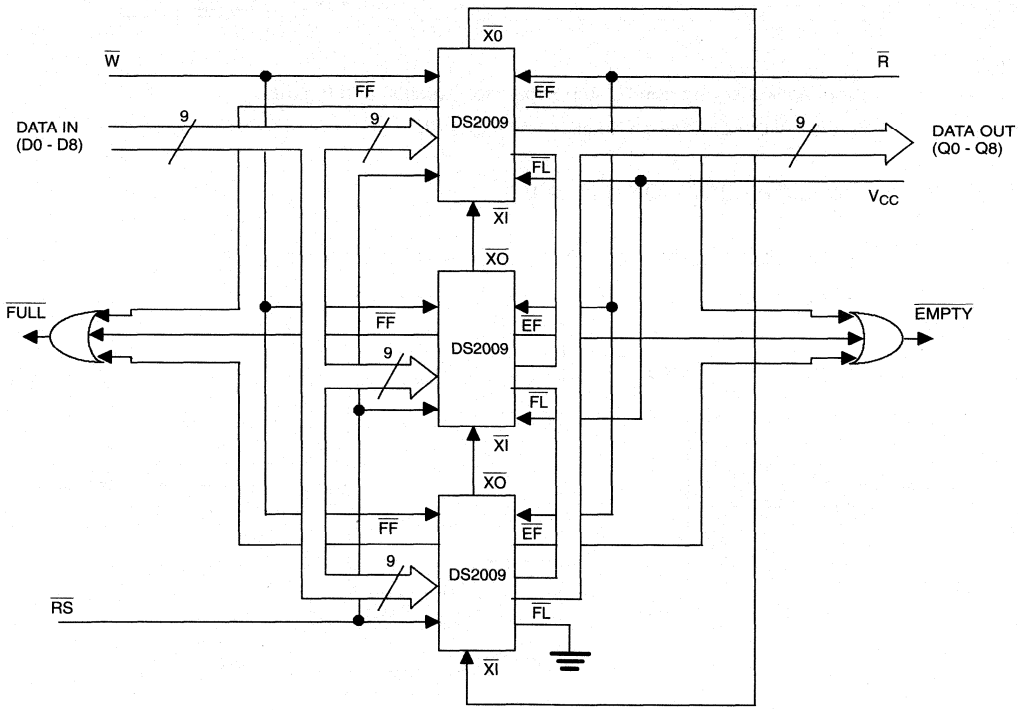
The DS2009 can easily be adapted to applications where more than 512 words are required. Figure 4 demonstrates depth expansion using three DS2009s. Any depth can be attained by adding DS2009s.

External logic is needed to generate a composite full flag and empty flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The DS2009 operates in the depth expansion configuration after the chip is reset under the following conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The retransmit function is not allowed in the depth expansion mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The half-full capability is not allowed in depth expansion.

A 1536 X 9 FIFO CONFIGURATION (DEPTH EXPANSION) Figure 4



COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 5).

BIDIRECTIONAL APPLICATIONS

Bidirectional applications that require data buffering between two systems (each system capable of read and write operations) can be achieved by pairing DS2009s as shown in Figure 6. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion can be used in this mode.

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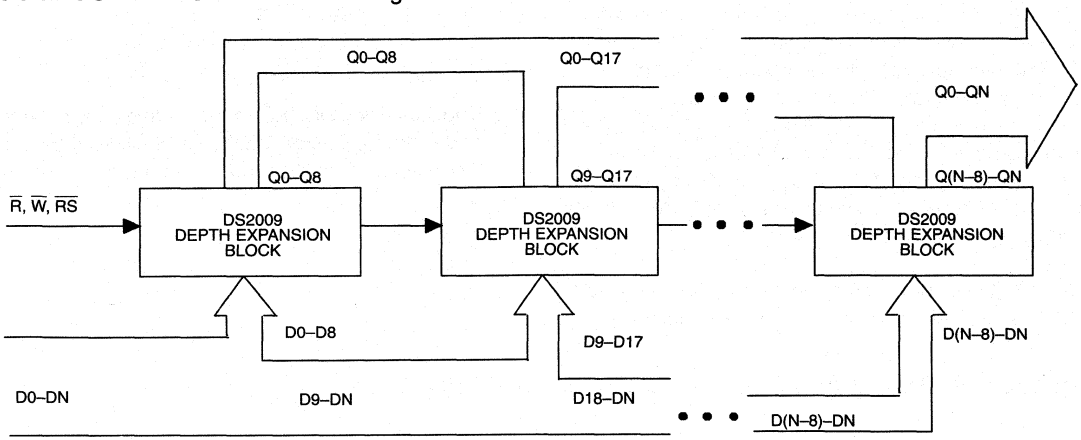
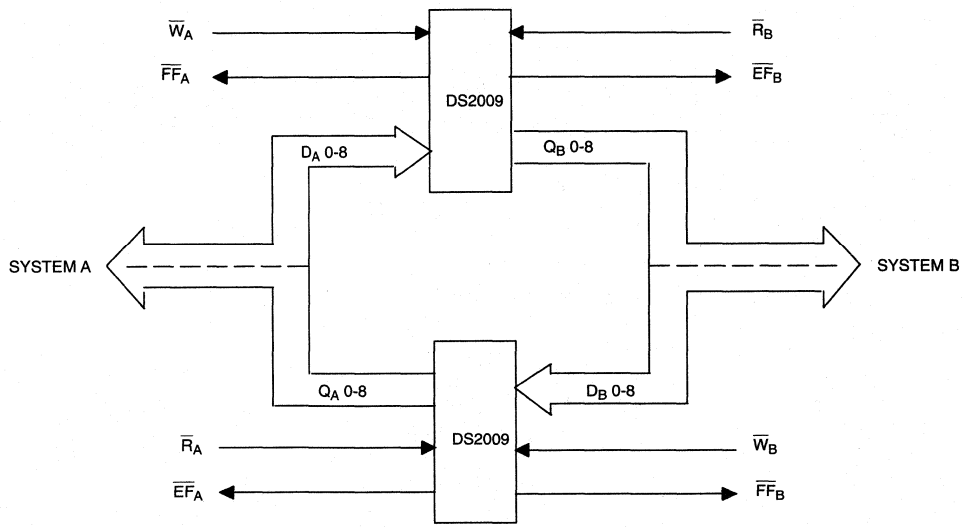
COMPOUND FIFO EXPANSION Figure 5



NOTES:

1. For depth expansion block diagram see "Depth Expansion" section and Figure 4.
2. For flag operation see "Width Expansion" section and Figure 3.

BIDIRECTIONAL FIFO APPLICATION Figure 6



HALF-FULL CAPABILITY

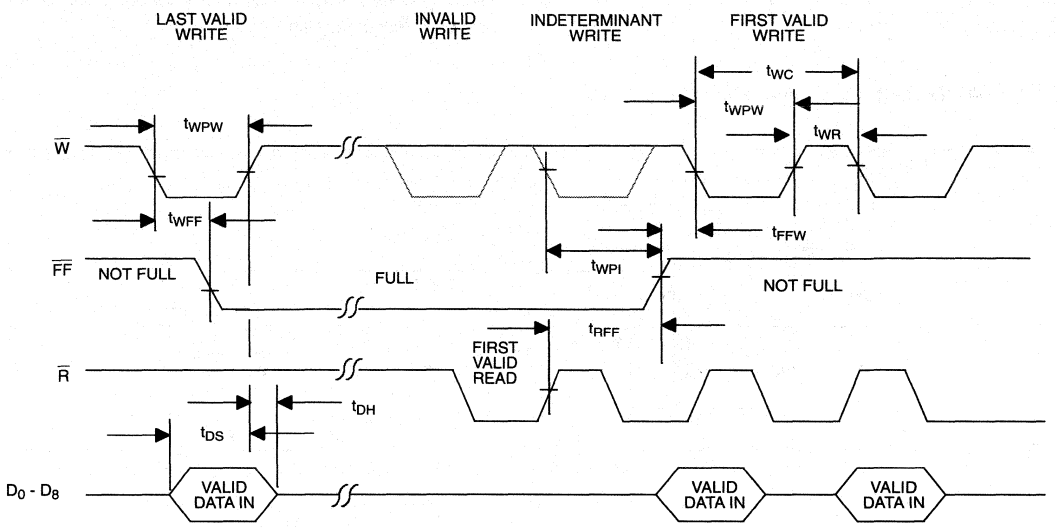
In the single-device and width-expansion modes, the $\overline{XO/HF}$ output acts as an indication of a half-full memory. ($\overline{XI}$ must be tied low.) After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain low until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The half-full flag is then reset (forced high) by the rising edge of the read operation.

WRITE MODE

The DS2009 initiates a write cycle (see Figure 7) on the falling edge of the write enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data setup

and hold time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing read operations. $\overline{FF}$ is asserted during the last valid write as the DS2009 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid read operation. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

WRITE AND FULL FLAG TIMING Figure 7



WRITE AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**NOTES**
Write Cycle Time	t_{WC}	45		65		80		100		140		ns	
Write Pulse Width	t_{WPW}	35		50		65		80		120		ns	1
Write Recovery Time	t_{WR}	10		15		15		20		20		ns	
Data Setup Time	t_{DS}	15		20		25		30		40		ns	
Data Hold Time	t_{DH}	5		5		10		10		10		ns	
$\overline{W}$ Low to $\overline{FF}$ Low	t_{WFF}		30		45		60		70		110	ns	2
$\overline{FF}$ High to Valid Write	t_{FFW}		5		5		10		10		10	ns	2
$\overline{R}$ High to $\overline{FF}$ High	t_{RFF}		30		45		60		70		110	ns	2
Write Protect Indeterminate	t_{WPI}		15		20		25		25		35	ns	2

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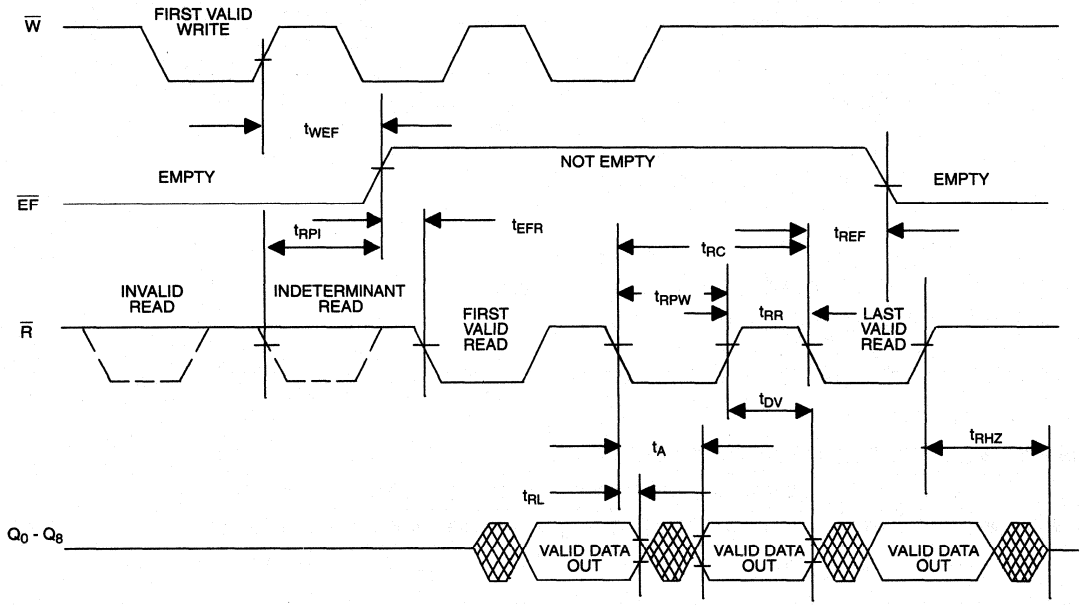
READ MODE

The DS2009 initiates a read cycle (see Figure 8) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the read mode of operation, the DS2009 provides fast access to data from 9 of 4608 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing write operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid write operation. Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

READ AND EMPTY FLAG TIMING Figure 8



READ AC ELECTRICAL CHARACTERISTICS

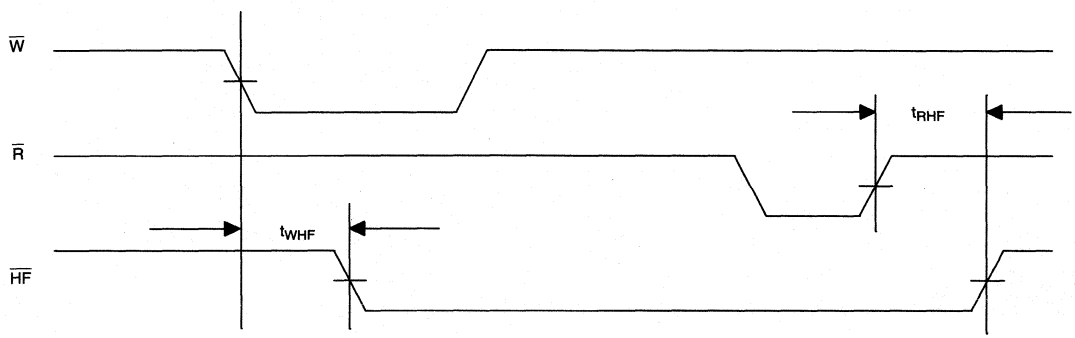
(0°C to 70°C; V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009–120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**NOTES**
Read Cycle Time	t_{RC}	45		65		80		100		140		ns	
Access Time	t_A		35		50		65		80		120	ns	1
Read Recovery Time	t_{RR}	10		15		15		20		20		ns	
Read Pulse Width	t_{RPW}	35		50		65		80		120		ns	1
$\overline{R}$ Low to Low Z	t_{RL}	5		10		10		10		20		ns	2
Data Valid from $\overline{R}$ High	t_{DV}	5		5		5		5		5		ns	2
$\overline{R}$ High to High Z	t_{RHZ}		20		25		25		25		35	ns	2
$\overline{R}$ Low to $\overline{EF}$ Low	t_{REF}		30		45		60		70		110	ns	2
$\overline{EF}$ High to Valid Read	t_{EFR}		5		5		10		10		10	ns	2
$\overline{W}$ High to $\overline{EF}$ High	t_{WEF}		30		45		60		70		110	ns	2
Read Protect Indeterminate	t_{RPI}		15		20		25		25		35	ns	2

HALF-FULL MODE

Unlike the full and empty flags, the half-full flag does not prevent device reads and writes. This flag is set by the next falling edge of write when the memory is 256 locations full. The flag will remain set until the memory is less than or equal to 256 locations full. The read operation (rising edge), which results in the memory being 256 locations full, removes the flag.

HALF-FULL FLAG TIMING Figure 9



8

HALF-FULL FLAG AC CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

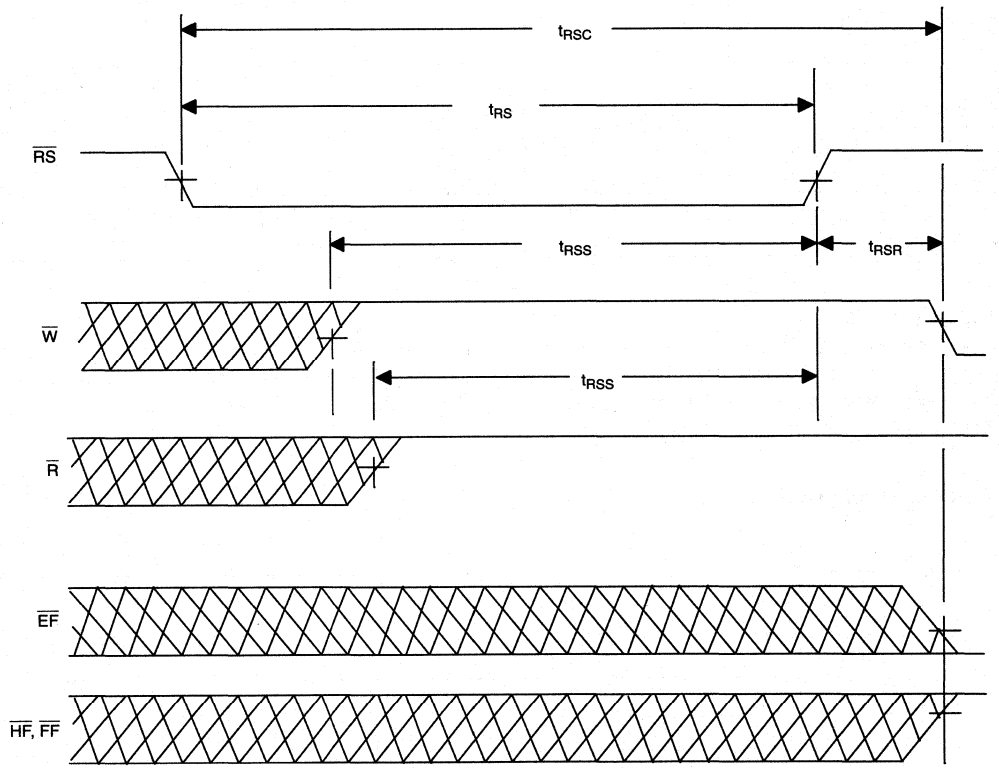
		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120		
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Write Low to Half-Full Flag Low	t_{WHF}		45		65		80		100		140	ns
Read High to Half-Full Flag High	t_{RHF}		45		65		80		100		140	ns

RESET

The DS2009 is reset (see Figure 10) whenever the Reset pin ($\overline{RS}$) is in the low state. During a reset, both the internal read and write pointer are set to the first location. Reset is required after a power-up before a write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ are $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during reset.

RESET Figure 10



NOTES:

$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during reset, but flags will be valid at t_{RSC}.

RESET AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-80		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Reset Cycle Time	t_{RSC}	45		65		80		100		140		ns	
Reset Pulse Width	t_{RS}	35		50		65		80		120		ns	1
Reset Recovery Time	t_{RSR}	10		15		15		20		20		ns	
Reset Setup Time	t_{RSS}	30		40		50		60		100		ns	2

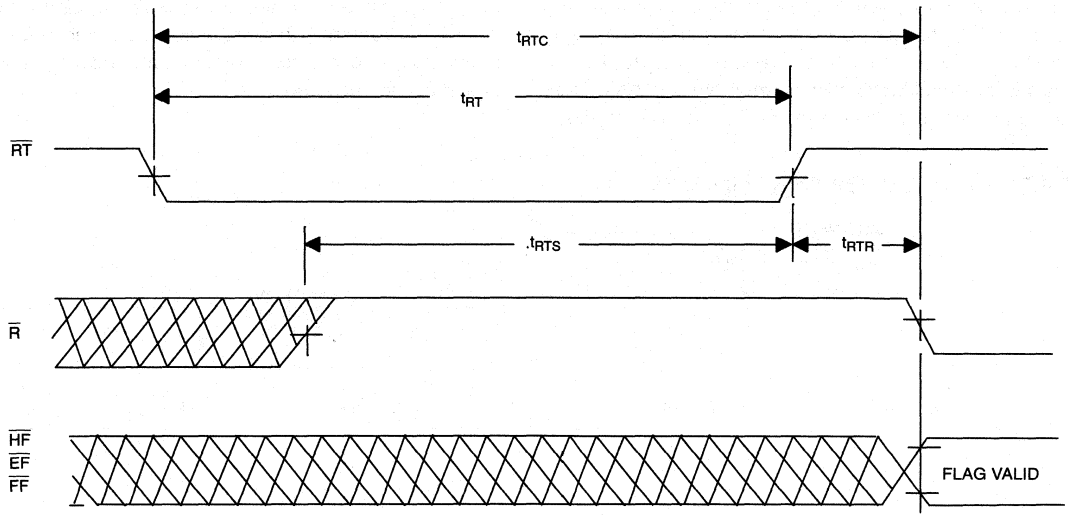
RETRANSMIT

The DS2009 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 11).

A retransmit operation sets the internal read pointer to the first physical location in the array but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high and must remain high for t_{RTR} afterwards.

The retransmit function is particularly useful when blocks of less than 512 writes are performed between resets. The retransmit feature is not compatible with depth expansion.

RETRANSMIT Figure 11



NOTE:

$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during retransmit, but flags will be valid at t_{RTC}.

RETRANSMIT
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-80		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Retransmit Cycle Time	t_{RTC}	45		65		80		100		140		ns	
Retransmit Pulse Width	t_{RT}	35		50		65		80		120		ns	1
Retransmit Recovery Time	t_{RTR}	10		15		15		20		20		ns	
Retransmit Setup Time	t_{RTS}	30		40		50		60		100		ns	

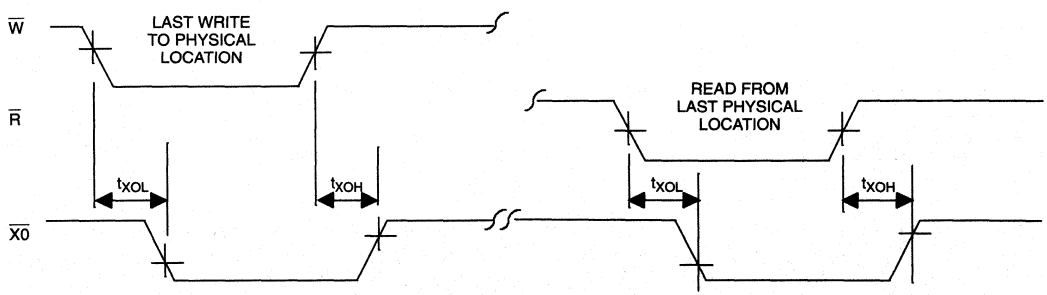
EXPANSION TIMING

Figures 12 and 13 illustrate the timing of the expansion out and expansion in signals. Discussion of expansion out/expansion in timing is provided to clarify how depth expansion works. Inasmuch as expansion out pins are generally connected only to expansion in pins, the user need not be concerned with actual timing in a normal depth expanded application unless extreme propagation delays exist between the $\overline{XO}$ and $\overline{XI}$ pin pairs.

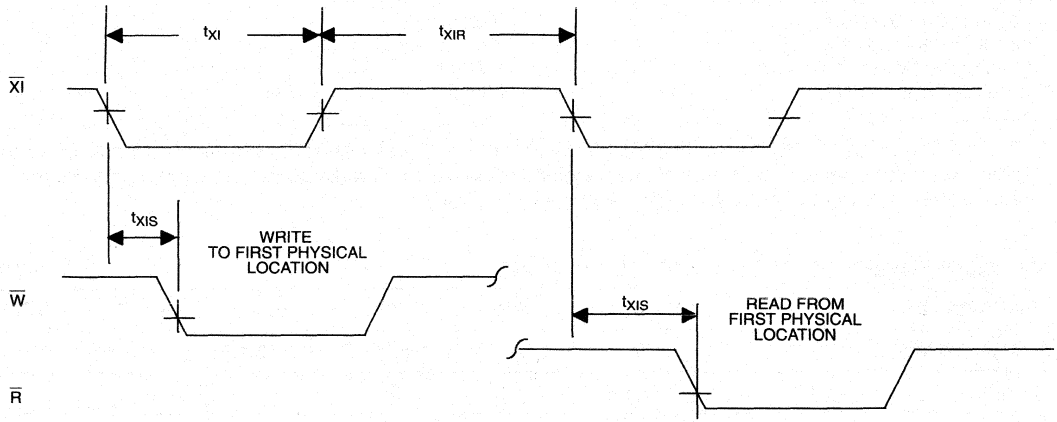
Expansion out pulses are the image of the write and read signals that cause them: delayed in time by t_{XOL} and t_{XOH}. The expansion out signal is propagated when the last physical location in the memory array is written and again when it is read (last read). This is in contrast to when the full and empty flags are activated, which is in response to writing and reading a last available location.

When in depth expansion mode, a given DS2009 will begin writing and reading as soon as valid write and read signals begin, provided $\overline{FL}$ was grounded at reset time. A DS2009 in depth expansion mode with $\overline{FL}$ high at reset will not begin writing until after an expansion in pulse occurs. It will not begin reading until a second expansion in pulse occurs and the empty flag has gone high. Expansion in pulses must occur t_{XIS} before the write and read signals they are intended to enable. Minimum expansion in pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

EXPANSION OUT TIMING Figure 12



EXPANSION IN TIMING Figure 13



EXPANSION LOGIC
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%)

		DS2009-35		DS2009-80		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Expansion Out Low	t_{XOL}		30		45		55		70		100	ns	
Expansion Out High	t_{XOH}		30		45		55		70		100	ns	
Expansion in Pulse Width	t_{XI}	35		50		65		80		120		ns	1
Expansion in Recovery Time	t_{XIR}	10		15		15		20		20		ns	
Expansion in Setup Time	t_{XIS}	15		20		25		30		40		ns	

AC TEST CONDITIONS

Input Levels	GND to 3.0V
Transition Times	5ns
Input Signal Timing Reference Level	1.5V
Output Signal Timing Reference Level	0.8V and 2.2V
Ambient Temperature	0°C to +70°C
V_{CC}	5.0V ± 10%

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Total Device Power Dissipation	1 Watt
Output Current per Pin	20 mA

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	3
Ground	GND		0		V	
Logic 1 Voltage All Inputs	V_{IH}	2.0		V_{CC} +0.3	V	3
Logic 0 Inputs	V_{IL}	-0.3		+0.8	V	3, 4

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current (Any Input)	I_{IL}	-1		1	µA	5
Output Leakage Current	I_{OL}	-10		10	µA	6
Output Logic 1 Voltage I_{OUT} = -1mA	V_{OH}	2.4			V	3
Output Logic 0 Voltage I_{OUT} = 4mA	V_{OL}			0.4	V	3
Average V_{CC} Power Supply Current – 35ns, 50ns, 60ns, 80ns, 120ns	I_{CC1}			100	mA	7, 9
Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL/RT}$ = V_{IH})	I_{CC2}			8	mA	7
Power Down Current (All Input = V_{CC} -0.2V)	I_{CC3}			500	µA	7, 10

CAPACITANCE

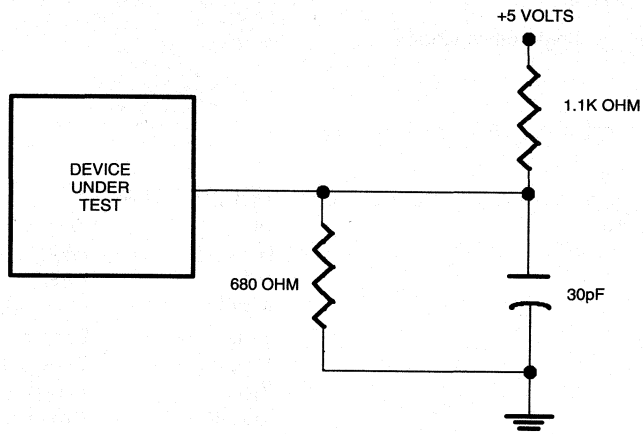
(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on Input Pins	C_I			7	pF	
Capacitance on Output Pins	C_O			12	pF	8

NOTES:

1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load diagram.
3. All voltages are referenced to ground.
4. -1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.4 \le V_{IN} \le V_{CC}$.
6. $\overline{R} \ge V_{IH}$, $0.4 \ge V_{OUT} \le V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.
9. DS2010, DS2011, DS2012, and DS2013 have I_{CC1}, = 120 mA MAX for 50ns, 65ns, 80ns, and 120ns speed grades.
10. DS2010 has I_{CC3} = 1mA MAX; DS2011, DS2012, DS2013 have I_{CC3} = 2mA MAX.

OUTPUT LOAD Figure 14



8

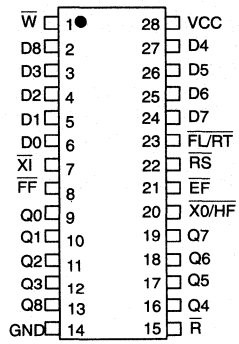
DALLAS SEMICONDUCTOR

DS2010
1024 x 9 FIFO Chip

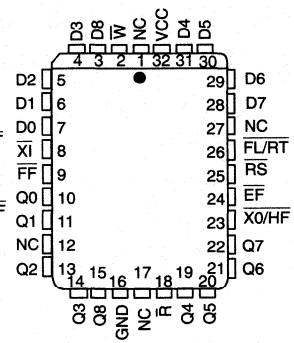
FEATURES

- First-in, first-out memory-based architecture
- Flexible 1024 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50ns, 65ns, 80ns, and 120ns access times
- Optional industrial temperature range -40°C to +85°C available, designated N

PIN ASSIGNMENT



28-Pin DIP
(300 and 600 Mil)
See Mech. Drawings Section



32-Pin PLCC
See Mech. Drawings Section

PIN DESCRIPTION

$\overline{W}$	–	WRITE
$\overline{R}$	–	READ
$\overline{RS}$	–	RESET
$\overline{FL/RT}$	–	First Load/Retransmit
D_{0-8}	–	Data In
Q_{0-8}	–	Data Out
$\overline{XI}$	–	Expansion In
$\overline{XO/HF}$	–	Expansion Out/Half Full
$\overline{FF}$	–	Full Flag
$\overline{EF}$	–	Empty Flag
V_{CC}	–	5 Volts
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS2010 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2010 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.

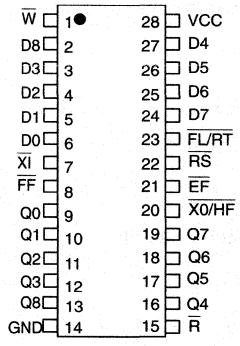
DALLAS SEMICONDUCTOR

DS2011
2048 x 9 FIFO Chip

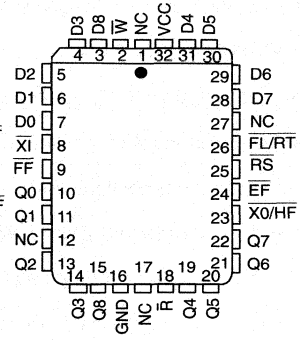
FEATURES

- First-in, first-out memory-based architecture
- Flexible 2048 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 50 ns, 65 ns, 80 ns, and 120 ns access times
- Optional industrial temperature range -40°C to +85°C available, designated N

PIN ASSIGNMENT



28-Pin DIP
(300 and 600 Mil)
See Mech. Drawings Section



32-Pin PLCC
See Mech. Drawings Section

PIN DESCRIPTION

$\overline{W}$	–	WRITE
$\overline{R}$	–	READ
$\overline{RS}$	–	RESET
$\overline{FL/RT}$	–	First Load/Retransmit
D_{0-8}	–	Data In
Q_{0-8}	–	Data Out
$\overline{XI}$	–	Expansion In
$\overline{XO/HF}$	–	Expansion Out/Half Full
$\overline{FF}$	–	Full Flag
$\overline{EF}$	–	Empty Flag
V_{CC}	–	5 Volts
GND	–	Ground
NC	–	No Connect

8

DESCRIPTION

The DS2011 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2011 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.

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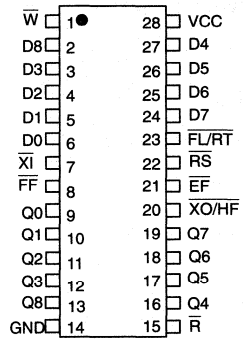
DALLAS SEMICONDUCTOR

DS2012
4096 x 9 FIFO Chip

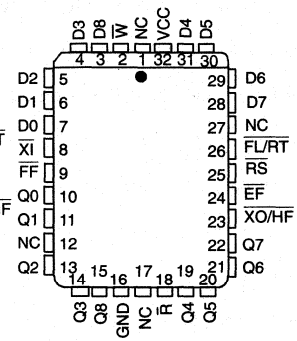
FEATURES

- First-in, first-out memory-based architecture
- Flexible 4096 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50 ns, 65 ns, 80 ns, and 120 ns access times
- Optional industrial temperature range -40°C to +85°C available, designated N

PIN ASSIGNMENT



28-Pin DIP (600 Mil)
See Mech. Drawings Section



32-Pin PLCC
See Mech. Drawings Section

PIN DESCRIPTION

$\overline{W}$	–	WRITE
$\overline{R}$	–	READ
$\overline{RS}$	–	RESET
$\overline{FL/RT}$	–	First Load/Retransmit
D_{0-8}	–	Data In
Q_{0-8}	–	Data Out
$\overline{XI}$	–	Expansion In
$\overline{XO/HF}$	–	Expansion Out/Half Full
$\overline{FF}$	–	Full Flag
$\overline{EF}$	–	Empty Flag
V_{CC}	–	5 Volts
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS2012 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half full flags, and unlimited expansion capability in both word size and depth. The DS2012 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.

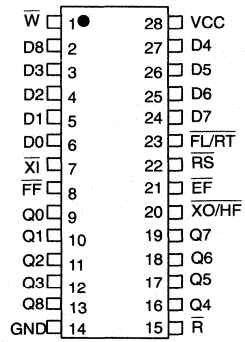
DALLAS SEMICONDUCTOR

DS2013
8192 x 9 FIFO Chip

FEATURES

- First-in, first-out memory-based architecture
- Flexible 8192 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50 ns, 65 ns, 80 ns, and 120 ns access times
- Optional industrial temperature range -40°C to +85°C available designated N

PIN ASSIGNMENT



28-Pin DIP (300 and 600 Mil)
See Mech. Drawings Section

PIN DESCRIPTION

$\overline{W}$	–	WRITE
$\overline{R}$	–	READ
$\overline{RS}$	–	RESET
$\overline{FL/RT}$	–	First Load/Retransmit
D^0_{-8}	–	Data In
Q^0_{-8}	–	Data Out
$\overline{XI}$	–	Expansion In
$\overline{XO/HF}$	–	Expansion Out/Half Full
$\overline{FF}$	–	Full Flag
$\overline{EF}$	–	Empty Flag
V_{CC}	–	5 Volts
GND	–	Ground
NC	–	No Connect

8

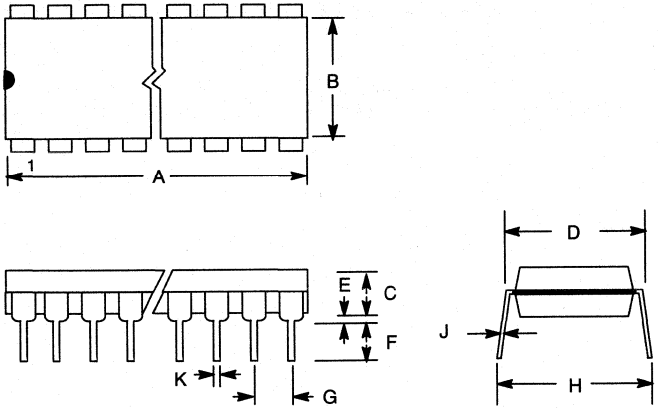
DESCRIPTION

The DS2013 8192 x 9 FIFO Chip implements a first-in, first-out algorithm, featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2013 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to DS2009 512 x 9 FIFO Chip data sheet for detailed device description.

MECHANICAL DRAWINGS

9

8– TO 28–PIN DIP (300 MIL)



Includes:
DS1200
DS1259
DS2009D
DS2010D
DS2011D
DS2013D

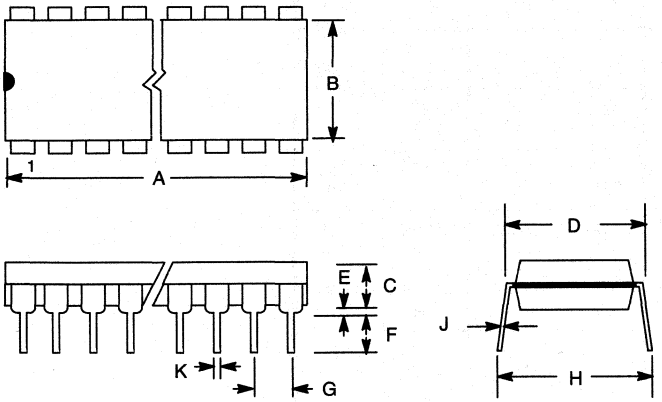
PKG	8-PIN		10-PIN		14-PIN		16-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.360	0.400	0.480	0.520	0.740	0.780	0.740	0.780
MM	9.14	10.16	12.19	13.21	18.80	19.81	18.80	19.81
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02
F IN.	0.120	0.140	0.110	0.130	0.120	0.140	0.120	0.140
MM	3.04	3.56	2.79	3.30	3.04	3.56	3.04	3.56
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
H IN	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
MM	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53

Continued on following page.

PKG	18-PIN		20-PIN		24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	0.890 22.61	0.920 23.36	0.970 24.63	1.040 26.42	1.150 29.21	1.260 32.00	1.345 34.16	1.370 34.80
B IN. MM	0.240 6.10	0.260 6.60	0.240 6.09	0.270 6.86	0.250 6.35	0.270 6.86	0.270 6.85	0.295 7.49
C IN. MM	0.120 3.05	0.140 3.56	0.120 3.05	0.140 3.56	0.120 3.05	0.140 3.56	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26	0.295 7.49	0.325 8.26	0.300 7.62	0.325 8.26	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02	0.015 0.38	0.040 1.02	0.015 0.38	0.040 1.02	0.015 0.38	0.050 1.27
F IN. MM	0.120 3.04	0.140 3.56	0.120 3.04	0.140 3.56	0.125 3.18	0.135 3.48	0.125 3.18	0.135 3.48
G IN. MM	0.090 2.23	0.110 2.79	0.090 2.23	0.110 2.79	0.090 2.23	0.110 2.79	0.090 2.23	0.110 2.79
H IN MM	0.320 8.13	0.370 9.40	0.310 7.87	0.390 9.91	0.320 8.13	0.370 9.40	0.320 8.13	0.370 9.40
J IN MM	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53	0.015 0.38	0.022 0.56	0.015 0.38	0.022 0.56

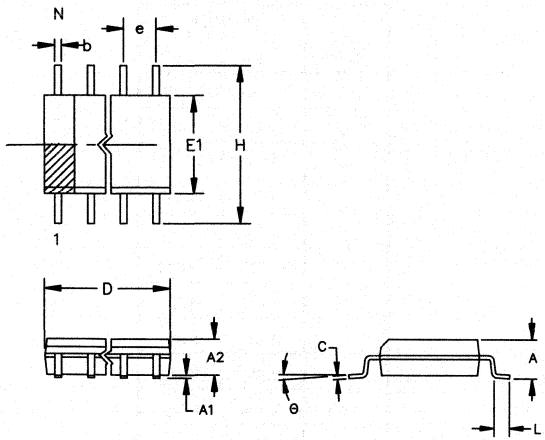
24– TO 40–PIN DIP (600 MIL)

Includes:
DS1609
DS2009
DS2010
DS2011
DS2012
DS2013



PKG	24-PIN		28-PIN		40-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	1.245 31.62	1.270 32.25	1.445 36.70	1.470 37.34	2.050 52.07	2.075 52.71
B IN. MM	0.530 13.46	0.550 13.97	0.530 13.46	0.550 13.97	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06	0.140 3.56	0.160 4.06	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88	0.600 15.24	0.625 15.88	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.380	0.050 1.27	0.015 0.380	0.040 1.02	0.015 0.380	0.040 1.02
F IN. MM	0.120 3.05	0.145 3.68	0.120 3.05	0.145 3.68	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79
H IN MM	0.625 15.88	0.675 17.15	0.625 15.88	0.675 17.15	0.625 15.88	0.675 17.15
J IN MM	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56	0.015 0.38	0.022 0.56	0.015 0.38	0.022 .56

16–, 20–, 24–, 28–PIN SOIC (300 MIL)

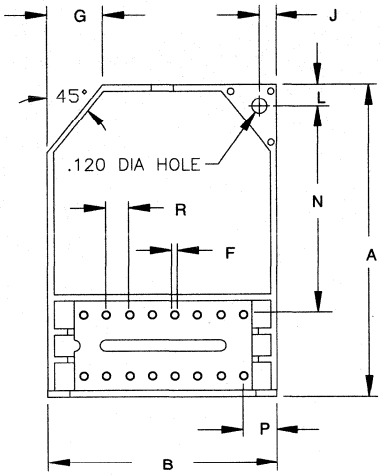


Includes:
DS1200S
DS1259S
DS1609S

The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

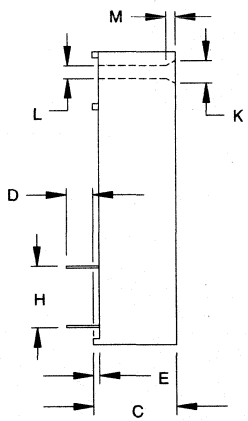
PKG	16-PIN		20-PIN		24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68	0.094 2.39	0.105 2.67
A1 IN. MM	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33
D IN. MM	0.398 10.11	0.412 10.46	0.498 12.65	0.511 12.99	0.598 15.19	0.612 15.54	0.698 17.73	0.712 18.08
e IN. MM	0.050 BSC 1.27 BSC						0.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02	0.016 0.406	0.040 1.20	0.016 0.40	0.040 1.02	0.016 0.40	0.040 1.02
Θ	0°	8°	0°	8°	0°	8°	0°	8°

DS1260 SMART BATTERY

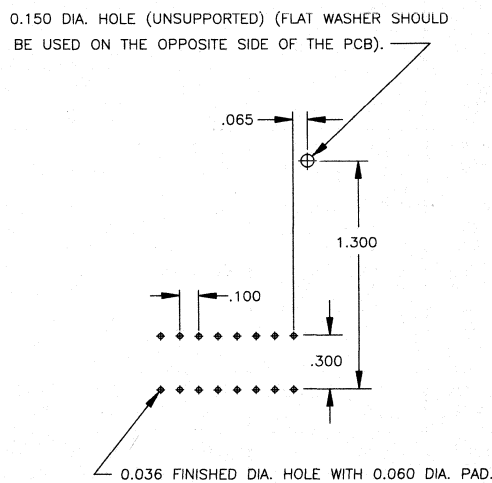


BOTTOM VIEW

DIM	INCHES	
	MIN	MAX
A	1.480	1.500
B	1.030	1.050
C	0.390	0.415
D	0.125	0.145
E	0.020	0.040
F	0.016	0.020
G	0.240	0.260
H	0.295	0.315
J	0.090	0.110
K	0.160	0.180
L	0.110	0.130
M	0.035	0.065
N	0.985	1.010
P	0.155	0.175
R	0.095	0.105

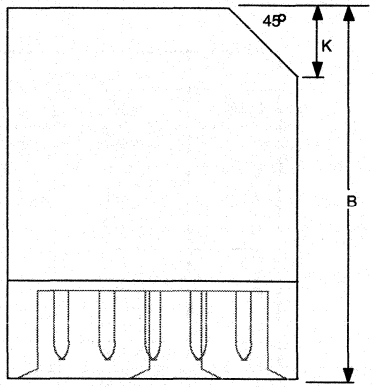


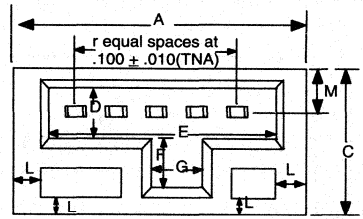
SIDE VIEW

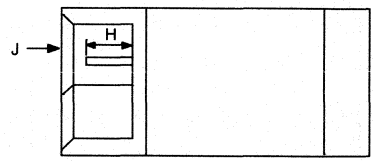


ELECTRONIC KEY/TAG

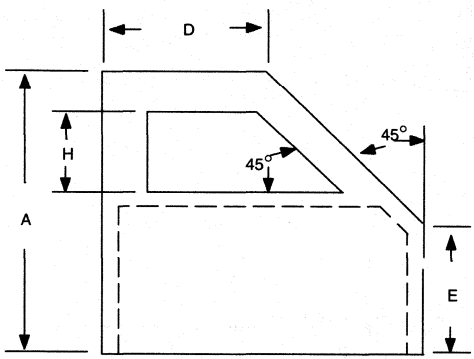
Includes:
DS1201

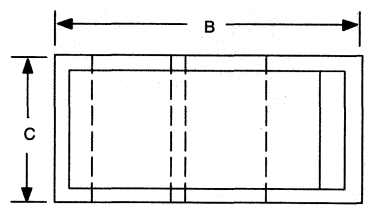






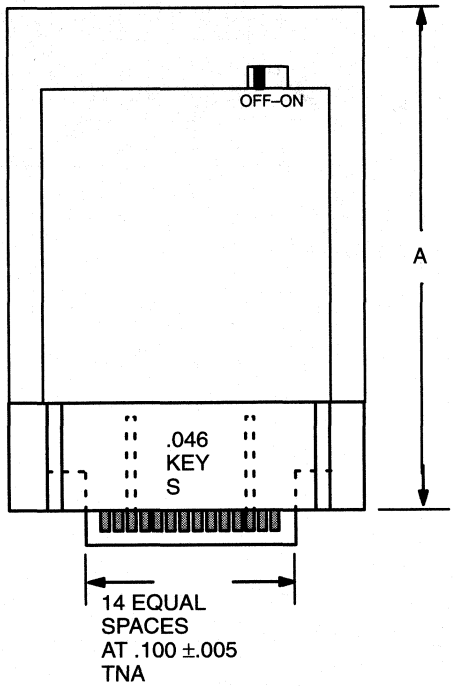
KEY/TAG CAP



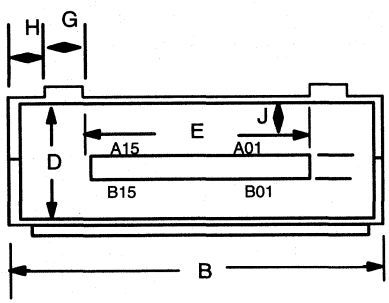


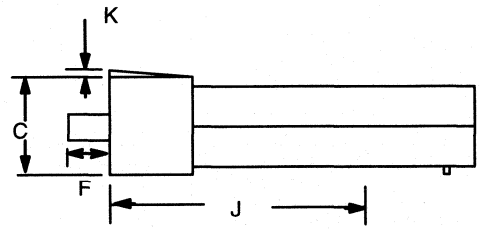
PKG	ELECTRONIC KEY/TAG		KEY/TAG CAP	
DIM	MIN	MAX	MIN	MAX
A IN. MM	0.610 15.50	0.650 16.51	0.790 20.07	0.810 20.57
B IN. MM	0.740 18.80	0.760 19.30	0.680 17.27	0.700 17.78
C IN. MM	0.310 7.87	0.355 9.02	0.405 10.29	0.425 10.80
D IN. MM	0.100 2.54	0.110 2.79	0.290 7.37	0.310 7.87
E IN. MM	0.505 12.83	0.515 13.08	0.410 10.41	0.430 10.92
F IN. MM	0.100 2.54	0.110 2.79		

NON-VOLATILE READ/WRITE CARTRIDGE

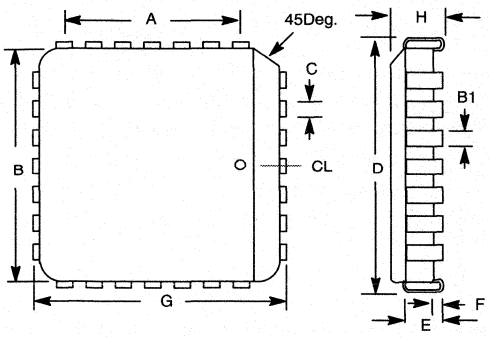


	INCHES	
DIM	MIN	MAX
A	3.020	3.040
B	2.275	2.295
C	0.600	0.630
D	0.440	0.460
E	1.590	1.607
F	0.115	0.135
G	0.115	0.135
H	0.140	0.160
J	1.760	1.790
K	0.040	0.060

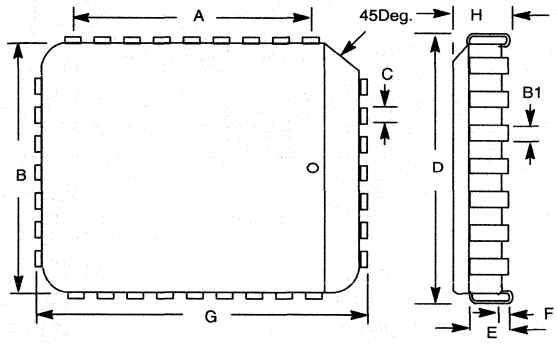




28- AND 32- PIN PLASTIC LEADED CHIP CARRIERS (PLCC)



28- Pin Includes:

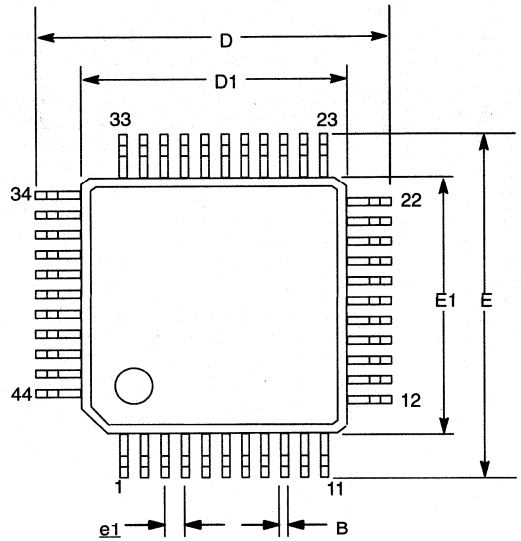


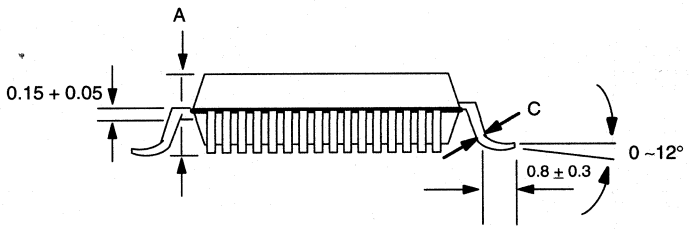
32-Pin Includes:
DS2009R
DS2010R
DS2011R
DS2012R

PKG	28-PIN		32-PIN	
DIM	MIN	MAX	MIN	MAX
A IN. MM	0.300 BSC 7.62		0.400 BSC 10.16	
B IN. MM	0.445 11.30	0.460 11.68	0.442 11.30	0.460 11.68
B1 IN MM	0.013 0.33	0.021 0.53	0.013 0.33	0.021 0.53
C IN MM	0.027 0.68	0.33 0.84	0.027 0.68	0.33 0.84
D IN. MM	0.480 12.19	0.500 12.70	0.480 12.19	0.500 12.70
D2 IN. MM	0.390 9.91	0.430 10.92	0.390 9.91	0.430 10.92
E IN. MM	0.090 2.29	0.120 3.05	0.060 1.52	0.095 2.41
E2 IN. MM	0.390 9.91	0.430 10.92	0.490 12.45	0.530 13.46
F IN. MM	0.020 0.51		0.015 0.38	
G IN MM	0.480 12.19	0.500 12.70	0.580 14.7	0.600 15.24
H IN MM	0.165 4.19	0.180 4.57	0.100 2.54	0.140 3.56

44–PIN QUAD FLAT PACK (PRELIMINARY)

Includes:
DS1280

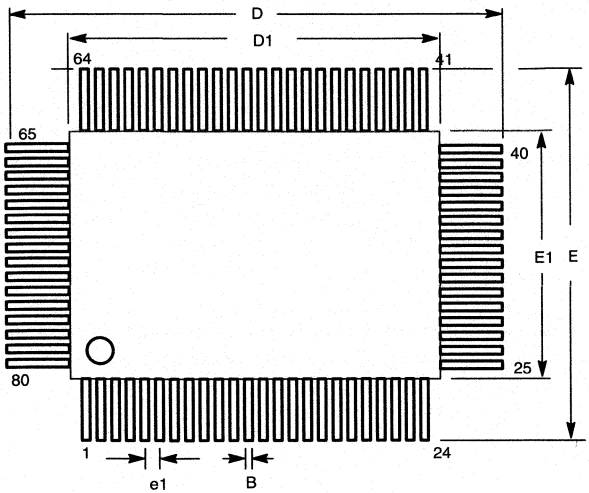


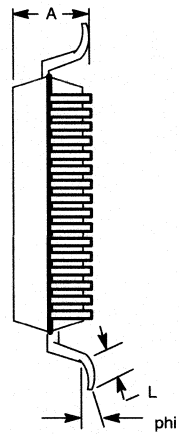


PKG	10 X 10 BODY		14 X 14 BODY	
DIM	MIN	MAX	MIN	MAX
A MM	–	2.45	–	3.4
B MM	0.30	0.45	0.20	0.50
C MM	0.13	0.23	0.10	0.20
D MM	13.65	14.35	16.95	18.00
E MM	13.65	14.35	16.95	18.00
D1 MM	9.90	10.10	13.80	14.20
E1 MM	9.90	10.10	13.80	14.20
L MM	0.65	0.95	0.50	1.10
e1 IN MM	0.315 0.80 BSC		0.039 1.00 BSC	

80-PIN QUAD FLAT PACK (14.0 MM X 20.0 MM)

Includes:
DS1280





PKG	80-PIN	
DIM	MIN	MAX
A IN. MM	0.11 2.80	0.128 3.25
B IN. MM	0.010 0.25	0.020 0.45
e1 IN. MM	0.031 BSC 0.80 BSC	
D1 IN. MM	0.781 19.85	0.793 20.15
E1 IN. MM	0.545 13.85	0.557 14.15
E IN. MM	0.688 17.50	0.720 18.30
D IN. MM	0.921 23.40	0.953 24.20
L IN MM	0.025 0.65	0.038 0.95
phi	0°	8°

9